**IEEE P802.15**

**Wireless Personal Area Networks**

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| Project | IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs) |
| Title | Proposed text to clarify the HCS generation for dyamic data mode PHR |
| Date Submitted | October 2024 |
| Sources | Vinod Kristem, Xiliang Luo (Apple) |
| Re: |  |
| Abstract |  |
| Purpose | To propose the text to clarify the HCS generation for dyamic data mode PHR in “*P802.15.4ab™/D01 Draft Standard for Low-Rate Wireless Networks*” |
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**Discussion:**

Please refer to the DCN 15-24-0558-00-04ab-HCS-generation-for-Dynamic-PHR

**Proposed Change:**

Update the Draft D01 spec as suggested below:

**16.2.7.4.3 PHR2**

***Update the last paragraph of 16.2.7.4.3 as follows:***

The HCS field shall be an 8-bit CRC computed over the first 15 bits of the ~~PHR~~ PHR2, that is referred to as calculation field. The HCS shall be calculated using the polynomial , generated and transmitted as specified ~~in 21.2.4 (PHR of SUN OFDM PHY)~~ below.

The HCS is the one’s complement of the modulo-2 sum of the two remainders in a) and b):

a) The remainder resulting from divided (modulo 2) by , where the value is the number of bits in the calculation field.

b) The remainder resulting from the calculation field contents, treated as a polynomial, multiplied by and then divided (modulo 2) by .

As a typical implementation, at the transmitter, the initial remainder of the division shall be preset to all ones and is then modified via division of the calculation field by the generator polynomial . The one’s complement of this remainder is the HCS field. The HCS field is transmitted commencing with the coefficient of the highest order term.

At the receiver, the initial remainder is preset to all ones and the serial incoming 23 bits of the calculation field concatenated with HCS, when divided by in the absence of transmission errors, results in a unique non-zero remainder value. The unique remainder value is the polynomial , equivalent to a hex value of *0X0C*.

A typical implementation of HCS generation is depicted in Figure x.

1. Initialize the remainder register to all ones.
2. Shift the sequence into the divider beginning with .
3. After the last bit, , is shifted into the divider, the one’s complement of the remainder register contains the HCS:

A black background with a black square

Description automatically generated with medium confidence

Figure x: Typical HCS implementation for PHR2

An example PHR2 with HCS is shown in Figure y.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bits: 0 | 1 | 2-13 | | | | | | | | | | | | 14 | 15-22 | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |

Figure y: Example PHR2 with HCS