**IEEE P802.15**

**Wireless Personal Area Networks**

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| Project | IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs) | |
| Title | **D4 Comment resolution instructions** | |
| Date Submitted | [17 March 2021] | |
| Source | [] [] [address] | Voice: [ ] Fax: [ ] E-mail: [ ] |
| Re: | Comment resolution on D4 | |
| Abstract |  | |
| Purpose | Aid comment resolution | |
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### CID A-19

***Remove the definition of HCM on page 20***

***Remove the following text from P27L28-31:***

, M-ary pulse amplitude modulation (PAM) with Hadamard-coded modulation 29 (HCM) without the all-ones code

***Change P28L17-19 as follows:***

Binary pulse-amplitude modulation (2-PAM) with 8B10B line coding, as defined in 9.3.5 is supported. It is combined with Reed-Solomon (RS) forward error correction (FEC) to correct errors due to the noise.

***Remove HCM Allocation element from Table 4 Control frame subtypes.***

***Remove 6.6.17 HCM Allocation element and renumber the subsequent clauses.***

***Change 6.6.20 as follows:***

**6.6.20 PM-PHY MCS element**

The *PM-PHY MCS* element, shown in 0, holds a subset of supported MCS for the PM-PHY.

|  |
| --- |
| **1 Octet** |
| Clock Rates |

**PM-PHY MCS element**

**Clock Rates:** A bitmap indicating the set of supported clock rates. Reserved bits shall be set to 0. A 1 in the bitmap indicates that the given clock rate is supported. A 0 indicates that the clock rate is not supported. 0 shows the bitmap structure.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | processed first | | | | processed  last | | | | |
| 1. **Bit in the bitmap:** | 0 | 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
| 1. **Clock rate:** | 12.5 MHz | 25 MHz | 50 MHz | 100 MHz | | 200 MHz | reserved | reserved | reserved |

**Clock rate bitmap**

***Remove entry 13 HCM Allocation from table 12***

***Remove capHcm from table 37***

***Replace the sentence “PM-PHY enables moderate data rates from 1 Mb/s to some 100 Mb/s.” with:***

PM-PHY enables moderate data up to around 100 Mb/s.

***Change the sentences on P103L7-11 as follows:***

2-PAM with 8B10B line coding and RS FEC is used. The PM-PHY includes means to adapt the data rate of the link to varying channel conditions by varying the clock rate on a per PPDU basis.

***Change table 39 as follows:***

* ***Modulation: 2-PAM***
* ***Line Coding: 8B10B***
* ***Replace “Data rates with 2-PAM and 8b10b” with “Data rates”***
* ***Remove the “Min” column”***

***Replace the text on P103L15-16 with***

The base MCS for the PM-PHY shall be Clock Rate ID = 0, i.e., use 2-PAM, 12.5 MHz clock rate.

***Change the sentence in P104L12 as follows:***

PPDU header fields that contain numbers shall be transmitted starting with the LSB of the number first to the MSB of the number last.

***Remove “independent of the clock rate” in P104L16.***

***Change P104L19 as follows:***

The second section is intended for channel estimation and synchronization. It enables both, cross- and autocorrelation with an appropriate window size.

NOTE – The general approach has been described by Schmidl and Cox [B12], Minn et al. [B3], Schellmann et al. [B10] and Goroshko et al. [B9].

For the preamble, the base sequence A8, a specific pseudo-noise sequence of length 8 is used, as defined in B.2. A8 is repeated six times yielding a total sequence length of Each base sequence of length 8 is multiplied with positive or negative sign as given below which is known to create a sharper peak after autocorrelation, compared to a double sequence of the same total length as described by Goroshko [B9]. The total preamble reads [A8 A8 A8 A8 A8 A8] where for elements of the sequence. The preamble is finally passed through the 2-PAM Modulator.

***Remove table 41.***

***Delete “data stream /” in P106L7***

***Remove “The MCS 12 ID is composed as depicted in Figure 75.” in P107L12-13***

***Remove figure 75***

***Change text in P107L15-L20 as follows:***

MCSs are defined by the applied clock rate. The Clock Rate ID describes the used clock rate as defined in Table 43. The data rate for each MCS can be derived based on the corresponding clock rate and cyclic prefix duration. For instance, using RS(256,248) with 2-PAM, 8B10B and clock rate 12.5 MHz yields 9.6 Mb/s.

Table X ***(TE: adapt number)*** defines the relationship between MCS ID and clock rate.

***Insert a new table X at the end of subclause 9.2.5 as follows:***

***Create three columns MCS ID, Clock rate ID, Clock rate***

***Insert a row: MCS ID 0, Clock rate ID 0, Clock rate 12.5 MHz***

***Insert a row: MCS ID 1, Clock rate ID 1, Clock rate 25 MHz***

***Insert a row: MCS ID 2, Clock rate ID 2, Clock rate 50 MHz***

***Insert a row: MCS ID 3, Clock rate ID 3, Clock rate 100 MHz***

***Insert a row: MCS ID 4, Clock rate ID 4, Clock rate 200 MHz***

***Change “Channel estimation sequence, defined in B.2” to “Payload Channel estimation sequence, defined in B.2” in table 43.***

***Remove “For specific MCS, only a subset of the blocks may be used.” in P107L25.***

***Replace figure 76 with the following figure:***



***Change the text in P108L3-14 as follows:***

Header or payload data enters the transmitter and is scrambled in order to randomize uncoordinated interference. 8B10B line coding is applied as the second step. For FEC, the payload uses RS(256, 248) and the header uses RS(36, 24).

NOTE - According to Ivry **Fehler! Verweisquelle konnte nicht gefunden werden.** and Boada **Fehler! Verweisquelle konnte nicht gefunden werden.**, a particular order of line and channel coding shown in **Fehler! Verweisquelle konnte nicht gefunden werden.** achieves lowest error rates. After FEC, only the systematic part of the binary output code word (248 bits) is well balanced.

For maintaining a constant average light output, also the redundant part of the binary code word (360 – 240 = 120 bits in case of header data and 2560-2480 = 80 bits in case of payload data) passes through 8B10B line encoder. Both parts are concatenated again in a multiplexer. Subsequently, 2-PAM bit-to-symbol mapping is applied for the header.

***Remove P109L17-19.***

***Change text in P109L21-P110L2 as follows:***

The bit-to-symbol mapper is using PAM with 2 levels. For 2 levels, each input bit is mapped in one symbol. The symbols are mapped to levels as {0, 1} to {0, 1}, respectively.

***Remove table 44***

***Remove 9.3.7.***

***Remove Annex B4***