# Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

**Submission Title:** H2020 EPIC Project: Next Generation FEC for Tb/s and THz Systems
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**Re:** n/a

**Abstract:** This talk will give an introduction and overview of H2020 EPIC project. The project content and objectives, with the ultimate target of design and implementation of practical ultra-high speed FEC technology for B5G systems, will be detailed. The FEC design framework of the EPIC project which holistically unifies the information theoretic code design principles with advanced VLSI techniques will be discussed. Based on the inherent trade-offs between the coding theory and efficient FEC architecture design, e.g. in terms randomness, parallel/serial operations, locality, the design space exploration (DSE) figures of all three major code-class, e.g. Turbo codes, LDPC, and Polar codes, will be provided.

**Purpose:** Information of IEEE 802.15 IG THz

# H2020 EPIC Project: Next Generation FEC for Tb/s and THz Systems

The EPIC project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 760150.

**E**nabling **P**ract**i**cal Wireless Tb/s **C**ommunications with Next Generation Channel Coding

# What is EPIC?

- EPIC project designs and implements next generation **FEC technology** for a number of 5G and beyond (B5G) use cases**, primarily within ultra-high speed (>100Gbps) wireless systems (THz)**.

- 3-year (Sept 2017-Sept 2020) project is executed by 8 partners with in-depth expertise in coding theory&algorithm development, FEC implementation, and system-level design.


Fig: Abstracted link-level chain

# Partners:

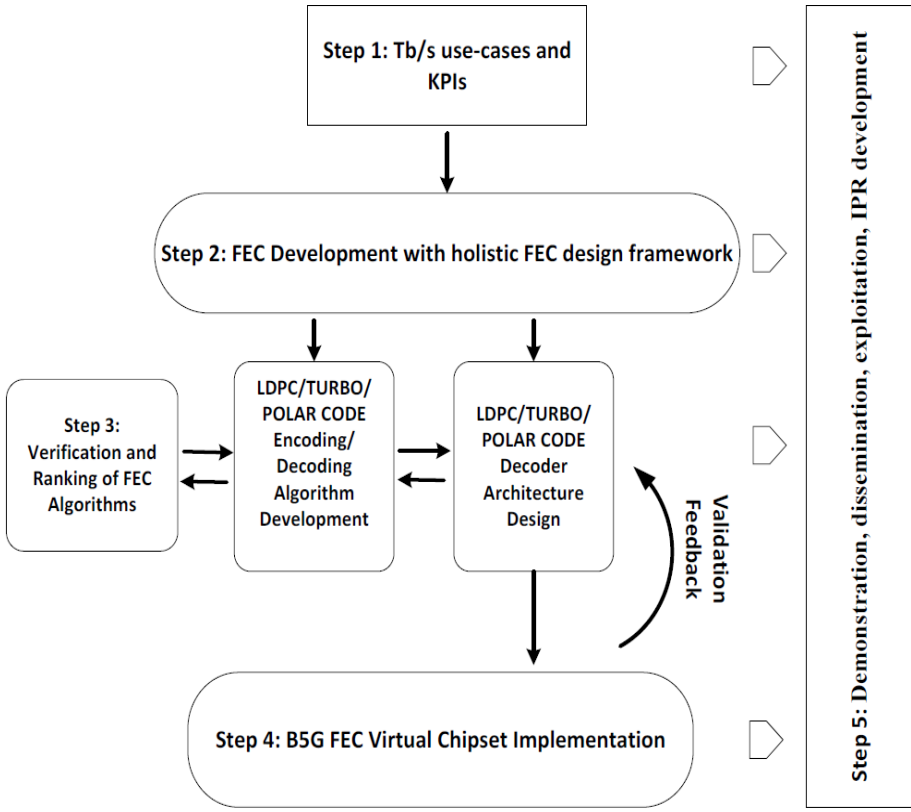
| | |
|---|---|
| TECHNIKON | Technikon Forschungs- und Planungsgesellschaft mbH (Coordinator)<br>Villach, Austria |
| INTERDIGITAL EUROPE | InterDigital Europe Ltd.<br>London, United Kingdom |
| imec | Interuniversitair Micro-Electronica Centrum (imec)<br>Leuven, Belgium |
| POLARAN | Polaran Ltd.<br>Ankara, Turkey |
| TECHNISCHE UNIVERSITÄT KAISERSLAUTERN | Technische Universität Kaiserslautern (Technical Lead)<br>Kaiserslautern, Germany |
| ERICSSON | Ericsson AB<br>Stockholm, Sweden |
| IMT Atlantique Bretagne-Pays de la Loire École Mines-Télécom | Institut Mines-Télécom, IMT Atlantique<br>Brest, France |
| CREONIC ip cores & system solutions | Creonic GMBH<br>Kaiserslautern, Germany |

# EPIC Project Objectives

- **Design** and **implement next generation Forward Error Correction (FEC)** for **wireless Tb/s technology** and **Beyond-5G (B5G) systems**.
- **Advance state-of-the-art Turbo**, **Low Density Parity Check (LDPC),** and **Polar Codes** and develop the principal channel coding technology for wireless Tb/s technology.
- Devise a disruptive **FEC design framework** to **unify algorithmic** and **implementation domains**.
- **Validate** and **demonstrate** the developed FEC technology in **virtual silicon tape-out** and provide **first-in-class wireless Tb/s FEC chipset architecture block**.

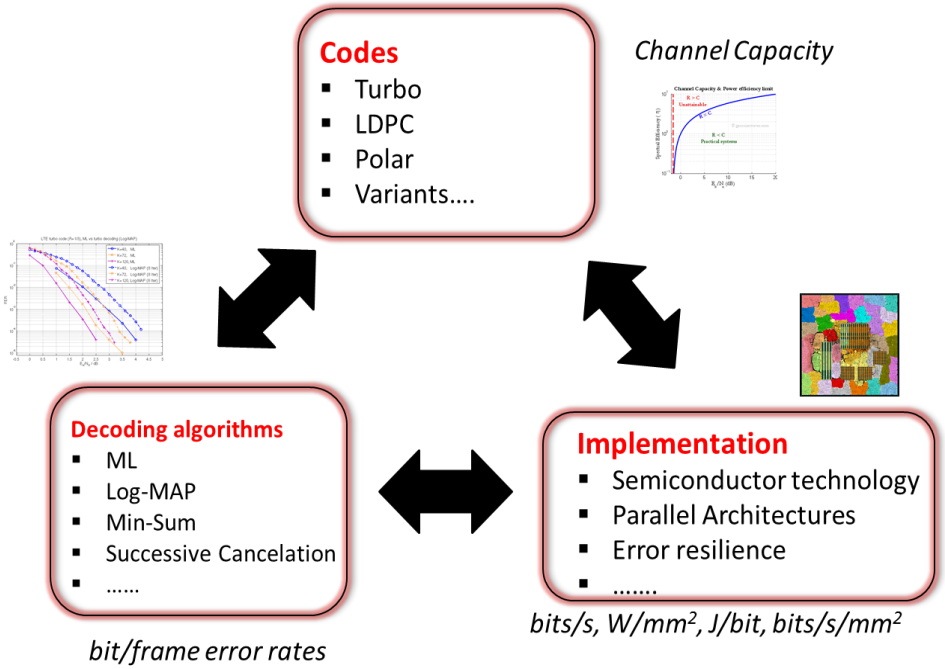
# EPIC Methodology for B5G FEC Technology Design

- Identify B5G use-cases, link level, and FEC requirements in terms of communication and implementation performances
- Execute on EPIC design framework to develop FEC technology according to the FEC requirement guidelines
- Develop LDPC/Turbo/Polar Encoding/Decoding Algorithms
- Implement selected B5G FEC candidates in virtual chipset



# EPIC Design Framework

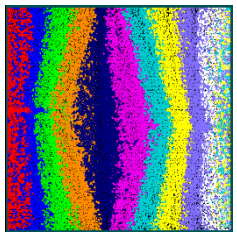
- Holistic approach that combines information-theoretic code design principles with advanced VLSI techniques
  - Objective: To develop highly-optimized dedicated architectures in advanced semiconductor technology nodes
- The framework is driven by key performance trade-offs such as:
  - Code, algorithm and implementation level parameters (code randomness/locality/regularity, decoding algorithm complexity, bit/word/sub-block level parallel vs. sequential architectures, optimality vs. approximation)
  - Communication performance and implementation efficiency KPIs (BER/FER, throughput, energy/power/area efficiency)

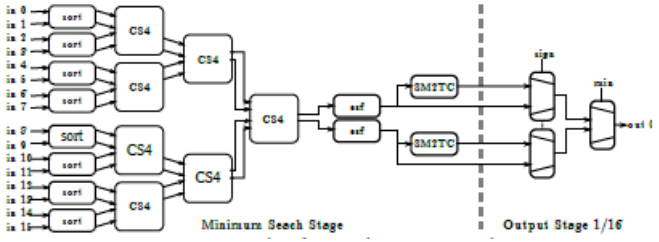


# Information Theory/Implementation Gap

Energy efficient high throughput architectures require

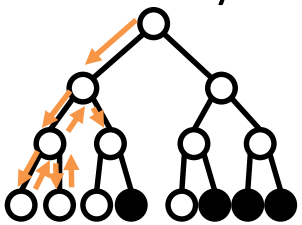
- Large parallelism
- Large regularity
- Large locality

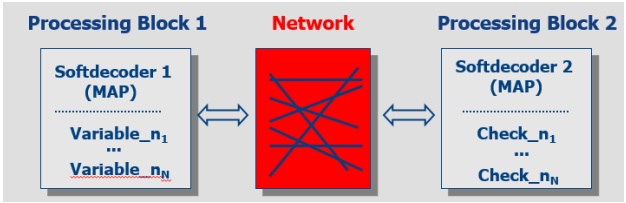





Coding theory requires randomness and no-locality

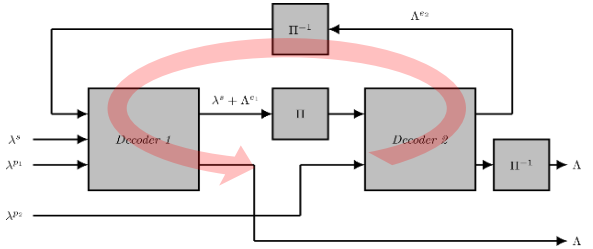
- LDPC: Tanner Graph
- Turbo Code: Interleaver





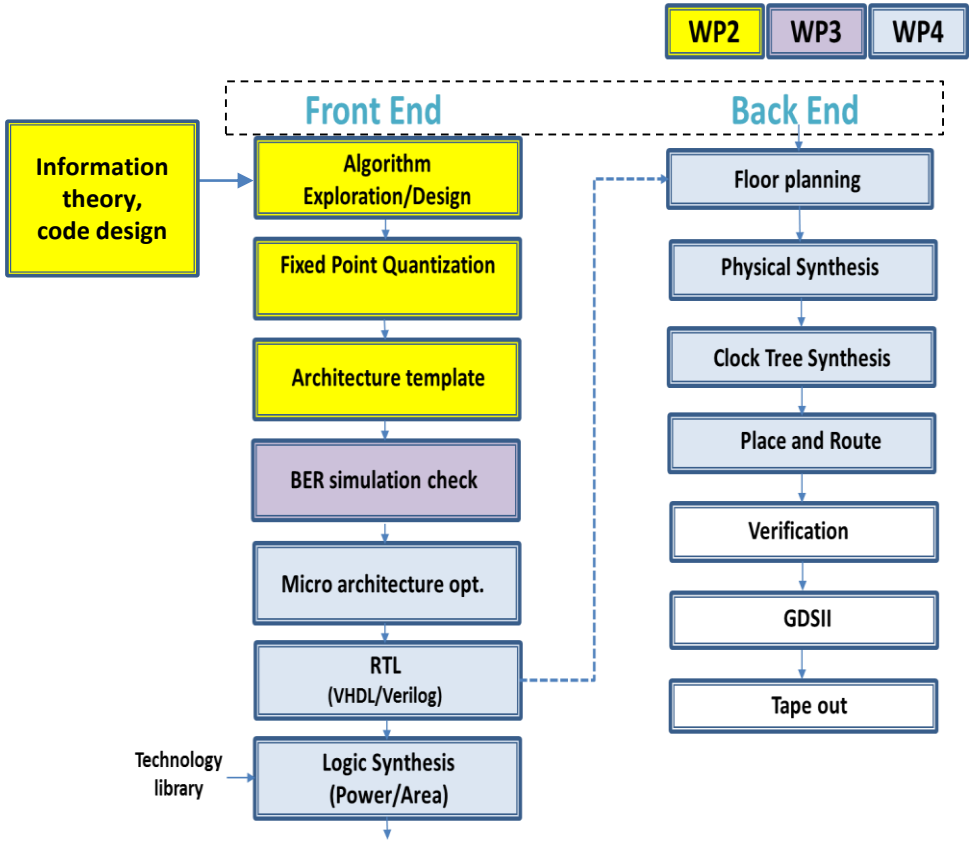

Some decoding algorithms are inherently serial

- Turbo-Code decoding
- Polar Code successive cancelation



# Strong link with Silicon technology

- Information theory, algorithms, architecture and implementation in Silicon are mapped on the technical workpackages
- Selected designs will go all the way through the ASIC implementation (front-end and back-end) in deeply-scaled CMOS
- Target technology node: 7nm CMOS
  - Better area efficiency, better energy efficiency



# B5G use-cases and system-level&FEC requirements

- Explored potential wireless ultra-high throughput use-cases for B5G.
  - System requirements and KPIs (bit and frame error rate, throughput, latency, power, cost, flexibility)
  - FEC level-KPIs utilizing system requirements (bit and frame error rate, throughput, latency, energy efficiency, area efficiency, and power density)

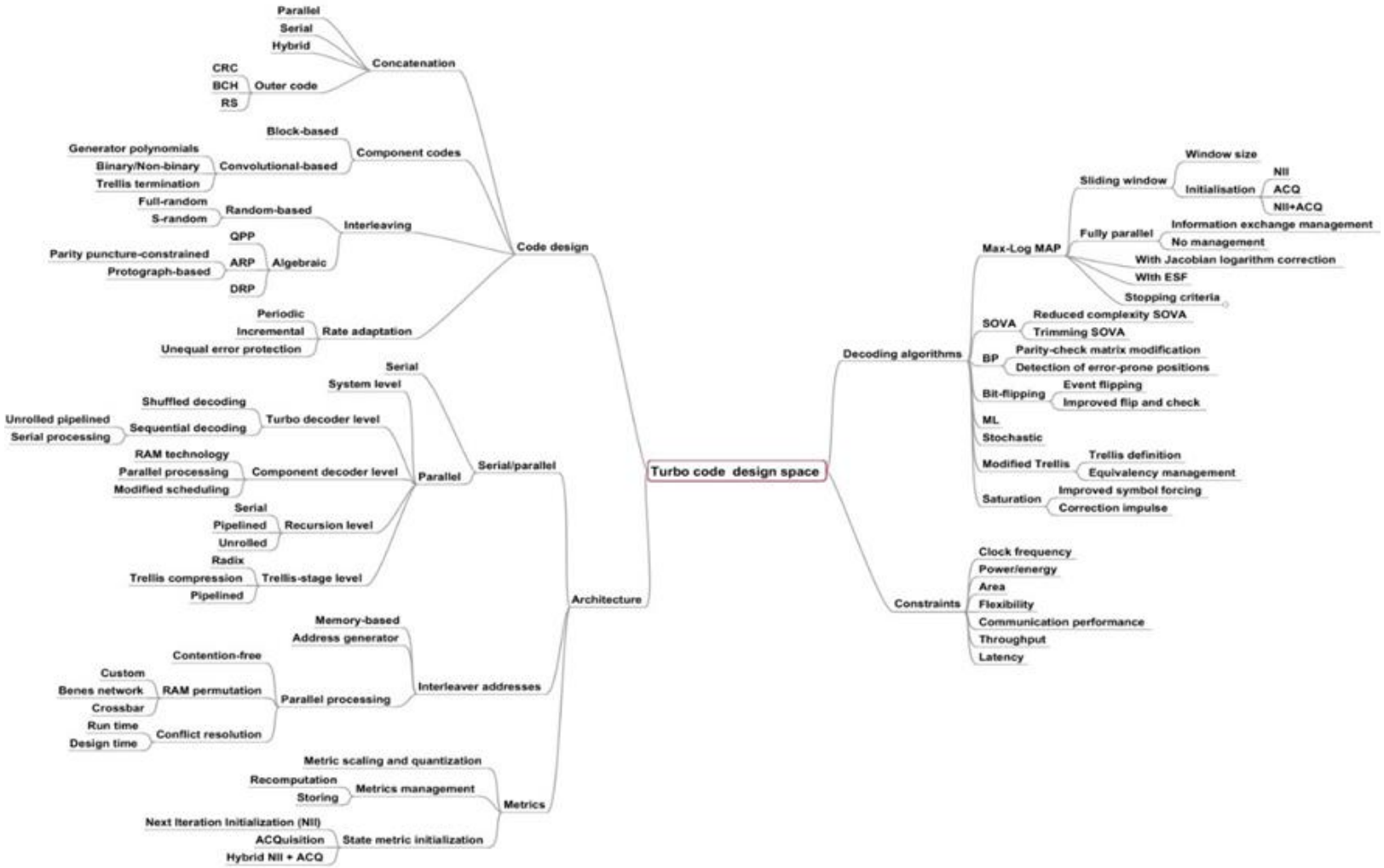
| | BER | Flexibility | Latency | Throughput [Gbps] |
|---|---|---|---|---|
| **Virtual reality** | 10^-6 | high | 0.5ms | 500,00 |
| **Data kiosk** | 10^-12 | low | 0.5ms | 1000,00 |
| **Backhaul** | 10^-8 | medium | 100ns | 250,00 |
| **Intra-device com.** | 10^-12 | low | 100ns | 500,00 |
| **Fronthaul** | 10^-12 | medium | 25ns | 1000,00 |
| **Data center** | 10^-12 ~ 10^-15 | medium | 100ns | 1000,00 |
| **Hybrid wireless fiber** | 10^-12 | medium | 200ns | 1000,00 |
| **High speed satellite** | 10^-10 | medium | max ~10ms | 100-1000 |

# EPIC FEC Implementation KPI Bounds – Broad strokes

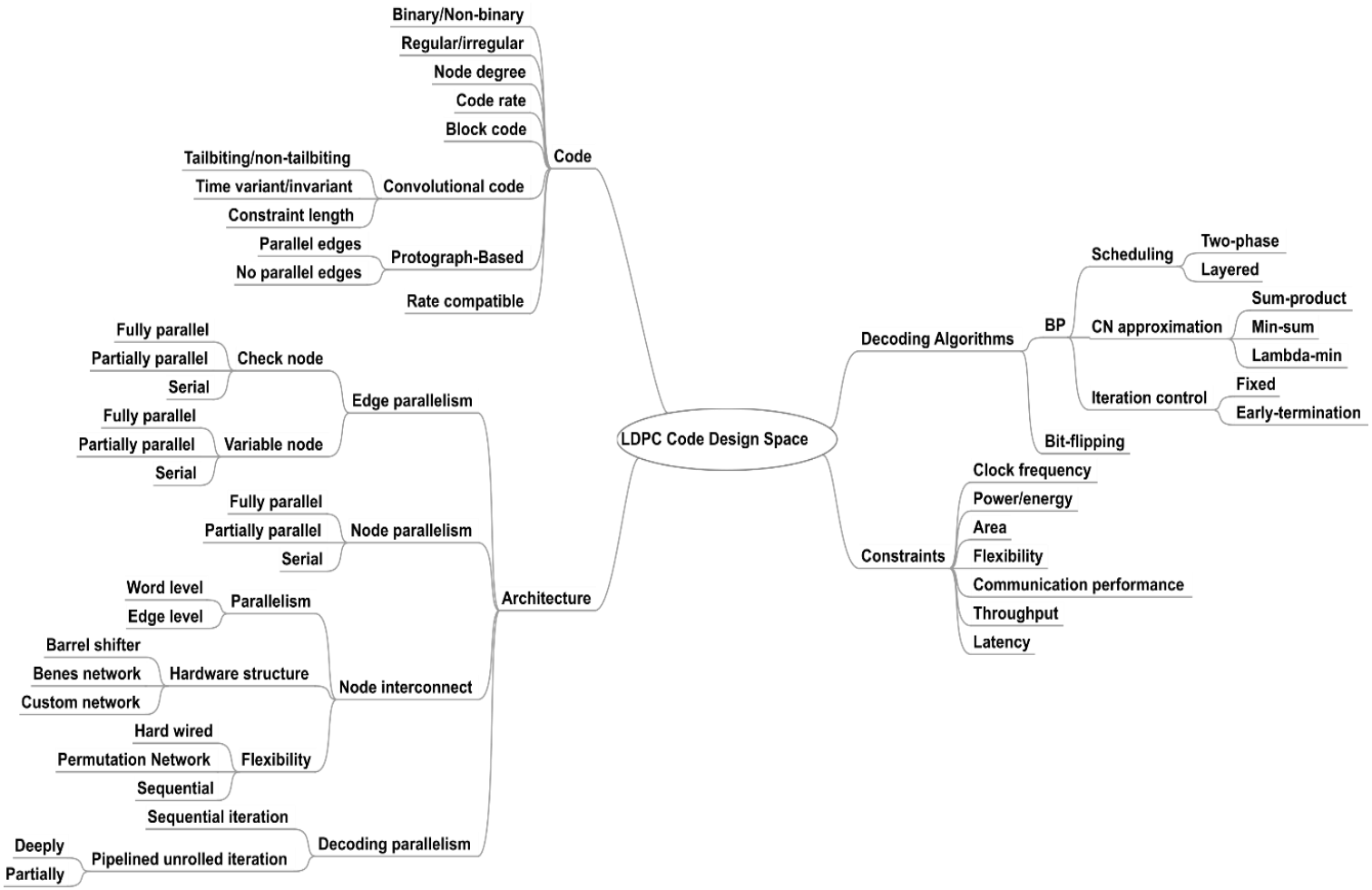
- Practical FEC chip **area constraint** on a SoC: ~10 $mm^2$
- FEC chip **power budget** to avoid heat removal issues: ~1 W
- FEC decoder **throughput**: 1 Tbps
- Detailed FEC KPI requirements in public report: D1.2 B5G Wireless Tb/s FEC KPI Requirements and Technology Gap Analysis (available at https://epic-h2020.eu/)

| **EPIC FEC KPI bounds** | |
|---|---|
| Area limit | 10 $mm^2$ |
| Area efficiency limit | 100 Gb/s/ $mm^2$ |
| Energy efficiency limit | ~1 pJ/bit |
| Power density limit | 0.1 W/$mm^2$ |

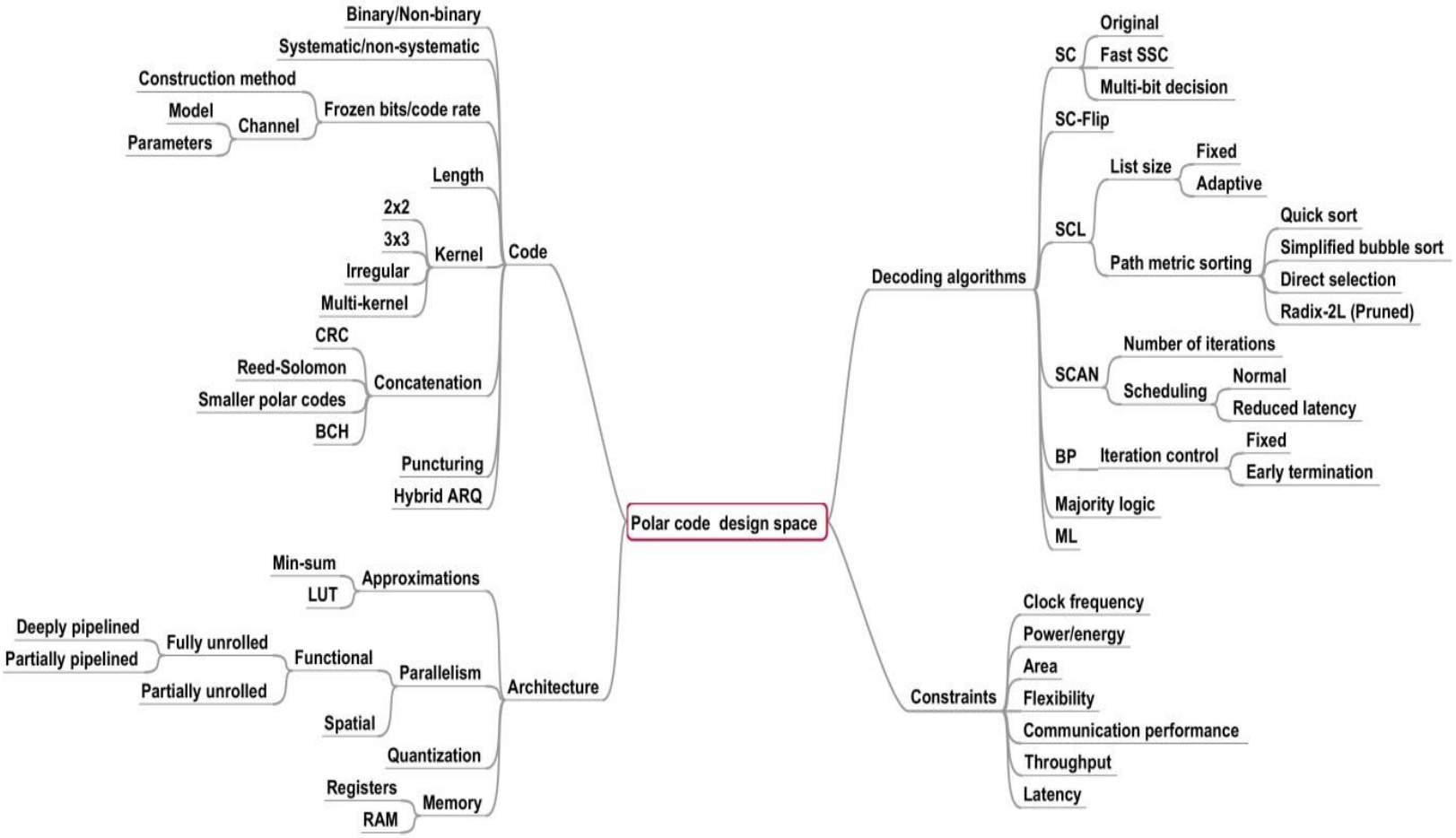
# Design Space Turbo-Codes



# Design Space LDPC Codes



# Design Space Polar Codes



# Current Status and Future Work

- EPIC project has explored various THz/Tbps B5G use-cases, and derived their system&FEC-level KPIs.
- EPIC architecture-aware FEC design framework is developed.
- Active design and implementation study of B5G FEC technology.
- Project progress and reports are available at: https://epic-h2020.eu/.

# General Project Information

- Project reference: **760150**
- Project start: **1st September 2017**
- Duration: **3 years**
- Total costs/EC contribution: **EUR 2.966.268,75**
- **Eight partners** from **seven** different **European countries:**
  - Creonic Gmbh , Ericsson AB, IMEC, Institut Mines-Telecom, InterDigital Europe, Polaran, Technikon, Technische Universitaet Kaiserslautern
- **Mission:** EPIC aims to develop a new generation of Forward-Error-Correction (FEC) codes in a manner that will serve as a fundamental enabler of practicable beyond 5G wireless Tb/s solutions and also to develop and utilize a disruptive FEC design framework allowing to advance state-of-the-art FEC schemes.
- Website: www.epic-h2020.eu
- Twitter: Epic760150; Linkedin: https://www.linkedin.com/in/epic-project-184362150

# EPIC Grant Agreement No. 760150

"The EPIC project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 760150."

If you need further information, please contact the coordinator:

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Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding