Project: IEEE P802.15 Working Group for Wireless Speciality Networks (WSNs)

Submission Title: Semiconductor technologies for THz Communications Date Submitted: 7 May 2018 Source: André Bourdoux, IMEC Address Kapeldreef 75, 3001 Leuven, Belgium E-Mail: bourdoux@imec.be

Re: n/a

Abstract: The implementation of circuits at frequencies above 100GHz poses significant challenges. Many circuits have been proposed using either heterogenous bipolar transistors (HBT) or high electron mobility transistors (HEMT) in III-V compound material. However, when price is an issue and large digital circuits are needed, CMOS technologies are preferred but they perform poorly at frequencies well above 100GHz. This presentation describes the capabilities of these technologies and discusses several approaches to reach high power at RF together with large digital circuits.

Purpose: Information for the IG THz

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Semiconductor technologies for THz Communications

Date: 2018-05-07

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		Leuven, Belgium		

Abstract

The implementation of circuits at frequencies above 100GHz poses significant challenges. Many circuits have been proposed using either heterogenous bipolar transistors (HBT) or high electron mobility transistors (HEMT) in III-V compound material. These are performant but specialty expensive implementations.

When price is an issue and large digital circuits are needed, CMOS technologies are preferred. They, however, perform poorly at frequencies well above 100GHz.

This presentation describes the capabilities of these technologies and discusses several approaches to reach high power at RF together with large digital circuits.

Outline

Application needs

The active device scene

Circuits >100GHz implemented in bulk CMOS

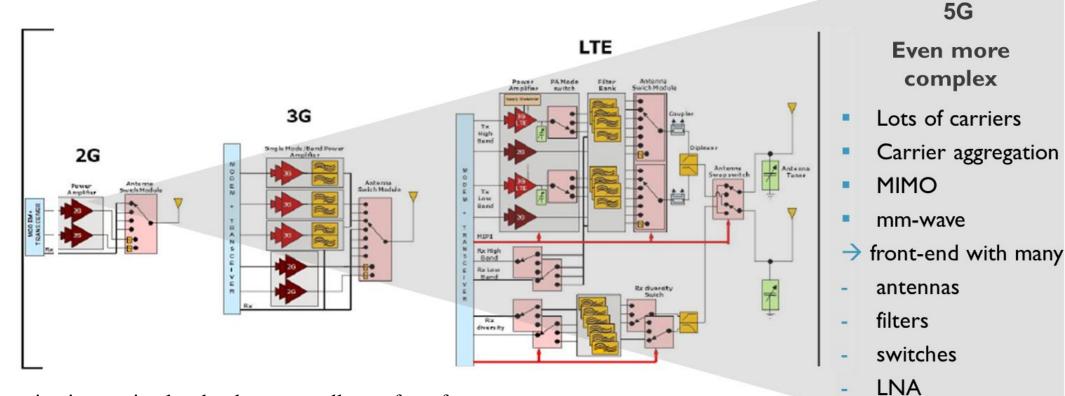
Conclusions

Application needs

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PA

5G: increasing complexity for the RF front-end Going to mm-wave

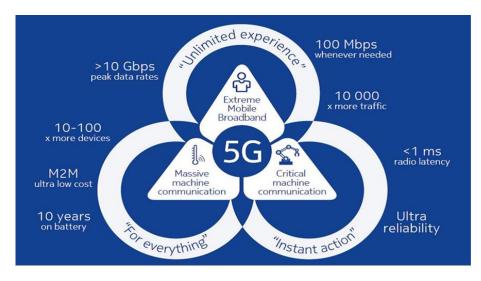


Increasing integration level reduces overall cost, form factor, power:

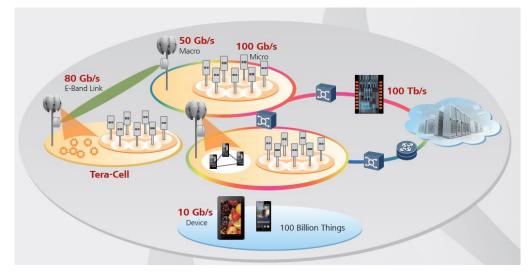
- combination of power amplifier with its controlling circuitry
- bringing as much as possible into one IC or module (3D integration)

Wireless communication: 5G and beyond

Source: Nokia



Source: Huawei, 5G: A Technology vision



- 5G will provide a total solution for a wide range of requirements Contains existing sub-6 GHz bands of 4G and new bands at mm-wave up to 90GHz Increased back- and fronthauling requirements towards 100s Gb/s
- 6G: wireless data rates > 100 Gb/s

Carrier frequencies > 100 GHz : optical & wireless communication will meet See e.g.

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European projects in ICT-09 cluster: operation > 90 GHz, up to 1Tb/s IEEE802.15.3d
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doc.: IEEE 802.15-18/0191-00-0thz

Stereo camera <Detection Image> Detection via millimeter radar and stereo camera of front rear and pedestrian. Front Pedestrian detection Front side Earth sensing Astronomy e.g. microwave backgroud Medical Biotech .g. tumor or caries . genetic & prol THz imaging & sensing Industrial Security e.g. package e.g. drug & orocess contin Source: P. de Maagt et al.,

Sensing: mm-wave offers several advantages Radar:

Range resolution = $c/(2*bandwidth) \rightarrow$ larger bandwidth easier to realize at higher frequencies

Better resolution of velocity and angle with smaller wavelength

Automotive radar 76-81 GHz: maturing market using Si technologies

BiCMOS and single-chip CMOS

Future >100 GHz ?

Smart home/office/building/city, e-health, ... : numerous applications from sub-10 GHz to >100GHz, potentially large market, pressure on form factor, power consumption

Mm-wave imaging

Spectroscopy

•••

Key requirements for >100GHz implementations

Efficient circuits @ frequency > 100GHz:

PA: high output power for link budget (range) VCO/PLL: low phase noise for good EVM (spectral efficiency)

Highly integrated solution including

RF

Digital (digital calibration, PHY processing) Memory

Relatively large volumes

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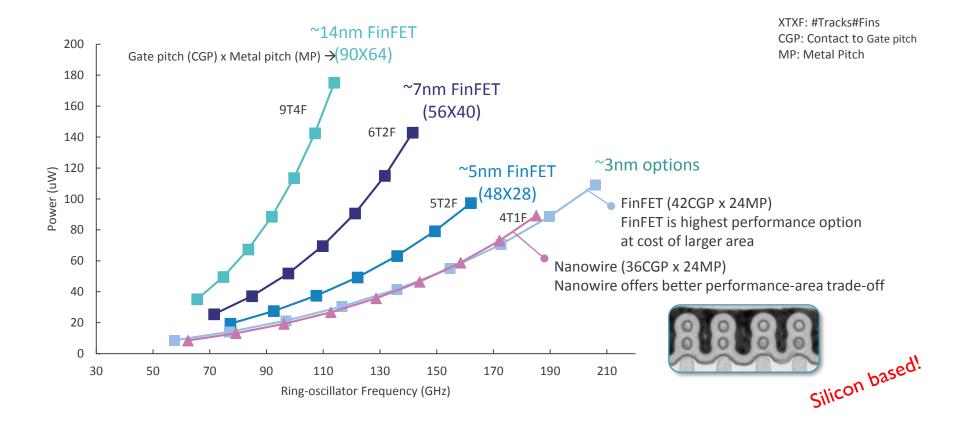
CMOS ?

CMOS?

CMOS ?

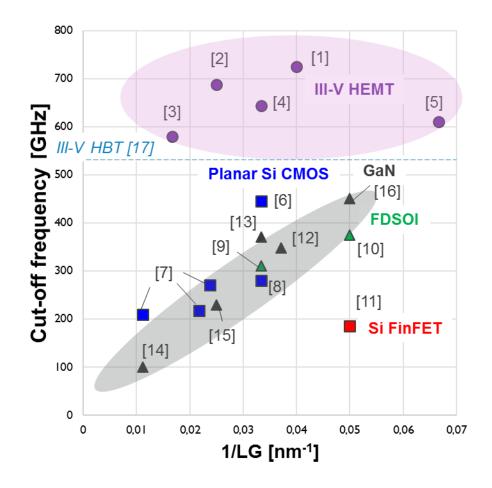
The active device scene

Evolution for logic f_T of Si-based FETs will not increase (much) with further scaling



May 2018

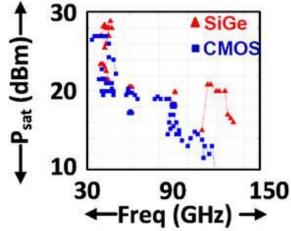
High-speed applications need fast device with good power handling capabilities ... which can be combined with CMOS



- CMOS cannot do it alone anymore
- **f**_T of Si-based FETs will not increase (much) with further scaling
- FinFET delivers intrinsically lower speed than planar
- III-V HEMT offers >500GHz f_T at relaxed gate length
- GaN similar to planar bulk but stronger driving capabilities

SiGe HBT beating CMOS in speed/power handling

1. Superiority evidenced by published designs



2. Long-term predictions for SiGe

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 11, NOVEMBER

Physical and Electrical Performance Limits of High-Speed SiGeC HBTs—Part I: Vertical Scaling

Michael Schröter, Senior Member, IEEE, Gerald Wedel, Bernd Heinemann. Christoph Jungemann, Senior Member, IEEE, Julia Krause, Pascal Chevalier, Member, IEEE, and Alain Chantre, Senior Member, IEEE

cuses on the vertically scaled structure. According to isothermal device simulation, the "ultimate" doning profile yields a neak transit frequency f_T of almost 1.5 THz a BV_{CEO} above 1 V (dependent on BE bias) and a zero-bias internal base sheet resistance of about 3 k Ω /sq. The reasons for achieving a higher product $f_T BV_{CEO}$ (> 1.5 THzV) than anticipated from the classical Johnson limit are explained. Finally, it is found that f_T is Submission

doc.: IEEE 802.15-18/0191-00-0thz 3. SiGe technology developments SiGe HBT with f_T/f_{max} of 505 GHz/720 GHz

B. Heinemann, H. Rücker, R. Barth, F. Bärwolf, J. Drews, G. G. Fischer, A. Fox, O. Fursenko, T. Grabolla, F. Herzel, J. Katzer, J. Korn, A. Krüger, P. Kulse, T. Lenke, M. Lisker, S. Marschmeyer, A. Scheit, D. Schmidt, J. Schmidt, M. A. Schubert, A. Trusch, C. Wipf, and D. Wolansky

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Project details

Total cost:	Topic(s):			
EUR 43 025 971,22	ECSEL-2016-1 - ECSEL Key Applications and Essential technologies (RIA)			
EU contribution:	Call for proposal:			
EUR 12 081 281,89	H2020-ECSEL-2016-1-RIA-two-stage See other projects for this call			
Coordinated in:	Funding scheme:			
France	ECSEL-RIA - ECSEL Research and Innovation Action			

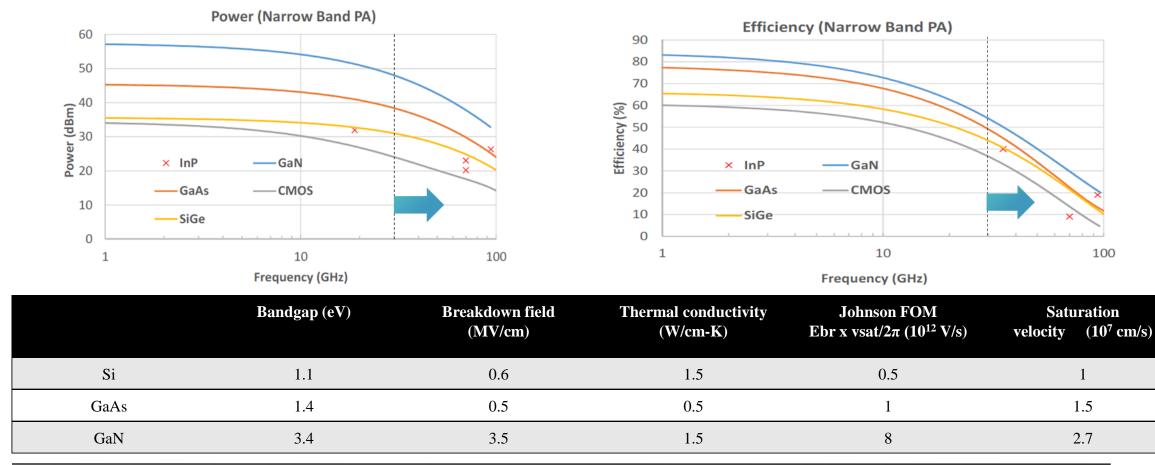
Objective

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The TARANTO project targets to break the technological barriers to the development of the next BiCMOS technology platforms, allowing the improvement of the performance of the HBT (Heterojunction Bipolar Transistors) with a much higher level of integration. This new generation of transistors HBT will be a key factor to meet the needs of high-speed communications systems and high data rate required for the integration of heterogeneous intelligent systems as well as for intell.

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GaN and GaAs devices yield high output power and efficiency at high frequencies The trend continues @ >100GHz



Submission

All-silicon versus III-V co-integration

FinFET \rightarrow **lateral nanowires**

Best for complex logic Speed limited by 3D parasitics Poor driving capabilities

BiCMOS

Logic usually lags few generations behind Compatible with FD-SOI [ST Microelectronics, BJT + 28nm FD-SOI, BCTM 2016] Stronger driving capabilities than FinFET Highest f_T of silicon devices $f_T > I$ THz possible at $BV_{CEO} > IV$

RF-SOI

Higher f_T than FinFET Body bias is extra feature Allows for device stacking in PAs Switches with very low Ron*Coff

III-V

Higher f_T than Si possible Better power handling Growth on 300mm Si complex but feasible

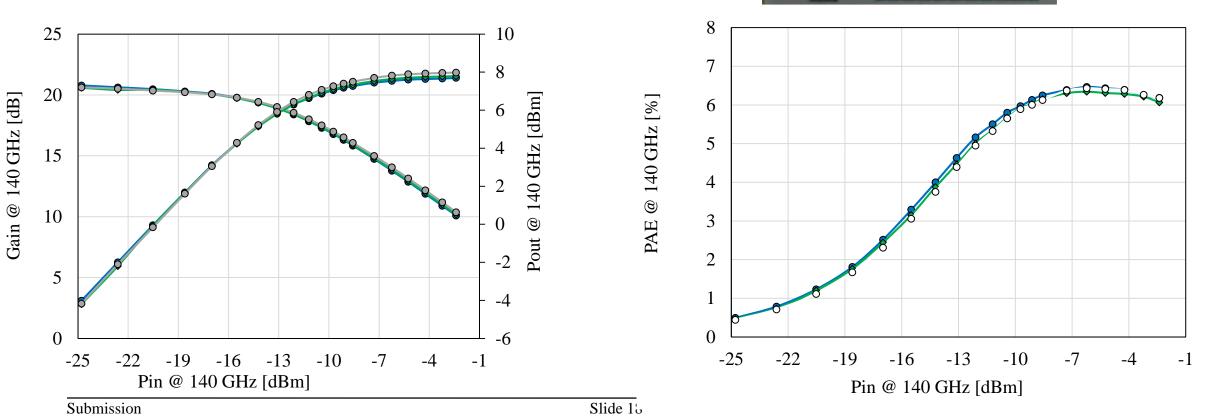
> several research groups in the world are considering cointegration of III-V materials on silicon

Submission

Circuits >100GHz implemented in bulk CMOS

140GHz PA in bulk CMOS

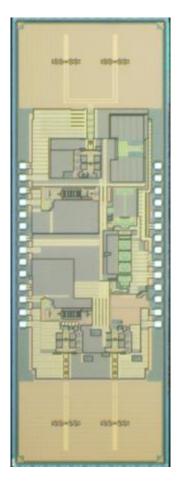
- 28 nm HPM
- V_{DD} = 0.9 V
- PA area = 0.11 mm²
- PA Pdc = 81 mW

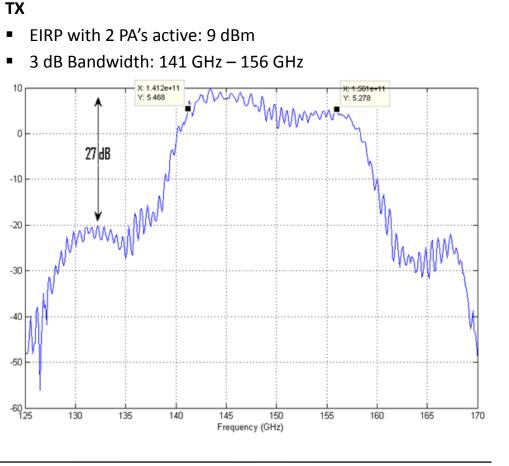


0.367

<u>91-00-0thz</u>

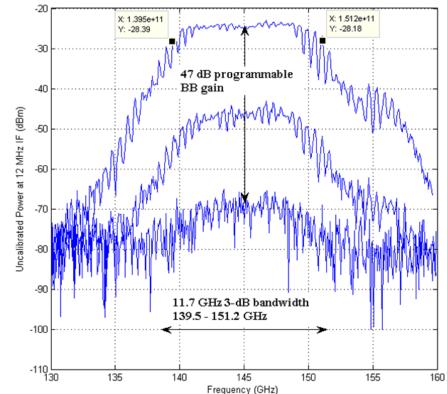
140GHz FMCW radar in bulk CMOS with on-chip antennas





RX

- 47 dB programmable Baseband gain
- 3 dB RF Bandwidth:
 139.5 GHz 151.2 GHz
- 3 dB baseband Bandwidth: 750 kHz – 18 MHz





Conclusions

May 2018

- Need for high(er) speed and high power at a small factor Higher degree of integration, packaging challenges
- Scaling roadmap slowing down, CMOS not going faster anymore
- Will market embrace other devices co-integrated with CMOS?

Or will design tricks in CMOS and digital compensation techniques rule out non-CMOS?

Which device will win? SiGe HBT, III-V HBT, HEMT, MOSFET, ...?

300 mm wafers are a must

Affordable?

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Ga-N

In-P

What are III-V semiconductors?

