**IEEE P802.15**

**Wireless Personal Area Networks**

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| Project | IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs) |
| Title | **D4 Comments Resolution Based Offset-VPWM PHY/MAC Specification**  |
| Date Submitted | September, 2017 |
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| Re: | Draft D4 Comment Resolution based Offset-VPWM PHY/MAC Specification  |
| Abstract | Details of Resolutions regarding to the submitted Comments on D4 are suggested for Offset-VPWM PHY/MAC Specification Revision. The PHY IV Offset-VPWM is designed to operate on the application services like LED ID, LiFi/CamCom, Digital Signage with Advertisement Information etc. |
| Purpose | Draft D4 Comments Resolutions and Editorial Revision. |
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# **1. PHY IV SUPERFRAME STRUCTURE**

# **4.8 Some access mechanism by PHY types**

# The UFSOOK, Twinkle VPPM, Offset-VPWM, MPM, VTASC, SS2DC, and IDE transmitter schemes use unslotted ALOHA; that is, when the transmitter has a packet to send, it just sends it. There is no beacon and the transmitter does not do a listen before talk channel activity check. The superframe structure Figure 19 consists of only the contention access period (see subclause 5.1.1.1.2).

# **2. PHY IV DIMMING**

**8.5.2.4.2 Offset-VPWM dimming**

Offset VPWM causes flicker and dimming is not supported.

# **3. PHY IV PPTU Format**

**8.6.1.2.2 Offset-VPWM Preamble Field**

The preamble field is used by the transceiver to obtain optical clock synchronization with an incoming message. The standard defines one fast locking pattern (FLP). The MAC shall select the optical clock rate for communication during the clock rate selection process. The preamble shall be sent at a clock rate chosen by the transmitter and supported by the receiver. The preamble is a time domain sequence and does not have any channel coding or line coding.

The preamble first starts with a FLP. The FLP is fixed as a pattern “11010010”. The fast locking pattern length shall not exceed the maximum. The timing information for preamble is shown in Figure 132.



**Figure 132 – Preamble Timing Diagram**

In the Offset-VPWM for smart device flash light PHY uses OOK modulation for preamble transmission using flash light. The preamble bit mapping shown in Figure 133.



**Figure 133 – Preamble Transmission – OFFSET VPWM BIT MAPPING**

**8.6.5.2.2 Offset-VPWM PSDU field**

The Offset-VPWM PSDU field has a variable length and carries the arbitrary number of payload bits. The end of the PSDU field is indicated by the presences of another SFD, which means that preamble frame.

# **4. PHY SPECIFICATIONS**

**13.5 Offset-VPWM**

The Offset-VPWM supported data rates and operating conditions are shown in PHY IV operating modes Table 81.

**13.5.1 Reference Architecture**

A reference implementation of the Offset-VPWM modulator is shown in Figure OffsetVPWMNEW.



Figure OffsetVPWM – Offset-VPWM Block Diagram

**13.5.2 OFFSET-VPWM PHY Encoder**

The offset-VPWM encoder is built-in with line coding and encoded with thesum (P + nV)of the unit to be added to the minimum pulse (P) which is a reference pulse width (V) as a Symbol ( P > V, V > time error (jitter) ). The Offset-VPWM specify a 2bit data symbol, 4bit data symbol according to number of added pulse.

The data symbol map for two bits symbol with pulse width and respective symbol blinking waveform are shown in Table 137 and Figure 186 respectively.

**Table 137 – Two Bits Symbol Mapping Truth Table**

|  |  |
| --- | --- |
| **Data Bits** | **Pulse Width** |
| 00 | P + 0V |
| 01 | P + 1V |
| 10 | P + 2V |
| 11 | P + 3V |

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**Figure 186 – Two Bit Symbol Data Diagram**

In offset-VPWM, the data is expressed with offset pulse width, 4bits data (for example) were mapped into 16 Offset-VPWM symbols. The 4 bits symbol mapping truth table is shown in Table 138.

|  |  |
| --- | --- |
| **Data Bits** | **Pulse Width** |
| 0000 | P+0V |
| 0001 | P+1V |
| 0010 | P+2V |
| 0011 | P+3V |
| 0100 | P+4V |
| 0101 | P+5V |
| 0110 | P+6V |
| 0111 | P+7V |
| 1000 | P+8V |
| 1001 | P+9V |
| 1010 | P+10V |
| 1011 | P+11V |
| 1100 | P+12V |
| 1101 | P+13V |
| 1110 | P+14V |
| 1111 | P+15V |

 **Table 138 – Four Bits Symbol Mapping Truth Table**

The symbol arrays mapping is described in waveform pattern as shown in Figure 187.



**Figure 187 – Symbol Array Mapping Timing Diagram**

The optimum value of P is 40 msec and V is vary from 10~50 % of P. The default V is 50% of P. The P and V are configurable over PHY attributes phyOffsetVPWMStdPERIOD, phyOffsetVPWMOffsetPERIOD respectively.

# **5. PHY IV MAC PROTOCOL SPECIFICATIONS**

**5.2.1.8 Frame Payload field**

**5.2.1.8.2 PHY IV**

**Offset-VPWM Frame Payload Field**

The Frame Payload field has a variable length and contains information specific to individual frame types. The offset-VPWM uses only the frame payload. If the PHY attribute phyOccFEC is set to FCS mode in the frame control field then the frame payload is protected as defined by the security suite selected for that frame.

**5.2.1.9 FCS Field**

**5.2.1.9.2 PHY IV**

**Offset-VPWM FCS Field**

The FCS is calculated over the MHR and MSDU parts of the frame. The FCS shall be only generated for payloads greater than zero bytes. The FCS is an optional and is given in Annex C. The FCS is configured through PHY attribute phyOccFEC*.*

**6. RECEIVER DECODING FOR OFFSET-VPWM**

**Annex J (Informative)**

**J.8 Offset-VPWM Decoding Method**

The receiver camera that has frame rate same as the optical clock rate shall be used to receive data i.e. 25 fps. To decode the data symbol, the smart device capture the visual frame using rolling-shutter mode. The offset-VPWM symbol is decoded with three consecutive frame and receiver can synchronize rising edge and check pulse width length for each symbols decoding.

The pulse width duration is calculated using PHY attributes phyOffsetVPWMStdPERIOD, phyOffsetVPWMOffsetPERIOD. The total pulse width duration is (phyOffsetVPWMStdPERIOD + phyOffsetVPWMOffsetPERIOD +/- 5% of phyOffsetVPWMStdPERIOD).

The receiver detection process in the wave formatted approach is show in Figure J.12.



**Figure J.12 – Receiver Detection Process**