**IEEE P802.15**

**Wireless Personal Area Networks**

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# #3: PPDU frame formats

## **8.6.1 Preamble field**

**8.6.1.4 PHY VI**

### 8.6.1.4.2 A-QL preamble field

The preamble field for A-QL is within a data-block time long. The preamble sequence (1010..10) shall have 64 bits length. The remainder of a block carrying the preamble is for PHR subfields and the training sequence (see Figure X).



Figure X. Preamble sequence, PHR subfields and training sequence of A-QL

### 8.6.1.4.3 Hidden A-QL (HA-QL) preamble field

The preamble field for HA-QL is one data-block time long (equivalent to two optical clock times), consisting of two blocks. The second block is the inverse form of the first block.

The preamble sequence (1010…10) along with four states of reference cells have 64 bit-length, and fill up a block of HA-QL code (e.g. 8x8 HA-QL block) as shown in Figure Y.



Figure Y. HA-QL Preamble

Deleted S8-PSK preamble

## **8.6.2 PHY header**

### 8.6.2.2 PHY IV

#### 8.6.2.2.1 S8-PSK PHY header (deleted)

#### 8.6.2.2.2 HS-PSK PHY header

PHY header subfields shall be mandatory configured by PHY PIB attributes. Besides, PHR field shall be optionally used to notice the change of the following PHY header subfields:

**Table – HS-PSK PHR subfields**

|  |  |  |
| --- | --- | --- |
| **PHY header subfields** | **Bit-width** | **Explanation on usage** |
| PSDU length | 16 | Length available at *phyHSpskPsduLength* configuration |
| HSC | 16 | Header check sequence |

### 8.6.2.3 PHY V

#### 8.6.2.3.2 CM-FSK PHY header

Not used

#### 8.6.2.3.3 C-OOK PHY header

Not used

### 8.6.2.4 PHY VI

#### 8.6.2.4.2 A-QL PHY header

PHY header subfields shall be mandatory configured by PHY PIB attributes. Besides, PHR field shall be optionally used to notice the change of the following PHY header subfields:

**Table – A-QL PHR subfields**

|  |  |  |
| --- | --- | --- |
| **PHY header subfields** | **Bit-width** | **Explanation on usage** |
| PSDU length | 16 | Length available at *phyAqlPsduLength* configuration |
| HSC | 16 | Header check sequence |

#### 8.6.2.4.3 HA-QL PHY header

Not used.

## **8.6.3 Header check sequence (HCS)**

### 8.6.3.2 PHY IV

#### 8.6.3.2.1 HS-PSK HSC

CRC-16 shall be used as HSC. The generation of CRC-16 (with polynomial generator 0x1021) is described in Annex C.

### 8.6.3.3 PHY V (not use)

**Deleted all these subsections.**

Not used

### 8.6.3.4 PHY VI

#### 8.6.3.4.1 A-QL HSC

CRC-16 shall be used as HSC. The generation of CRC-16 (with polynomial generator 0x1021) is described in Annex C.

#### 8.6.3.4.1 Hidden A-QL HSC (deleted)

## **8.6.4 Optional fields**

### 8.6.4.4 PHY VI

#### 8.6.4.4.1 A-QL optional field

A channel estimation sequence shall be added as an extended subfield after the PHR subfields to support a receiver dealing with multi-color imbalance or multi-color interference. The channel estimation sequence details are discussed in section “**15.1.4 A-QL Color calibration at the receiver**.”

## **8.6.5 PSDU field**

### 8.6.5.2 PHY IV

#### 8.6.5.2.4 S8-PSK PSDU field (delete this)

### 8.6.5.3 PHY V

#### 8.6.5.3.5 C-OOK PSDU field

The C-OOK PSDU consists of multiple data sub-packets (denoted as DS). Each sub-packet DS consists of its own preamble (DS preamble) and its payload carrying asynchronous bits (front Ab and rear Ab) and data bits. The DS payload may be encoded by the choice of inner FEC that is configurable by PHY PIB *phyOccFec*.

**Table 102- PSDU frame format**

|  |
| --- |
| PSDU |
| Sub-packet 1 | Sub-packet 2 | … | Sub-packet N |

 **Table 103- Sub-packet**

|  |  |
| --- | --- |
| **Preamble** | **DS payload** |
| **Ab (front)** | **data bits** | **Ab (rear)** |

There are four different PSDU frames supporting four PHY modes as follows. Among them, mode 1 and

mode 2 are operating at 2.2 kHz optical clock rate, whereas mode 3 and mode 4 are operating at 4.4 kHz

optical clock rate.

**Table 104– SubPacket Structure specification**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Mode 1** | **Mode 2** | **Mode 3** | **Mode 4** |
| DS clocks | 22B | 37B | 74B | 74B |
| Preamble  | 6B | 10B | 6B | 10B |
| DS payload (Ab, data bits, Ab)  |  (16B)8 bits | 18 bits (27B) | 33 bits(66B, 2B unused) | 40 bits(60B, 4B unused) |

### 8.6.5.4 PHY VI

#### 8.6.5.4.1 A-QL PSDU field

The count of payload blocks in PSDU (N) is calculated from the PSDU length read from the PHY header.

**Table 105—A-QL PSDU frame format**

|  |
| --- |
| PSDU |
| Data block 1 | Data block 2 | … | Data block N |

The block interval is specified at longer than the maximum interframe interval of camera sampling to make sure that every symbol is sampled at least once. The configuration of block interval is implemented by the PHY PIB *phyOccOpticalClockRate*.

The number of cells on the transmitter M×M is configurable by the PHY PIB *phyAqlNoCells*. At the four corners of the transmitter, the intensity of reference cells (the number of reference cells is configured via PHY PIB *phyAqlNoCellReference*) does not change when updating data to support the decoding under rotation (see **15.1 A-QL specification**). Thus, each data block shall carry (M×M – number\_reference\_cells) bits per color band, including Ab bits and data bits. When three color-bands (i, j, k) are used, the bit count carried by a block is triple.

#### 8.6.5.4.3 Hidden A-QL (HA-QL) PSDU field

PSDU consists of a number of data blocks (N) that is counted from a preamble to the next preamble.

**Table 105—HA-QL PSDU frame format**

|  |
| --- |
| PSDU |
| Data block 1 | Data block 2 | … | Data block N |

The block interval is specified at longer than the maximum interframe interval of camera sampling to make sure that every symbol is sampled at least once. The configuration of block interval is implemented by the PHY PIB *phyOccOpticalClockRate*.

Also, the data block utilizes 1/2-rate line coding. The optical clock rate is usually specified at 10Hz and

therefore, the block rate is at 5Hz to support 30fps camera receiver that has time-variant frame rate.

The number of cells on the transmitter m×n, including four reference cells at the four corners of Tx and the other data cells, is configurable by the PHY PIB *phyHaqlNoCells*. Thus, each data block shall carry (m×n – 4) bits per block, including Ab bits and data bits.