**IEEE P802.15**

**Wireless Personal Area Networks**

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| Project | IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs) |
| Title | **Kookmin D1 Text Revision updating to PHY PIBs** |
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| Source | Trang Nguyen, and Yeong Min Jang (Kookmin University) |
| Re: |  |
| Abstract | D1 PHY 4, 5, 6 specifications are revised according to PHY PIB attributes. |
| Purpose | D1 comments and resolutions |
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# #5: PHY A specifications

## **13.3 S2-PSK**

### 13.3.1 S2-PSK Encoder

**13.3.1.1 Bit-to-symbol mapping**

The configuration of modulation rate is performed over the PHY PIB attribute *phyS2pskModulationRate* that ensures being non-flicker. A lower modulation rate gains a lower probability of bad-sampling which caused by capturing at the pulse switching time. Usually, the constant value of the modulation rate is chosen at 200Hz for the indoor environment and 125Hz for the outdoor environment.

The symbol to each LED is a multiple-times repetition of a symmetric Manchester symbol (i.e. multiple times repetition of 01 or 10). After mapping, the optical clock rate (equivalent to bit rate) is configured over the PHY PIB attribute *phyOccOpticalClockRate* that being no greater than the camera frame rate (e.g. 10 Hz) to ensure every bit is sampled at least once.

**13.3.1.4 Line Coding**

The RLL coder shall be optionally implemented to protect the signal from the error caused by the rotation of camera and the error caused by the time deviation between a pair of light sources on the rolling image. The configuration of RLL coder is implemented over the PHY PIB attribute *phyOccRLLCode*.

Once the RLL code is applied, the PPDU shall utilize RLL coding at code rate 1/2 as follows.

|  |  |  |
| --- | --- | --- |
| **Duration** | **one bit time** | **one bit time** |
| Data bit | 0 | 1 |
| RLL coding | 0 0 | 0 1 |

After RLL coding, the output sequence shall be feed into S2-PSK Encoder.

### 13.3.2 S2-PSK Error Correction

**// Figure is deleted.**

The configuration of error correction for S2-PSK shall be implemented over the PHY PIB attribute *phyOccFec.*

By default, no error correction is used for S2-PSK. However, a majority bit voting shall be applied if the camera frame rate (e.g. 30fps) is higher than the optical clock rate (e.g. 10Hz), and being considered as a type of temporal error correction.

### 14.3.2 S2-PSK dimming Support

S2-PSK dimming is achieved by amplitude modulation as described in the sub-clause 4.5.3.1.5 Low-Clock-Rate OOK amplitude dimming. The benefit of amplitude dimming is that the data rate of transmission is maintained while performing dimming. In contrast, it requires hardware support.

The configuration of dimming level for S2-PSK shall be implemented over the PHY PIB attribute *phyOccDim.*

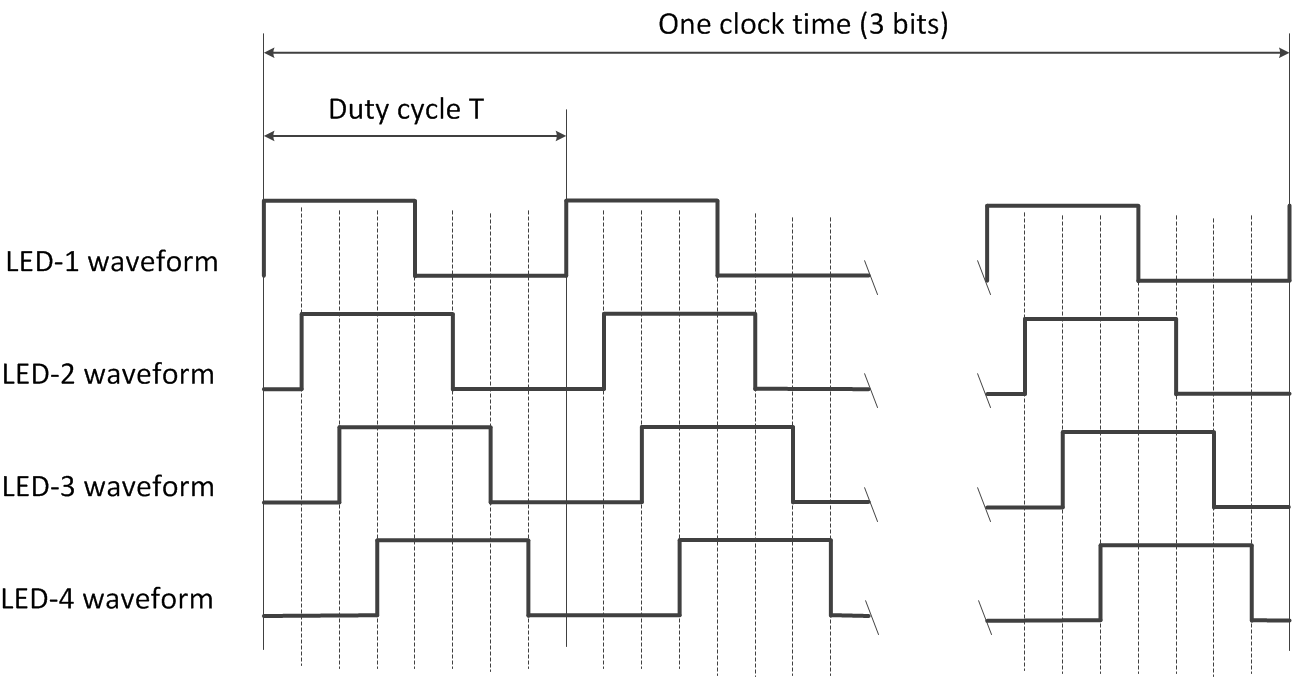
## **13.4.1.1 S8-PSK**

### 13.4.1.1.1 S8-PSK Encoder

By default, four-LEDs are grouped into a light source. However, the number of LEDs per group is configurable over the PHY PIB attribute *phyS8pskNoLightSources*.

Four square waveforms, that the (i+1)th waveform is delayed 1/8 duty cycle compared to the ith waveform (as shown in Fig. 289), are used to drive four LEDs. The modulation rate of waveform signals is configured over the PHY PIB attribute *phyS8pskModulationRate*.

The optical clock rate (i.e. the frequency at which a block of 3-bit is clocked out) shall be configured over the PHY PIB attribute *phyOccOpticalClockRate.*



**Figure 289. Waveforms to drive a group of four LEDs**

A pair of two light sources, each is a group of four-LEDs, is used to transmit 3 bits at once by controlling the shifting value (called ***S\_Phase\_Shift****)* of the phases of all waveforms between two groups. This is implemented by maintaining the phases of the waveforms of the first group at 0; T/8; 2T/8; 3T/8 respectively while shifting all the phases of the waveforms of the second group by (i ×T/8) compared to that of the first group, where i is an integer depending upon 3-bits input. The mapping from 3 bits data to the shifting value of all phases of waveforms between two light sources (value of i) is shown in table 203.

**Table 203. Mapping table from bits to S\_Phase\_Shift**

|  |  |
| --- | --- |
| 3-bits  **Input** | S\_Phase\_Shift / (T/8)  **Output** |
| 000 | 0 |
| 001 | 1 |
| 010 | 2 |
| 011 | 3 |
| 100 | 4 |
| 101 | 5 |
| 110 | 6 |
| 111 | 7 |

### 13.4.1.1.4 S8-PSK Decoder

At a time, a camera makes sampling two groups of light sources, each group generates a set of four ON/OFF states. The captured set of four-states of a group shall be represented by S\_Phase as shown in table 202. A sampling that is called bad-sampling when camera captures on the transition time of a single LED among LEDs of the group shall generate a presence of an unclear state (x\_state).

**Table 202. S\_Phase Determination**

|  |  |  |
| --- | --- | --- |
| Set of 4-States  (w/o presence x\_state)  **Input** | Set of 4-States  (w/ presence of x\_state)  **Input** | S\_Phase  **Output** |
| 1000 | 1x00 | 1 |
| 1100 | 11x0 | 2 |
| 1110 | 111x | 3 |
| 1111 | x111 | 4 |
| 0111 | 0x11 | 5 |
| 0011 | 00x1 | 6 |
| 0001 | 000x | 7 |
| 0000 | x000 | 8 |

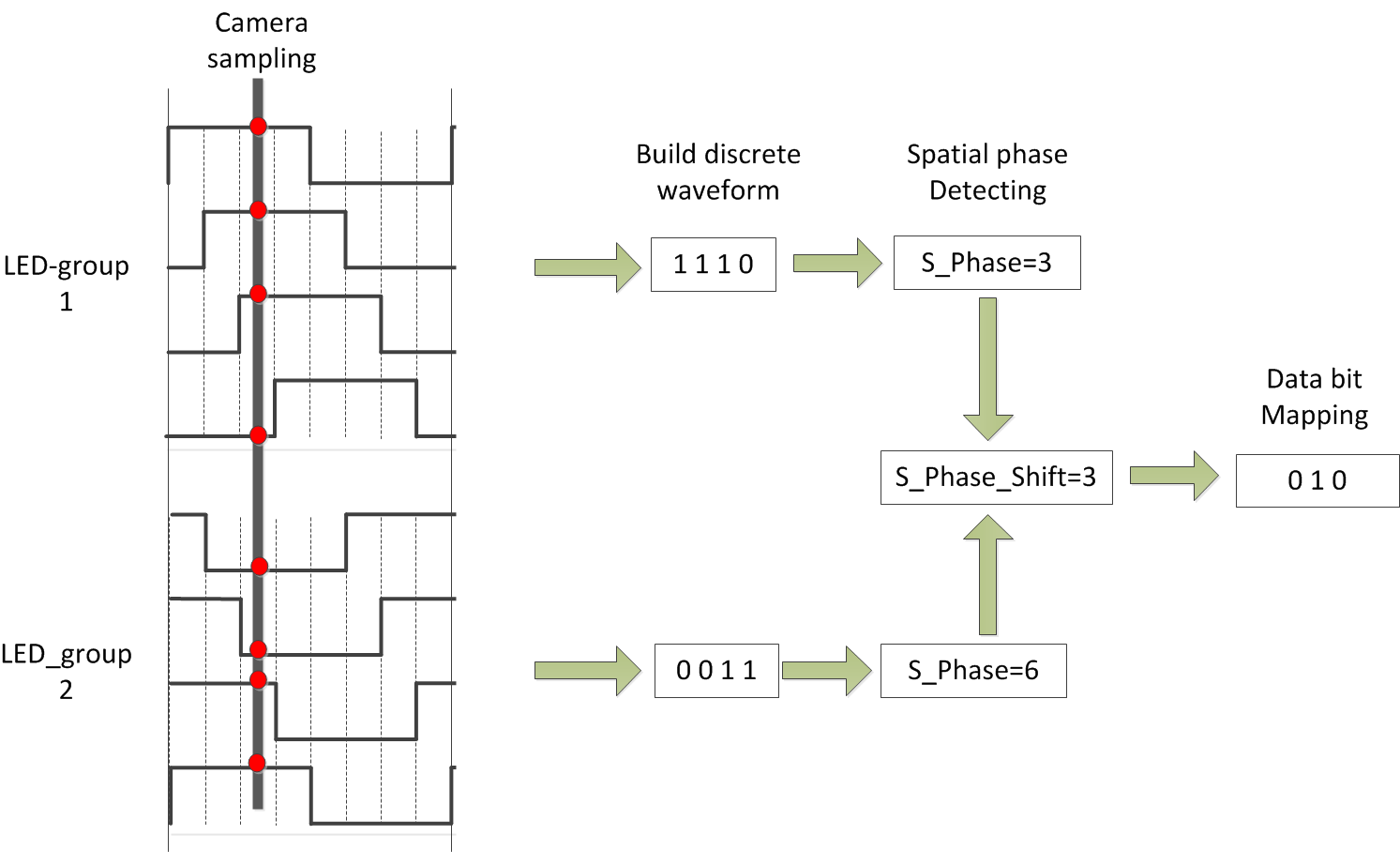
Using two sets of four-states determined from a pair of light sources, the value of ***S\_Phase\_Shift*** is determined as following:

***S\_Phase\_Shift = S\_Phase(1) - S\_Phase(2)***

where *S\_Phase(1)* represents the *S\_Phase* value determined from LED-group 1; *S\_Phase(2)* represents the *S\_Phase* value determined from LED-group 2.

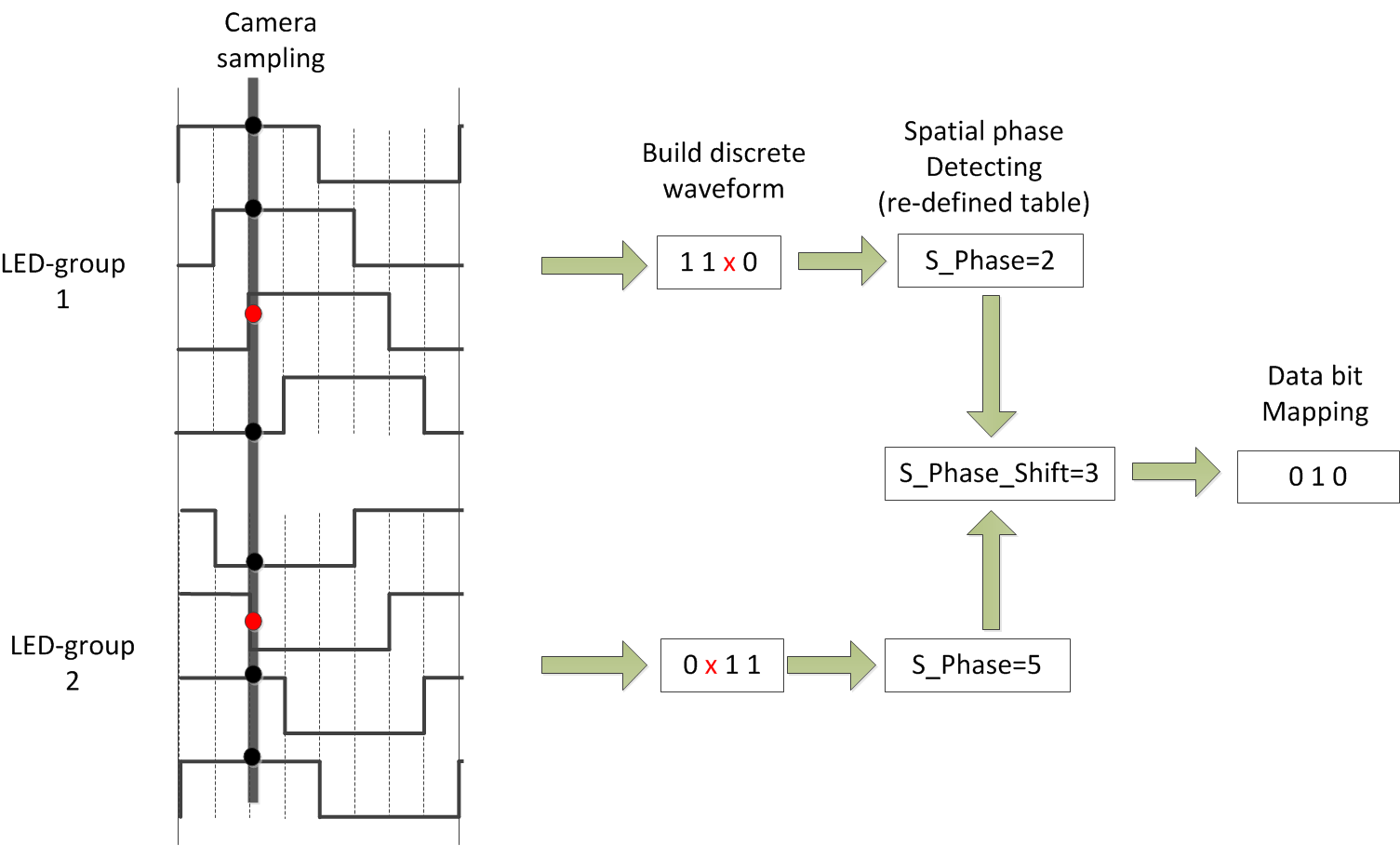
Finally, the de-mapping from S\_Phase\_Shift to 3 bits data shall be done inversely as the mapping table showed.

**Example 1:** Decoding under none-presence of bad-sampling

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**Figure 265 – An example of S8-PSK decoding**

**Example 2:** Decoding under presence of *bad-sampling*



**Figure.266. An example of S8-PSK decoding under the presence of bad-sampling**

### 13.4.1.1.4 S8-PSK Error Correction

The configuration of error correction for S8-PSK shall be implemented over the PHY PIB attribute *phyOccFec.*

By default, no error correction is used for S8-PSK. However, a majority bit voting shall be applied if the camera frame rate (e.g. 30fps) is higher than the optical clock rate (e.g. 10Hz), and being considered as a type of temporal error correction. Also, the decoding under bad-sampling condition is considered as an error correction with the code rate equals 1.

### 13.4.1.1.5 S8-PSK Dimming

S8-PSK dimming is achieved by amplitude modulation as described in the sub-clause 4.5.3.1.5 Low-Clock-Rate OOK amplitude dimming. The benefit of amplitude dimming is that the data rate is maintained while dimming is performed. In contrast, it requires hardware support.

The configuration of dimming level for S8-PSK shall be implemented over the PHY PIB attribute *phyOccDim.*

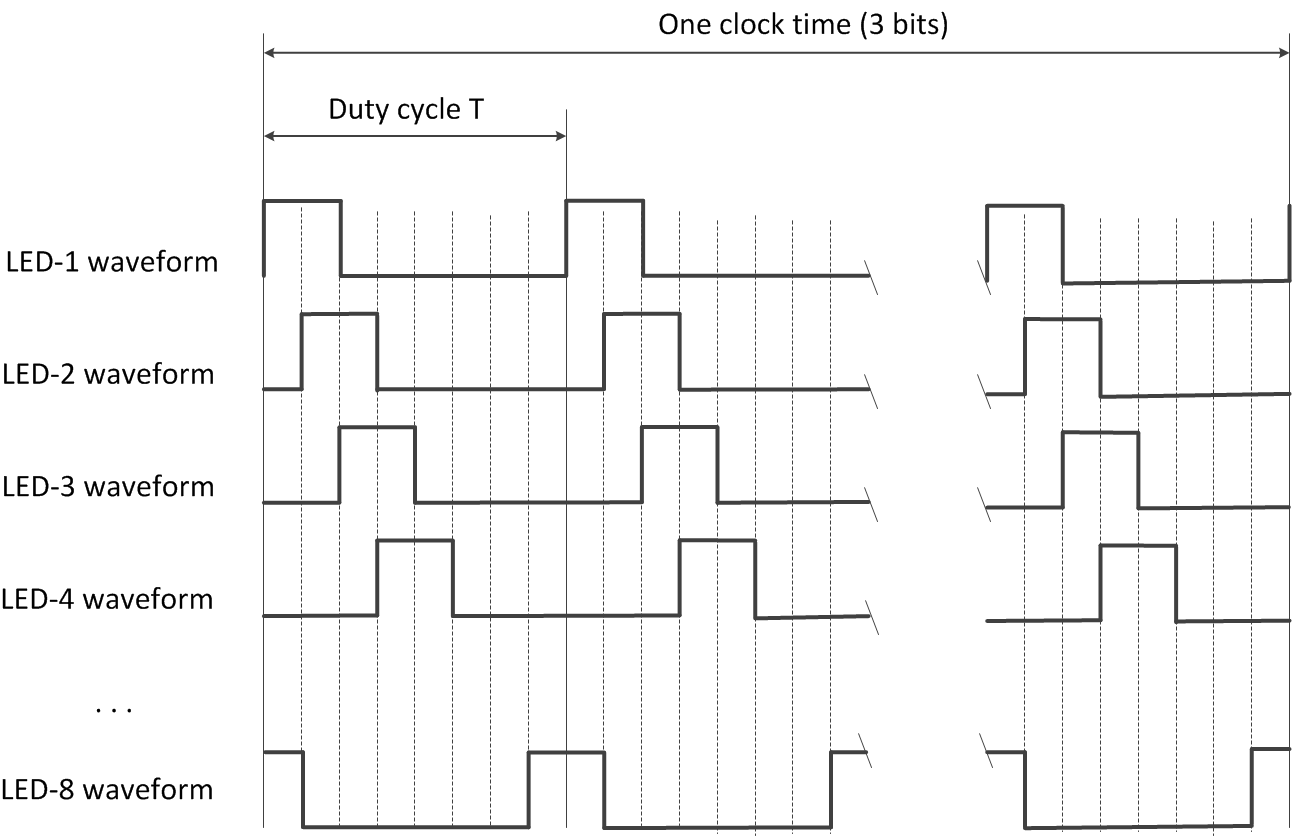
## **13.4.1.2 DS8-PSK**

### 13.4.1.2.1 DS8-PSK Encoder

By default, eight-LEDs are grouped into a light source. However, the number of LEDs per group is configurable over the PHY PIB attribute *phyHSpskNoLightSources*.

Eight rectangular waveforms, that the (i+1)th waveform is delayed 1/8 duty cycle compared to the ith waveform (as shown in Fig. 293), are used to drive the group of LEDs. The modulation rate of waveform signals is configured over the PHY PIB attribute *phyHSpskModulationRate*.

The optical clock rate (i.e. the frequency at which a block of 3-bit is clocked out) shall be configured over the PHY PIB attribute *phyOccOpticalClockRate.*



**Figure 293. Waveforms to drive a group of eight LEDs (example of 25% dimming)**

A pair of two light sources, each is a group of eight-LEDs, is used to transmit 3 bits at once by controlling the shifting value (called ***S\_Phase\_Shift****)* of the phases of all waveforms between two groups. This is implemented by maintaining the phases of the waveforms of the first group at 0; T/8; 2T/8; 3T/8; …; 7T/8, respectively while shifting all the phases of the waveforms of the second group by (i ×T/8) compared to that of the first group, where i is an integer depending upon 3-bits input. The mapping from 3 bits data to the shifting value of all phases of waveforms between two groups (value of i) is shown in table 209.

**Table 209. Mapping table from bits to S\_Phase\_Shift**

|  |  |
| --- | --- |
| 3-bits  **Input** | S\_Phase\_Shift / (T/8)  **Output** |
| 000 | 0 |
| 001 | 1 |
| 010 | 2 |
| 011 | 3 |
| 100 | 4 |
| 101 | 5 |
| 110 | 6 |
| 111 | 7 |

### 13.4.1.2.2 DS8-PSK Decoder

At a time, a camera makes sampling two groups of light sources, each group generates a set of eight ON/OFF states. The captured set of eight-states of a group shall be represented by S\_Phase as shown in table 211.

**Table 211: Determination of S\_Phase from states at different dimming levels**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **8-states Input** | | | | | | | **S\_Phase Output** |
| **Dimming 1/8** | **Dimming 2/8** | **Dimming 3/8** | **Dimming 4/8** | **Dimming 5/8** | **Dimming 6/8** | **Dimming 7/8** |
| 1000 0000 | 1000 0001 | 1000 0011 | 1000 0111 | 1000 1111 | 1001 1111 | 1011 1111 | 1 |
| 0100 0000 | 1100 0000 | 1100 0001 | 1100 0011 | 1100 0111 | 1100 1111 | 1101 1111 | 2 |
| 0010 0000 | 0110 0000 | 1110 0000 | 1110 0001 | 1110 0011 | 1110 0111 | 1110 1111 | 3 |
| 0001 0000 | 0011 0000 | 0111 0000 | 1111 0000 | 1111 0001 | 1111 0011 | 1111 0111 | 4 |
| 0000 1000 | 0001 1000 | 0011 1000 | 0111 1000 | 1111 1000 | 1111 1001 | 1111 1011 | 5 |
| 0000 0100 | 0000 1100 | 0001 1100 | 0011 1100 | 0111 1100 | 1111 1100 | 1111 1101 | 6 |
| 0000 0010 | 0000 0110 | 0000 1110 | 0001 1110 | 0011 1110 | 0111 1110 | 1111 1110 | 7 |
| 0000 0001 | 0000 0011 | 0000 0111 | 0000 1111 | 0001 1111 | 0011 1111 | 0111 1111 | 8 |

Likewise, a sampling that is called bad-sampling when camera captures on the transition time of a single LED among LEDs of the group shall generate a presence of an unclear state (x\_state). The determination of S\_Phase value under the presence of x\_state is as shown in table 218.

**Table 218: Determination of S\_Phase from states during dimming under presence of x\_state**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **8-states Input** | | | | | | | **S\_Phase Output** |
| **Dimming 1/8** | **Dimming 2/8** | **Dimming 3/8** | **Dimming 4/8** | **Dimming 5/8** | **Dimming 6/8** | **Dimming 7/8** |
| xx00 0000 | 1x00 000x | 1x00 00x1 | 1x00 0x11 | 1x00 x111 | 1x0x 1111 | 1xx1 1111 | 1 |
| 0xx0 0000 | x1x0 0000 | 11x0 000x | 11x0 00x1 | 11x0 0x11 | 11x0 x111 | 11xx 1111 | 2 |
| 00xx 0000 | 0x1x 0000 | x11x 0000 | 111x 000x | 111x 00x1 | 111x 0x11 | 111x x111 | 3 |
| 000x x000 | 00x1 x000 | 0x11 x000 | x111 x000 | 1111 x00x | 1111 x0x1 | 1111 xx11 | 4 |
| 0000 xx00 | 000x 1x00 | 00x1 1x00 | 0x11 1x00 | x111 1x00 | 1111 1x0x | 1111 1xx1 | 5 |
| 0000 0xx0 | 0000 x1x0 | 000x 11x0 | 00x1 11x0 | 0x11 11x0 | x111 11x0 | 1111 11xx | 6 |
| 0000 00xx | 0000 0x1x | 0000 x11x | 000x 111x | 00x1 111x | 0x11 111x | x111 111x | 7 |
| x000 000x | x000 00x1 | x000 0x11 | x000 x111 | x00x 1111 | x0x1 1111 | xx11 1111 | 8 |

After determining the values of S\_Phase for the pair of light sources, the value of ***S\_Phase\_Shift*** is calculated as following:

***S\_Phase\_Shift = S\_Phase(1) - S\_Phase(2)***

where *S\_Phase(1)* represents the *S\_Phase* value determined from LED-group 1; *S\_Phase(2)* represents the *S\_Phase* value determined from LED-group 2.

Finally, the de-mapping from S\_Phase\_Shift to 3 bits data shall be done inversely as the mapping table showed.

### 13.4.1.2.3 DS8-PSK Error Correction

The configuration of error correction for DS8-PSK shall be implemented over the PHY PIB attribute *phyOccFec.* If DS8-PSK modulation is selected and *phyOccFec = 1,* RS (15, 11) shall be used for DS8-PSK error correction.

Also, a majority bit voting shall be applied if the camera frame rate is higher than the optical clock rate and being considered as a type of temporal error correction. This is performed by configuring the optical clock rate over the PHY PIB attribute *phyOccOpticalClockRate* that is independent from the configuration of the modulation rate over the PHY PIB attribute *phyHSpskModulationRate*.

Also, the decoding under bad-sampling condition is considered as an error correction with the code rate equals 1.

### 13.4.1.2.4 DS8-PSK Dimming

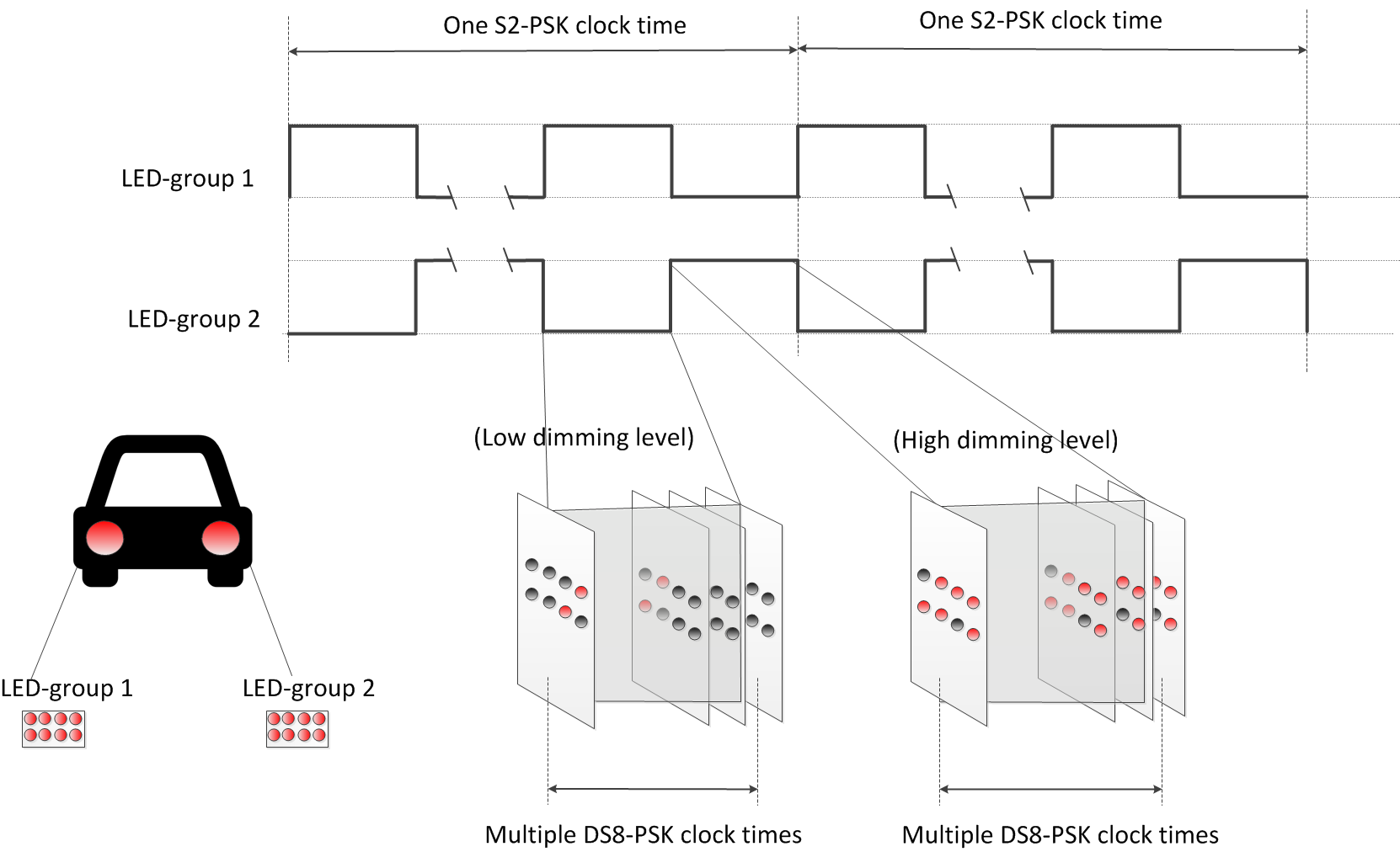
DS8-PSK dimming is supported in steps of 1/8 (12.5%). The dimming control is performed by the pulse width, not the amplitude. DS8-PSK dimming is a sub-set of VPPM dimming.

The configuration of dimming level is performed over the PHY PIB attribute *phyOccDim.*

## **13.4.1.3 HS-PSK**

### 13.4.1.3.1 HS-PSK Encoder

The DSM-PSK (e.g. DS8-PSK) encoder maps 3 bits data to waveforms driving LEDs on a pair of light sources at a high optical clock rate (such as 10kHz), meanwhile periodically change the dimming level from a selected low dimming level to a selected high dimming level. The change of dimming level during encoding that generates an AM signal at a low frequency of 200Hz (or 125Hz) shall be implemented over the S2-PSK encoder.



**Figure 2xx –HS-PSK for vehicular light sources**



**Figure 2xx – HS-PSK for LED Signage**

### 13.4.1.3.2 HS-PSK Decoder

For a dual-camera receiver system, the hybrid signal can be demodulated as below:

* A low frame rate camera (i.e. low-cost camera) is to detect the S2-PSK signal.
  + Can be either a global or a rolling shutter camera
  + Can be either a slow exposer or a quick exposer camera. A higher shutter speed camera is better for removing environmental noise and detecting LEDs.
* A high-speed camera (i.g. a global shutter and high frame rate camera) is to decode data from the DS8-PSK signal.

### 14.4.1.3.2 HS-PSK Error Correction

The configuration of error correction for HS-PSK shall be implemented over the PHY PIB attribute *phyOccFec.*

By default, no error correction is used for S2-PSK. However, a majority bit voting shall be applied if the camera frame rate (e.g. 30fps) is higher than the optical clock rate (e.g. 10Hz), and being considered as a type of temporal error correction.

For DS8-PSK in HS-PSK, RS (15, 11) shall be optionally used. Also, a majority bit voting shall be applied if the camera frame rate is higher than the optical clock rate (which is configurable over *phyOccOpticalClockRate*) and being considered as a type of temporal error correction. Also, the decoding under bad-sampling condition is considered as an error correction with the code rate equals 1.

### 14.4.1.3.2 HS-PSK Dimming Support

DS8-PSK dimming is supported in steps of 1/8 (12.5%). The dimming control is performed by the pulse width, not the amplitude. DS8-PSK dimming is a sub-set of VPPM dimming. The selection of the low dimming level and the high dimming level of DS8-PSK shall output the desired dimming level as following:

Output dimming level = ½ (low dimmed level + high dimmed level)

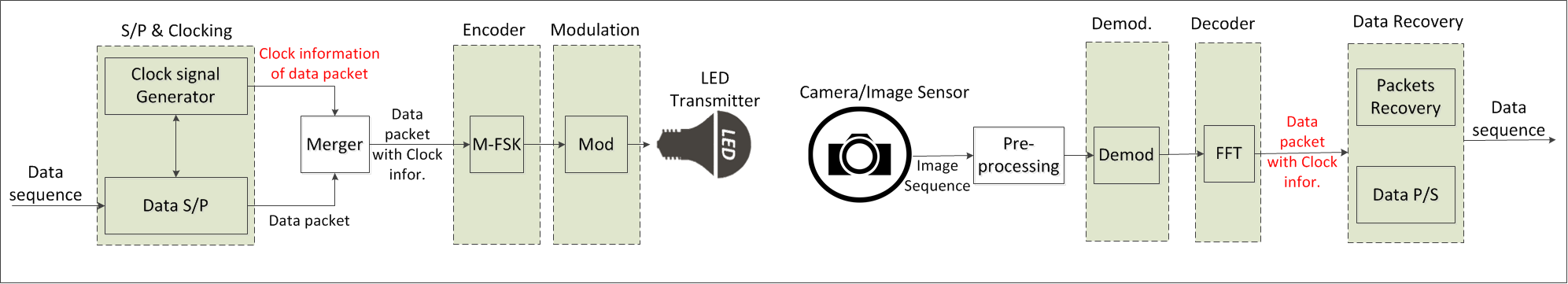
The configuration of desired dimming level is performed over the PHY PIB attribute *phyOccDim.*

# #6: PHY B Specifications

## **14.2 CM-FSK Modulation**

### 15.2.1 Reference Architecture

The CM-FSK modulation scheme is applied to a system as shown in **figure 288.** An LED panel is to transmit data modulated frequency-symbols, and by default, a rolling shutter camera is to receive data. A high-speed camera which the frame rate satisfying the Nyquist sampling can also be used instead of a rolling shutter camera.

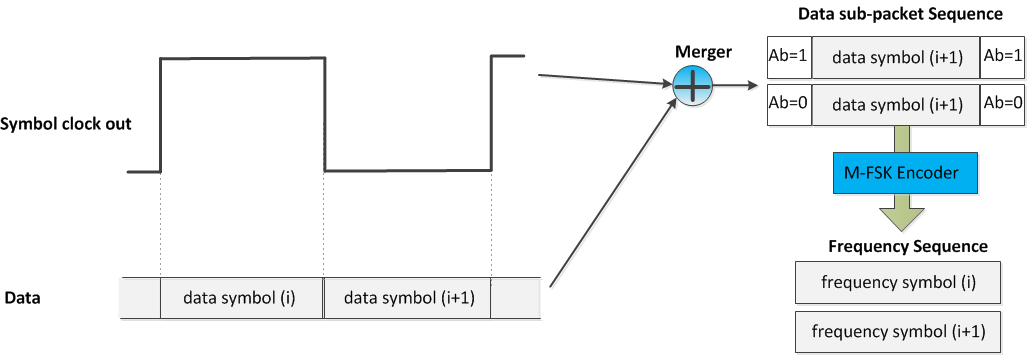
**

**Figure 288– Reference Architecture for CM-FSK system**

### 14.2.2 M-FSK Encoder

By default, a bit of clock information (Ab) is inserted at the beginning of a data packet to form a packet of bits. Also, the number of Ab bits may be increased being greater than one to support the detection of missing symbols during reception time in the receiver side. The configuration of Ab is implemented over the PHY PIB attribute *phyCmfskAb*.

The packet of bits is then mapped into a frequency symbol to transmit. Figure 289 illustrates an example of encoding procedure to map data into frequency symbol.

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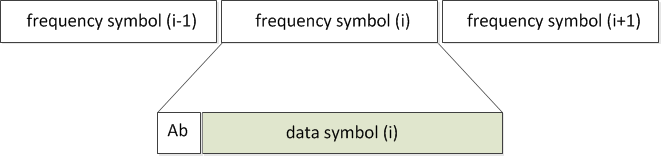
**Figure 289– Data and clock information merging in frequency domain**

The number of frequencies used to map data shall be configured over the PHY PIB attribute *phyCmfskNoFrequency*. 32 or 64 frequencies are suggested to use for selected devices. Also, the number of frequencies is extendable with reserved value of *phyCmfskNoFrequency*.

The frequency separation is fixed during a selected mode, and configurable over the PHY PIB attribute *phyCmfskFrequencySeparation.*

By default, all frequency symbols shall not modulate their phases. However, the number of phases is configurable over the PHY PIB attribute *phyCmfskNoPhase.* 2-PSK shall be additionally used in conjunction with M-FSK for a specific scenario, utilizing the bandwidth and coverage efficiency.

### 14.2.3 CM-FSK asynchronous communication

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**Figure 292– Data packet structure**

Asynchronous communication aims to support a varying frame rate camera demodulating data. A single Ab shall be inserted each data symbol and a camera that has a frame rate greater than the optical clock rate can be used to receive modulated data. The optical clock rate shall control the rate at which frequency symbols are clocked out, being lower than the selected camera frame rate. The configuration of the optical clock rate shall be implemented over the PHY PIB attribute *phyOccOpticalClockRate.*

### 14.2.3 32-FSK Modulation

32-FSK encodes a symbol of data, including one asynchronous bit and four data bits, into a frequency among selected 32 frequencies. The structure of symbol and the bits-to-symbol mapping table are as shown in figure 295.

**C32-FSK encoding table**

|  |  |
| --- | --- |
| Baud symbol | Frequency symbol |
| fSF | **fo** |
| 00000 | f1 |
| 00001 | f2 |
| . . . | . . . |
| 11110 | f31 |
| 11111 | f32 |
| f'SF | f33 |

**Symbol structure**

|  |  |
| --- | --- |
| Bits: 1 | 4 |
| Ab | Data |

**Figure 295– Symbol structure and 32-FSK encoding table**

Beside 32 frequencies are selected to encode a symbol of five bits, two additional frequencies are used as preamble symbols. The calculation of data frequencies and preamble frequencies is as follow:

* Data frequency: fi = fSF + i.∆f (i=1; 2;…; 32)
* Preamble frequency: f’SF = fSF + 33.∆f

where ∆f is the frequency separation value; fSF and f’SF are two preambles.

The configuration of the first frequency preamble (fSF) shall be implemented over the PHY PIB attribute *phyCmfskPreamble1*. This attribute is 200Hz by default.

### 14.2.4 64-FSK Modulation

64-FSK encodes a symbol of data, including one asynchronous bit and five data bits, into a frequency among selected 64 frequencies. The structure of symbol and the bits-to-symbol mapping table are as shown in figure 297.

**64-FSK encoding table**

|  |  |
| --- | --- |
| Baud symbol | Frequency symbol |
| fSF | **fo** |
| 00000 | f1 |
| 00001 | f2 |
| … | |
| 11110 | f31 |
| 11111 | f32 |
| f'SF | f33 |
| 010000 | f34 |
| 010001 | f35 |
| … | |
| 111110 | f64 |
| 111111 | f65 |

**Symbol structure**

|  |  |
| --- | --- |
| Bits: 1 | 5 |
| Ab | Data |

**Figure 297– Symbol structure and 64-FSK encoding table**

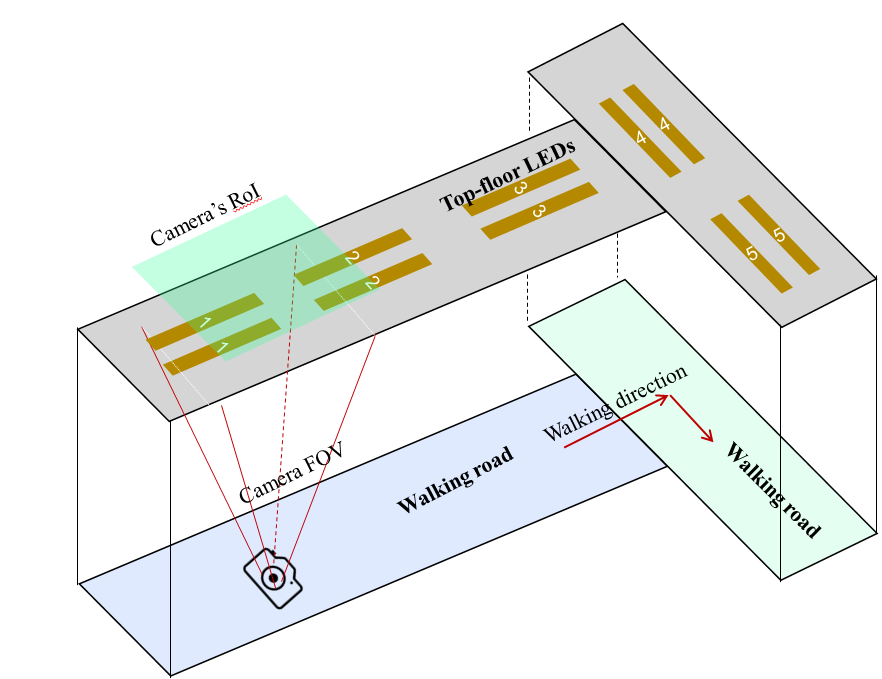
The 64-FSK frequency band is a twice extension of the 32-FSK frequency band. The first 32 data frequencies and two preamble frequencies are the same values as addressed in the 32-FSK modulation. Also, the other 32 frequencies are additionally allocated on the right side of the 32-FSK modulation band to achieve a higher capacity of data per frequency symbol.

### 14.2.5 Hybrid Frequency-Phase Shift Keying

The hybrid frequency and phase mode is enable when *phyCmfskNoPhase ≠ 0.*

The M-FSK is achieved by allocating different frequencies on the selected band. When *phyCmfskNoPhase =1,* 2-PSK modulation is additionally used on the hybrid modulation to tackle the bandwidth efficiency. The number of phases is two (zero-phase and inverse-phase) to modulate a square wave.

Figure 297 shows a use-case of hybrid M-FSK and 2-PSK. The modulation of M-FSK is applied the same for both LEDs within the pair of light sources. Whereas, bit “0” is mapped by modulating the same phase signals to a pair of LEDs, bit “1” is mapped by modulating the inverse-phase signals to the pair.



**Figure 297– A lighting system design using pairs of LEDs for hybrid M-FSK/2-PSK modulation**

## **14.3 C-OOK**

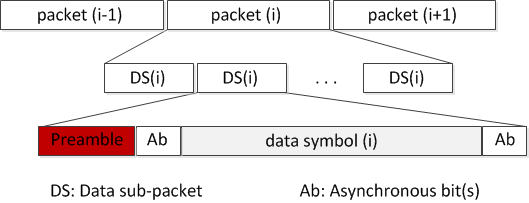
## **14.3.1 C-OOK Encoder**

C-OOK mode is selected if the PHY PIB attribute *phyOCCMscID* = 3.

A sub-packet of data shall be modulated using OOK modulation. The optical clock rate at which OOK symbols are clocked out is configurable over PHY PIB attribute *phyOccOpticalClockRate.* Two options of the optical clock rate, 2.2 kHz and 4.4 kHz, are suggested for the optical clock rate.

RLL coding shall be applied to maintain the average brightness at 50%. The configuration of RLL code shall be implemented over the PHY PIB attribute *phyOccRLLCode*. Manchester code and 4B6B code are suggested for C-OOK mode.

The data packet structure is as shown in figure 299. A packet is the multiple-times repetition of a data sub-packet to avoid missing data in between the gap time of adjacent images. The times of repetition depends on the selected mode, and is configurable over the PHY PIB attributes *phyCookPacketRate* and *phyCookSubPacketRate*. For example, if *phyCookPacketRate =1* specifying 10 packet/sec and *phyCookSubPacketRate =0* specifying 60 sub-packet/sec, every data sub-packet shall be repeated 6 times.



**Figure 299– Data packet structure**

A Data Sub-packet (DS) shall consist of a preamble symbol and payload section. The configuration of preamble is performed over the PHY PIB attribute *phyCookPreambleSymbol*. The preamble shall be configured being suitable to the selected RLL coding. Manchester coded payload shall require a short preamble while 4B6B coded payload shall require a longer preamble. Table 142 shows the suitable preamble for selected RLL code.

T**able 142: Data Sub-packet (DS) format**

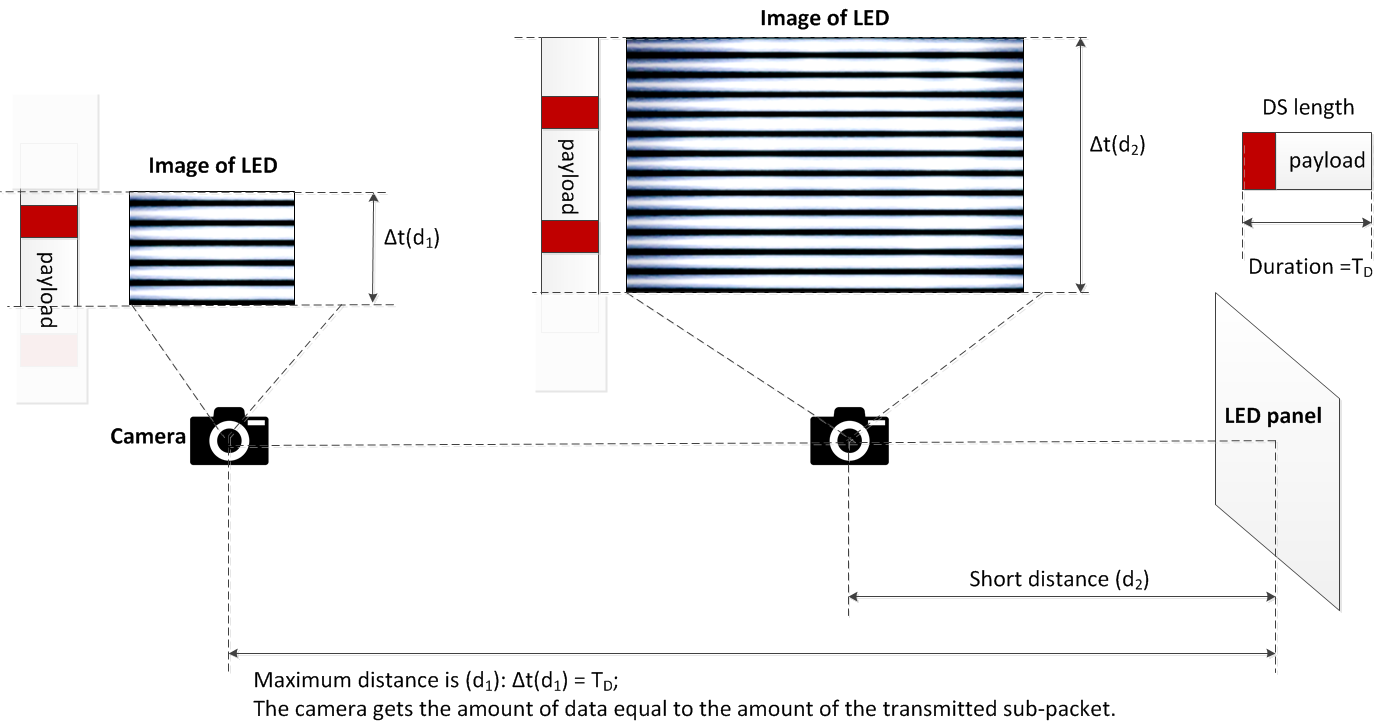
|  |  |  |  |
| --- | --- | --- | --- |
| **Preamble** | **DS Payload** | | |
| **Ab** | **Data** | **Ab** |
| 011100 | 1bit/  2 bits | Manchester coding | 1bit/  2 bits |
| 0011111000 | 4B6B coding |

The payload of DS shall consist of three parts: a front Ab, data, and a rear Ab. The front Ab and the rear Ab carry the same information, which consists of a single asynchronous bit or more. The configuration of the number of asynchronous bits for the front Ab and the rear Ab shall be implemented over the PHY PIB attribute *phyCookAb*.

The use of a single Ab to support Asynchronous Decoder shall be described in section 14.3.2. A pair of Ab bits to support the detection of missing packets shall be described in section 14.3.3.

### 14.3.2 C-OOK Asynchronous Decoder

To demodulate the entire data sub-packet DS, the distance from a camera to the LED transmitter should be close enough. Figure 301 shows the relationship between the amount of data being captured by the camera and the distance from the camera to the LED transmitter.



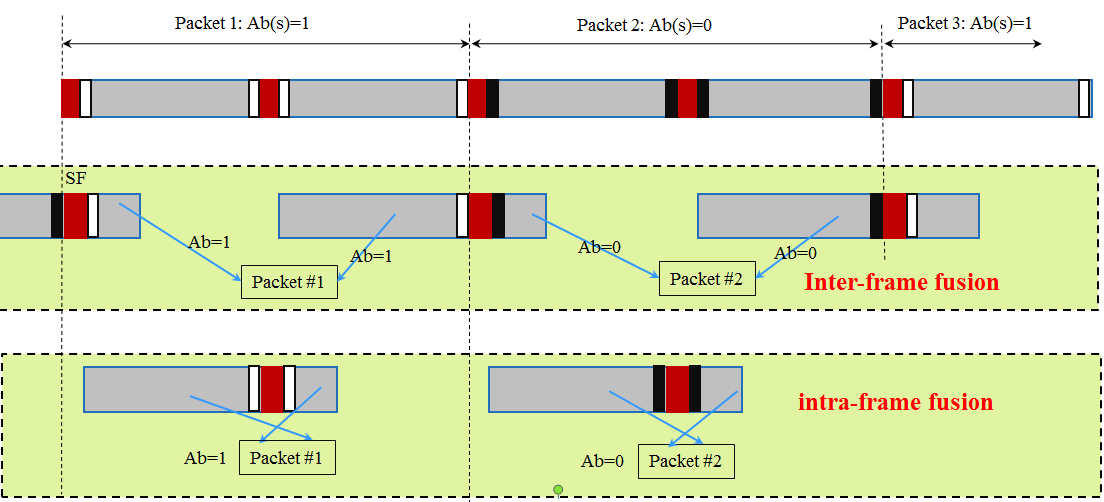
**Figure 301– Decoding scenario**

From the figure 301, the maximum distance achieved is the distance at which the camera gets the amount of data equal to the amount of the sub-packet.

**Decoding case 1: Fuse incomplete parts of a sub-packet into a complete one**

At this distance far, the distance d1 as shown in figure 301, the camera detects the preamble symbol and then demodulates the amount of data enough for a sub-packet; however, the uncertainty whether the forward part and the backward part counted from the position of the preamble belong to a sub-packet or not is problematic. The problem of a small amount of data also happens at a shorter distance when the transmitted sub-packet is long.

Asynchronous bits representing the clock information of the packet are used for the asynchronous decoding algorithm in this case.



**Figure 302– Decoding algorithm at a far distance**

Figure 302 illustrates the decoding algorithm to recover a packet of data from the forward part and the backward part of an image when the size of LED is small in the captured image. By observing the values of an asynchronous bit before and an asynchronous bit after the preamble, two statements of fusing those two parts of image are addressed:

* Case 1- *Inter-frame data fusion*: Fusing two sub-parts of a packet at two different images into a complete packet.

This type of data fusion is applied in case two Ab on an image are different.

* Case 2- *Intra-frame data fusion*: Recovering a complete packet from an image.

This type of data fusion is applied in case two Ab on an image are similar.

**Decoding case 2: Combination of Data Fusion and Majority Voting**

When the camera goes closer to the LED transmitter, the amount of data being captured per image is greater than that of a sub-packet. Therefore, the extra amount of data is used for correcting the possible error by applying a majority vote.

At distance d2 on figure 301, the amount of data equivalent to two sub-packets is captured. The majority voting is used in this case to correct the error throughout the entire sub-packet.

Figure 303 shows an experimental example of decoding under *Intra-frame data fusion.* The extra data after fusion a sub-packet is used for correcting the error by voting.

Assume that the camera frame rate may vary but be greater than the packet rate of transmission. Therefore, any extra data after fusion is useful for the error correction by grouping multiple images which belong to a sub-packet to vote. The voting is on the amount of data grouped from all of the forward parts and backward parts of images as well as extra data.



**Figure 303– An example of decoding employing intra-frame fusion along with error correction.**

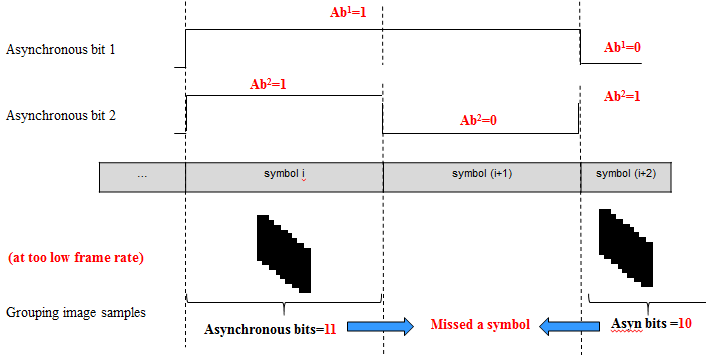
### 15.3.3 Missing packet detection on frame rate drop

The decoding algorithm in sub-clause 15.3.2 was proposed under the assumption of the receiver frame rate greater than the transmitting packet rate. In some circumstance, the frame rate may drop to less than the packet rate, causing to an entire packet is missed. The detection of the missed packet is proposed herein for a later process.

The core idea comes from the usage of asynchronous bits inserted into the payload of every sub-frame. Two bits (Ab1Ab2) are inserted at the forward and the backward of the body payload as shown in Figure 303. Those two bits together bring the clock information of the sub-packet and being modulated as shown in Figure 304.

|  |  |  |  |
| --- | --- | --- | --- |
| **Preamble** | **Ab (front)** | **Body payload** | **Ab (rear)** |
|  | 2 bits (Ab1Ab2) | Variable | 2 bits  (Ab1Ab2) |

**Figure 303– Data Sub-Packet Structure**



**Figure 304–Asynchronous bits transmission and a missed-symbol Detection**

Ab1 and Ab2 are square signals. Ab1 changes from zero/one into one/zero every time of single data packet, while Ab2 changes every time of two data packets.

The combination of two Ab, Ab1 and Ab2, generates four different values, 00 01 10 and 11. Therefore, the usage of those two Ab enables the detection of 2 missed packets continuously. It means the detection of missed packets is 100% successful for any frame rate drop to no less than 1/3 of the packet rate. For example, a packet rate at 10Hz with 2 Ab allows the frame rate drops to 3.3fps while all the missed packets are detectable.

### 15.3.3 Packet Structure Specification Modes

Tables below suggest some parameters for C-OOK modes.

**Table – Suggested Parameters for C-OOK modes**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Mode 1** | **Mode 2** | **Mode 3** | **Mode 4** |
| Optical clock rate | 2.2 kHz | 2.2 kHz | 4.4 kHz | 4.4 kHz |
| Sub-Packet rate | 100 DS/s | 60 DS/s | 60 DS/s | 60 DS/s |
| Bit rate | 60 bps | 150 bps | 580 bps | 700 bps |

**Table – Sub-Packet Structure on Suggested C-OOK modes**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Mode 1** | **Mode 2** | **Mode 3** | **Mode 4** |
| Preamble | 6B | 10B | 6B | **10B** |
| Front Ab | 2B | 2B | **4B** | **4B** |
| Payload (body) | 8 bits | 13 bits | 33 bits  (24B) | 41 bits  **(62B)** |
| Rear Ab | 2B | **2B** | **4B** | **4B** |

# #7: PHY C Specifications

## **16.1 A-QL Mode**

Updating. Resolution will be provided.

## **16.5 Hidden A-QL**

Updating. Resolution will be provided.