**IEEE P802.15**

**Wireless Personal Area Networks**

|  |  |
| --- | --- |
| Project | IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs) |
| Title | **2D-invisible sequential code**  |
| Date Submitted | May 2016 |
| Source | [Nam-Tuan Le, Trang Nguyen, Yeong Min Jang][Kookmin University][Seoul, Korea] | Voice: [ ]Fax: [ ]E-mail: [yjang@kookmin.ac.kr] |
| Re: | [If this is a proposed revision, cite the original document.][If this is a response to a Call for Contributions, cite the name and date of the Call for Contributions to which this document responds, as well as the relevant item number in the Call for Contributions.][Note: Contributions that are not responsive to this section of the template, and contributions which do not address the topic under which they are submitted, may be refused or consigned to the “General Contributions” area.] |
| Abstract | [PHY and MAC specification for 2D-invisible sequential code] |
| Purpose | [PHY and MAC specification of 2D-invisible sequential code for draft-D0-text-input] |
| Notice | This document has been prepared to assist the IEEE P802.15. It is offered as a basis for discussion and is not binding on the contributing individual(s) or organization(s). The material in this document is subject to change in form and content after further study. The contributor(s) reserve(s) the right to add, amend or withdraw material contained herein. |
| Release | The contributor acknowledges and accepts that this contribution becomes the property of IEEE and may be made publicly available by P802.15. |

**PHY Layer Operating mode(s)**

|  |
| --- |
| **PHY Operating Modes** |
| **Modulation****(m:n)** | **RLL Code** | **Optical Clock Rate** | **FEC** | **Data Rate (bits)****m x n x 15 x** RS\_rate x CC\_ rate |
| **Outer code (RS)** | **Inner code (CC)** |
| 2D-invisible sequential code 4:3 | None | 10Hz | RS\_option | CC\_option | **60** x RS\_ratex CC\_ rate |
| 2D-invisible sequential code 16:10 | None | 10Hz | RS\_option | CC\_option | **800** x RS\_ratex CC\_ rate |
| 2D-invisible sequential code 8:5 | None | 10Hz | RS\_option | CC\_option | **200** x RS\_ratex CC\_ rate |
| 2D-invisible sequential code 16:9 | None | 10Hz | RS\_option | CC\_option | **720** x RS\_ratex CC\_ rate |
| 2D-invisible sequential code 8:3 | None | 10Hz | RS\_option | CC\_option | **120** x RS\_ratex CC\_ rate |

N: Number of vertical cells

M: Number of horizontal cells

RS\_option: Select one RS scheme from Table 1

CC\_option: Select one CC scheme from Table 2

Figure 1 shows an example of cell configuration on display device with M=4 and N=3.

N=3

M=4

Figure 1. Example of cell construction

Table 1: Outer code (RS)

|  |  |  |
| --- | --- | --- |
| RS\_option | RS description | RS\_rate |
| 1 | None | 1 |
| 2 | RS(64,32) | 1/2 |
| 3 | RS(160,128) | 128/160 |
| 4 | RS(15,7) | 7/15 |
| 5 | RS(15,11) | 11/15 |
| 6 | RS(15,2) | 2/15 |
| 7 | RS(15,4) | 4/15 |

Table 2: Inner code (CC)

|  |  |  |
| --- | --- | --- |
| CC\_option | CC description | CC\_rate |
| 1 | None | 1 |
| 2 | CC(1/4) | 1/4 |
| 3 | CC(1/3) | 1/3 |
| 4 | CC(2/3) | 2/3 |

**2.0 PHY specifications**

2.1 Reference modulator diagram

The reference implementation diagram is in Figure 2.

Data

Serial to parallel

Display data

Encoder

Display device

FEC encoder

Figure 2. Reference modulator diagram

The image framing order for n x m bits data encoding is shown in Figure 3.

n x m bits data

Serial to parallel

Encoder

Reference image

m x n bits embedded image

FEC encoder

Figure 3. Image frame order

2.2 Invisible sequential code Encoder

The encoded bits in display cell are defined as:

Logic zero: represented by the unchanged sensitive element of color space.

Logic one: represented by the changed sensitive element of color space.

An example of logic bit encoding is shown in Figure 4.

Reference display

Modulated display

Figure 4. Example of modulated image frame with 110001000010 bits stream. (a. Reference image. b. Modulated image)

# PHY Layer Dimming Method

Invisible sequential code can support dimming by changing the brightness of display image. The brightness does not affect the invisible element of reference image and embedded image. The reference diagram is shown by Figure 5.

Data

Serial to parallel

Display data

Encoder

Display device

FEC encoder

Dimming level

Figure 5 Reference modulator diagram with dimming control data

1. **PPDU format**

The PPDU frame structure shall be formatted as illustrated in Figure 6.

PSDU

PHY header

Preamble

SHR

PHY payload

PHR

Figure 6Format of the PPDU

4.1 Preamble Field

The synchronization of one superframe data based on 2 mark image frames as Figure 7. Length of preamble field varies from 24 to 380 bits. It depends on the operation mode.

Synchronization 1

Synchronization 2

Figure 7 Preamble frame

4.2 PHY header

The PHY header, as shown in Table 2, defines the data length of data payload.

Table 2.

|  |  |  |
| --- | --- | --- |
| PHY header fields | Bit-width | Explanation on usage |
| PSDU length | 8 | Length up to aMaxPHYFrameSize |
| SS\_option | 4 | Provide information about SS option |
| RS\_option | 4 | Provide information about RS option |

4.3 PSDU field

The PSDU field has a variable length and carries the data of the PHY frame.

**5.0 PHY PIB attributes**

**6.0 Superframe Structure**

Invisible sequential code is applied for broadcasting mode. There is no access control mechanism. There is no superframe.

**7.0 MAC frame formats**

The MAC frame contains only frame Payload. The length of frame Payload is defined by PSDU length value of PHY header.

**8.0 MAC PIB attributes**