[1]IEEE P802.15
Wireless Personal Area Networks

Project	IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)
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Re:	IEEE 802.15 TG4q
Abstract	Samsung PHY Proposal documentation to IEEE 802.15.4q
Purpose	This document is intended to explain the overview and details of the Samsung PHY proposal submitted in response to the call for proposal (CFP) from IEEE 802.15.4q.
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Release	The contributor acknowledges and accepts that this contribution becomes the property of IEEE and may be made publicly available by P802.15.

[1] Samsung

PHYSICAL LAYER PROPOSAL DOCUMENTATION

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1. Introduction

The scope of this document spans the proposal for physical (PHY) layer amendment as response to the Call for Proposals issued by the IEEE 802.15.4q Task Group. This document will address the modulation, coding schemes and preambles required for the 802.15.4q physical layer. It also addresses how the proposal meets different technical requirements documented by TG4q. Finally, it summarizes the capabilities of the proposal in meeting the specifications in the technical guidance document.

2. Technical Requirements for IEEE 802.15.4q

The requirements that are set forward by the IEEE 802.15.4q are

- Support for a communication range of
  - 30 m in a free-space environment, at the lowest mandatory rate.
  - 10 m in an indoor environment, at the lowest mandatory rate.
- Ultra low power (ULP) capability of 15 mW.
- Performance requirement of 1% packet error rate (PER) for a packet size of 20 bytes.
- Regulatory compliance.

The criteria relevant to PHY layer of TG4q are

- Power consumption estimates at the transmitter and at the receiver, for an emitted isotropic radiation power (EIRP) of -5 dBm.
- Interference rejection capability.
- Co-existence with other networks.

3. Overview of Proposal

This proposal is designed to satisfy the technical requirements of the IEEE 802.15.4q. The rest of the document deals with following aspects:

- Transmission Protocol
  - Transmitter block diagram.
  - Frame format.
  - Forward error correction (FEC).
  - Interleaving.
  - Modulation based on pseudo random and orthogonal ternary sequences.
  - Pulse shaping.
  - Preamble and start frame delimiter (SFD) specifications.
  - Supported data rates.
  - Band plan and co-existence.
  - Transmit signal power spectral density.
- Receiver Architecture
  - Non-coherent receiver architecture.
- Performance Evaluation
- Link budget calculation
- Power consumption
- Compliance with TGD

4. Transmission Protocol

Transmission protocol described in this section is applied to the Protocol service data unit (PSDU).

4.1 Frame Format

The physical layer frame (PPDU) is formed from the PSDU as shown in

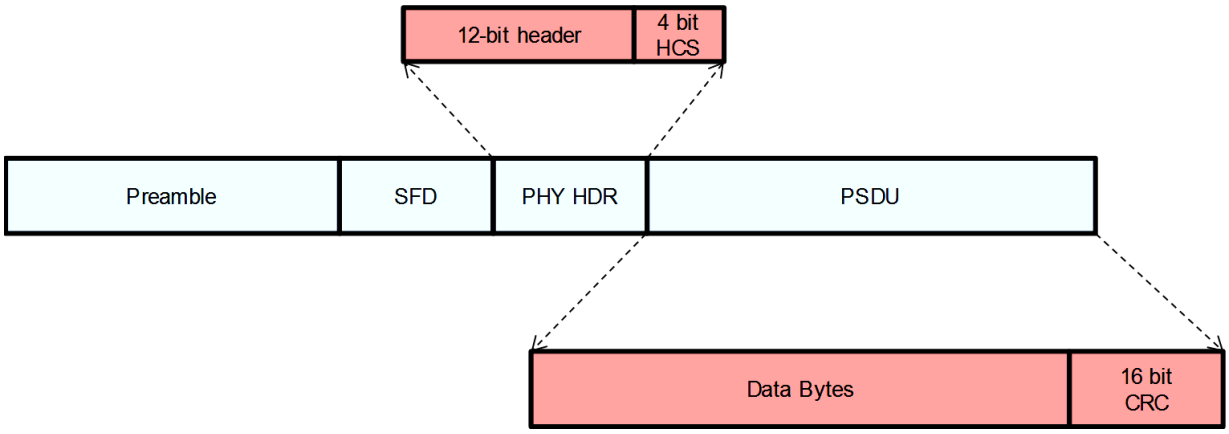

Figure 4.1-1 Physical layer frame format.

The physical layer frame consists of the following four fields:

a. Preamble: This field consists of specific bit-pattern for frame synchronization.
b. Start frame delimiter (SFD): This field identifies the beginning of the frame and re-confirmation of the synchronization.
c. PHY header (HDR): This field contains useful information regarding the parameters such as length indication, modulation and coding schemes used.

4.2 Transmitter Block Diagram

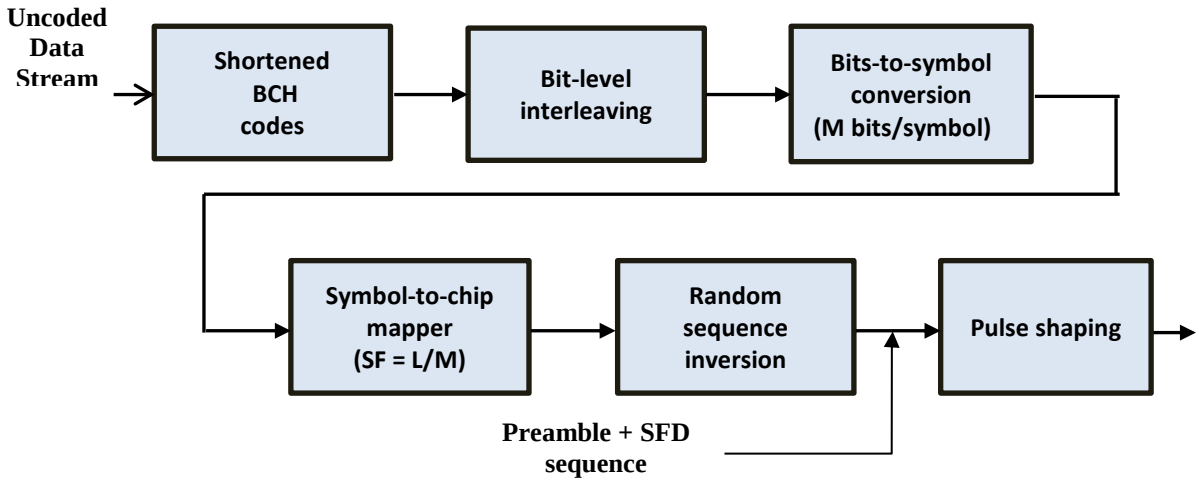

Figure 4.2-1 Block diagram of the transmitter.

Uncoded data (PSDU) is received from the higher layer in form of bits, and is passed through the following baseband processing mechanisms before RF processing (up-conversion) and transmission.

1) Shortened BCH encoding: to protect data against channel induced errors and to ensure uniform error protection across the data.
2) Bit-level interleaving: combined with FEC to minimize bit errors in the event of symbol errors.
3) Bit-to-sequence mapping (using ternary orthogonal sequences): converts the symbol into sequence of chips in order to give robustness against channel noise and interference.
4) Random sequence inversion: inverts the polarity of incoming spreading sequences in a random fashion. This is done to minimize direct current (DC) and harmonic components in the transmitted signal, resulting in smooth continuous power spectral density (PSD). This block operates at the rate of symbol clock.
5) Pulse shaping: Performs pulse shaping to limit the out of band emissions.

In the following sections, we build a detailed framework for the transmitter blocks and their operation on incoming signals/bits.

4.3 Shortened BCH Codes

The "Shortened BCH codes" will add error protection bits to the PSDU. The shortened versions of 2-bit error correcting BCH (63, 51) codes are used. The generator polynomial and parity polynomial for BCH (63, 51) codes are given by

$$g(x) = 1 + x^3 + x^4 + x^5 + x^8 + x^{10} + x^{12} \quad (4.3.1)$$

$$p(x) = \mathrm{mod}(x^{12}m(x), g(x)) \quad (4.3.2)$$

where m(x) is the message bits polynomial.

Parity bits for every message block can be achieved by using a simple linear feedback shift register (LFSR) circuit as shown in the Figure 4.3-1.

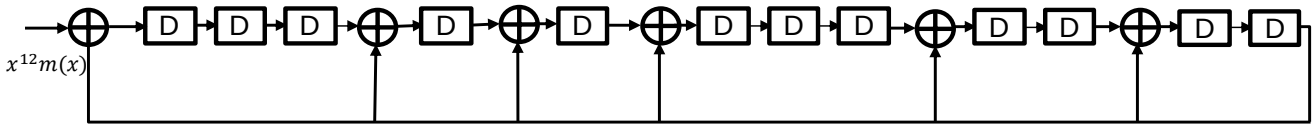

Figure 4.3-1 LFSR based implementation of parity generator for BCH (63, 51) code.

Shortened BCH codes, denoted by BCH$(63-\ell, 51-\ell)$, can be obtained from the above BCH(63,51) code for any given $1 \leq \ell < 51$. Shortened code parameters are calculated as below for any PSDU length.

Total number of message blocks,

$$M_B = \left\lceil \frac{N_{PSDU}}{51} \right\rceil \qquad (4.3.3)$$

N_{PSDU} – length of the packet in bits.

Length of the new message block,

$$K = \left\lceil \frac{N_{PSDU}}{M_B} \right\rceil \qquad (4.3.4)$$

Shortening length of the code,

$$\ell = 51 - K \qquad (4.3.5)$$

Length of the new encoded block,

$$N = 63 - \ell \qquad (4.3.6)$$

Length of the new bit-stream,

$$N_{zeropad} = M_B K \qquad (4.3.7)$$

Required number of zeros for insertion

$$Z = N_{zeropad} - N_{PSDU} \qquad (4.3.8)$$

Thus, M_B message blocks of K bits are formed. Each of these message blocks is passed through the parity generator circuit (shown in Figure 4.3-1) to yield the corresponding 12-bit parity. The resulting parity bits are appended at the end of the message block to obtain the corresponding codeword. The total number of bits at the output of shortened BCH codes block for a PSDU can be calculated as

$$N_{coded} = M_B N \qquad (4.3.9)$$

4.4 Bit-level Interleaving

Once codewords are obtained from the BCH encoder, bit-level interleaving is performed on the encoded data, where bits across codewords are interleaved with an appropriate chosen depth. The primary purpose of this operation is to protect bit errors against symbol errors. Typically, the interleaving depth is chosen based on the modulation. Let N be the length of the codeword. Let d be the interleaver depth. The following procedure is followed for one round of interleaving:

a. Collect d blocks of codewords
b. Write them **row-wise** in a $d \times N$ dimensional array.
c. Read the array **column-wise** and output the data sequentially.

The following sketch depicts the procedure for an interleaving depth of $d = 4$.

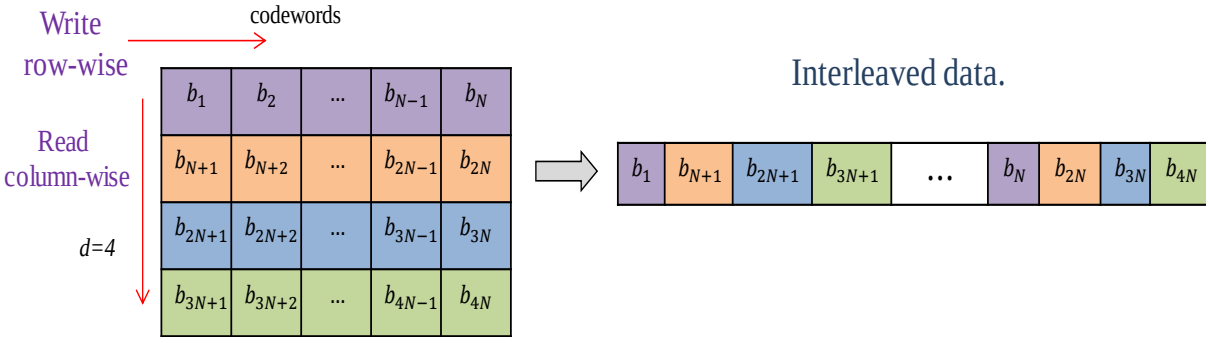

Figure 4.4-1 Interleaving operation for depth d = 4.

4.4.1 Calculation of interleaving blocks

Next, we outline the calculation of number of blocks for interleaving. Let M_B be the number of codewords obtained from the encoder stage. Depending on the modulation, choose an appropriate value for d.

Define the parameters

$$Q = \left\lfloor \frac{M_B}{d} \right\rfloor; \quad r = mod\,(M_B,\, d\,) \qquad (4.4.1)$$

Perform d-depth interleaving for the block of $d \cdot Q$ codewords and perform r-depth interleaving for rest of r codewords.

4.5 Bits-to-Symbol Conversion

This block takes the bit stream from the interleaver, and packs them into blocks of M bits each. Each block comprises a "symbol". Therefore, we can interpret this as each symbol conveying M bits of information. After packing, each symbol is passed to the modulation block for symbol-to-chip mapping. The value of M is chosen appropriately based on the modulation scheme employed.

4.6 Modulation: Symbol-to-Chip Mapping

This part performs the baseband modulation. In the present context, the modulation is performed by a process of mapping symbol to a sequence of chips. Succinctly, for every symbol (M bits/symbol) generated at its input, the modulator outputs a unique sequence from a pre-defined set of L-length ternary sequences. The ratio $SF = L/M$ is the spreading factor of the modulation scheme. The choice of SF is determined by the data rate requirements. We call this as the ***Variable Spreading Factor-Ternary ON-OFF Keying*** (VSF-TOOK).

The "Bit-to-Symbol Converter"- stage converts binary stream of bits into a sequence of M-bit symbols. Equivalently, this procedure maps bit stream from binary alphabet on to a symbol alphabet $\mathbb{S}$, which is defined as

$$\mathbb{S} \stackrel{\text{def}}{=} \{0, 1, \dots, A-1\}, \qquad \text{where } A = 2^M.$$

Corresponding to each symbol $m \in \mathbb{S}$, define a unique L-length, ternary sequence as

$$\mathbf{c}_m = \left[c_m[0], \dots, c_m[L-1]\right]^T, \qquad c_m[n] \in \{-1, 0, +1\} \;\; n \in \{0, \dots, L-1\}.$$

The collection of these sequences is denoted by the set

$$\mathbb{C} \stackrel{\text{def}}{=} \{\mathbf{c}_0, \dots, \mathbf{c}_{A-1}\}.$$

We call the set $\mathbb{C}$ as the *spreading code* and its elements are called the *spreading sequences.* It needs to be emphasized that the spreading code $\mathbb{C}$ is designed such that the spreading sequences in the set are mutually near-orthogonal, i.e., ideally it is expected that $\mathbf{c}_{m_1}^{\mathrm{T}}\mathbf{c}_{m_2} = 0, \; \forall\, \mathbf{c}_{m_1}, \mathbf{c}_{m_2} \in \mathbb{C}, \; m_1 \neq m_2$.

We define the modulation using spreading sequences as the mapping:

$$\mathcal{M}: \mathbb{S} \rightarrow \mathbb{C}.$$

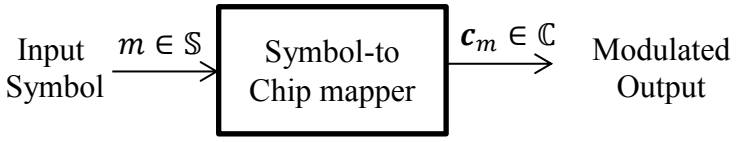

Figure 4.6-1 Modulation process: Symbol-to-chip mapping.

Bits	Symbol ($\mathbb{S}$)	Mapping	Spreading code ($\mathbb{C}$)
000	0	→	$\mathbf{c}_0$
001	1	→	$\mathbf{c}_1$
010	2	→	$\mathbf{c}_2$
011	3	→	$\mathbf{c}_3$
100	4	→	$\mathbf{c}_4$
101	5	→	$\mathbf{c}_5$
110	6	→	$\mathbf{c}_6$
111	7	→	$\mathbf{c}_7$

Figure 4.6-2 Illustrative example for modulation for M=3.

For the given symbol m, in a pre-determined manner, the modulator maps it onto a specific spreading sequence $\mathbf{c}_m$ in $\mathbb{C}$. This procedure is illustrated in Figure 4.6-1. Further, we have also illustrated the idea through an example in Figure 4.6-2.

4.6.1 Design of spreading codes

There are two types of codes chosen for modulation: orthogonal codes and pseudorandom codes.

i. **Orthogonal code:** This code is used for the case $M = 1$, i.e., symbols are binary. Orthogonal code consists of two ternary sequences which are perfectly orthogonal to each other. These sequences exclusively map symbols '1' and '0'.

ii. **Pseudorandom code:** This code consists of a set of $A = 2^M$ sequences with good cross-correlation properties. The sequences are typically chosen to be pseudorandom sequences. To reduce the complexity of implementation, we can generate the pseudorandom code as follows:

   a) Obtain an L-length pseudorandom sequence with good cyclic autocorrelation property. This is the spreading sequence $\mathbf{c}_0$. We call this the *"basic sequence".*

   b) For $m = 1, \dots, A-1$, circular-shift $\mathbf{c}_0$ by m positions to obtain $\mathbf{c}_m, m = 1, \dots, A-1$.

   The above procedure generates the spreading code $\mathbb{C} = [\mathbf{c}_0, \cdots, \boldsymbol{c}_{A-1}]$. Since we start with the basic sequence $\mathbf{c}_0$ that has good cyclic autocorrelation properties, it is guaranteed that elements of $\mathbb{C}$ exhibit good cross-correlation properties.

4.6.2 Definitions of modulation schemes

The choice of modulation schemes depends on the factors such as the performance and required data rate. The following tables give the different modulation schemes employed, with their definitions and the nomenclature.

Orthogonal Codes:

M	L	Nomenclature	Orthogonal Sequences (symbols: '1' / '0')
1	1	1/1-TOOK	1 / 0
	2	1/2-TOOK	[1 0] / [0 -1]
	4	1/4 -TOOK	[1 0 0 1] / [0 -1 -1 0]
	8	1/8 -TOOK	[1 0 -1 0 0 -1 0 1] / [0 -1 0 1 1 0 -1 0]

Pseudorandom Codes:

M	L	Nomenclature	Basic Sequence ($\mathbf{c_0}$)
2	4	2/4-TOOK	[1 0 0 0]
3	8	3/8-TOOK	[0 0 0 1 -1 0 1 1]

4	16	4/16-TOOK	[1 -1 0 0 0 0 1 0 -1 0 0 1 1 0 1 1]
5	32	5/32-TOOK	[-1 0 0 1 0 1 -1 0 -1 -1 1 -1 0 1 0 1 0 0 0 1 0 0 1 1 -1 0 0 0 0 0 1 1]

4.7 Random Sequence Inversion

This block is used to mitigate the spectral lines in the transmitted signal. This is achieved by randomly inverting the polarity of all the chips in a spreading sequence. Thus, it eliminates the dependence of a signal's spectrum upon the actual transmitted data, making it more dispersed to meet the spectral regulation requirements. This operation works at the symbol level (at spreading sequence level) and the random phase inversion is achieved by the use of a pseudorandom binary sequence (PRBS) generator, whose output is used in deciding whether to invert the spreading sequence or not. The sketch of the block is as shown below.

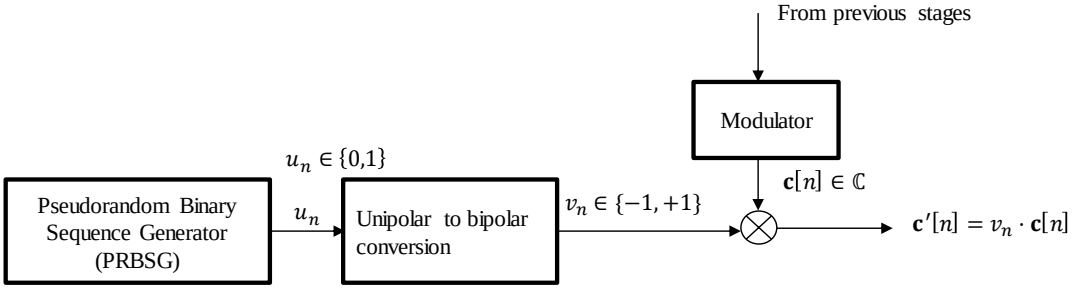

Figure 4.7-1 Schematic of the random sequence inversion stage.

The PRBS generator is obtained by using the ITU 16-bit scrambler. The shift register implementation of PRBS generator is illustrated in Figure 4.7-2

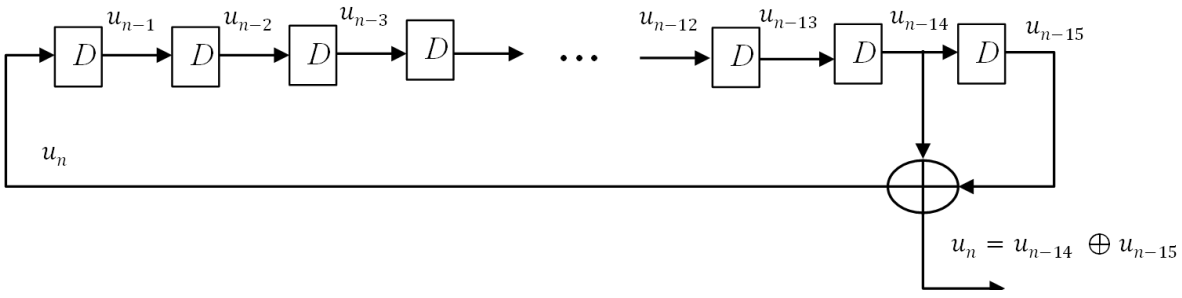

Figure 4.7-2 Linear feedback shift register based implementation of the PRBS generator.

The PRBS generator employs the generator polynomial

$$G(x) = 1 + x^{14} + x^{15}.$$

Therefore, the pseudorandom binary sequence output is generated recursively as

$$u_n = u_{n-14} \oplus u_{n-15}, \qquad n = 0,1,\ 2, \ldots$$

where $\oplus$ is the modulo-2 addition operator. Further, the initial seed of the PRBS is denoted by

$$u_{init} = [u_{-1},\ \ldots, u_{-14},\ u_{-15}]$$

The randomization pattern depends on u_{init}.

The output of the PRBS generator $\{u_n\}$, which is a unipolar binary sequence, is passed through the bipolar converter to yield a bipolar sequence $\{\ v_n\}$. The conversion operation can be represented as

$$v_n = 2u_n - 1.$$

That is

$$v_n = \begin{cases} 1 & \text{if } u_n = 1 \\ -1 & \text{if } u_n = 0 \end{cases}.$$

The polarities of the sequences are randomly inverted as:

$$\mathbf{c}'[n] = v_n \cdot \mathbf{c}[n], \qquad \mathbf{c}[n] \in \mathbb{C},\ \ n = 1, \ldots$$

4.8 Pulse Shaping

The Gaussian pulse with a time-bandwidth product of BT = 0.3 is used as the pulse shaping filter. The impulse response of the filter is given by

$$g(t) = B\sqrt{2\frac{\pi}{\ell n(2)}} * e^{-\left(\frac{2\pi^2 B^2 t^2}{\ell n\ 2}\right)} \qquad (4.8.1)$$

where B is the bandwidth. The time domain response and frequency domain response of the Gaussian pulse shaping filter with BT = 0.3 and $T = 1\mu s$ are as illustrated below

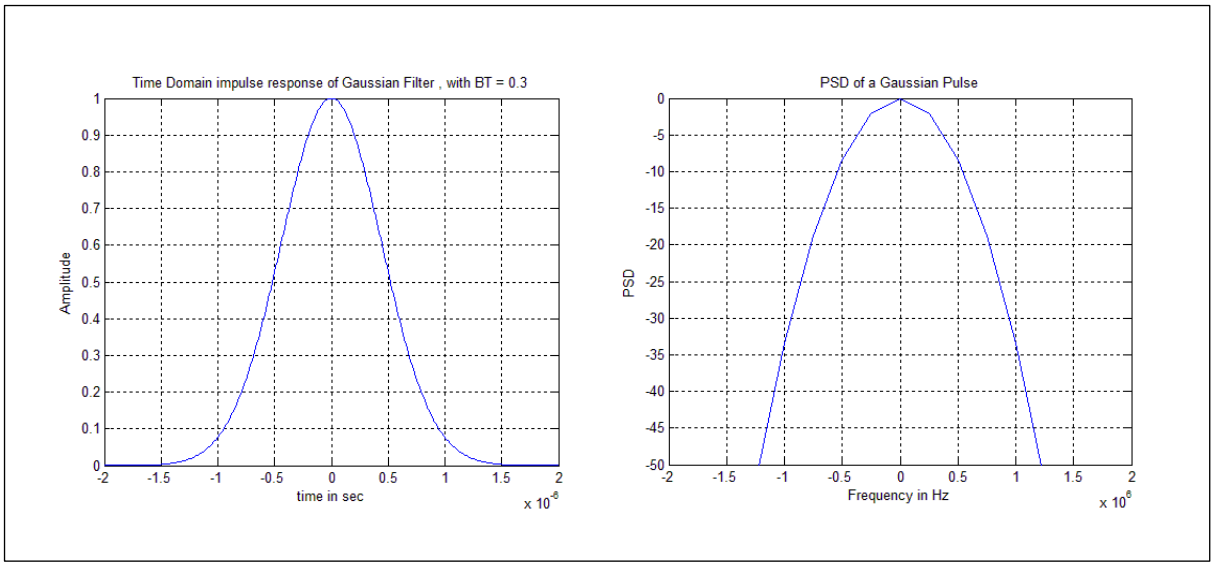

Figure 4.8-1 Time domain and frequency domain responses of the Gaussian pulse shaping filter.

4.9 Preamble and SFD

Four different preambles are defined for supporting multiple data rates in order to maximize the energy efficiency of PSDU. For any preamble, a 32-bit base sequence is repeated N_{rep} times. Preamble is immediately followed by an SFD bit-pattern which is again spread by the base sequence. Depending on the length and type of base sequence used, four different combinations of preamble and SFD are defined.

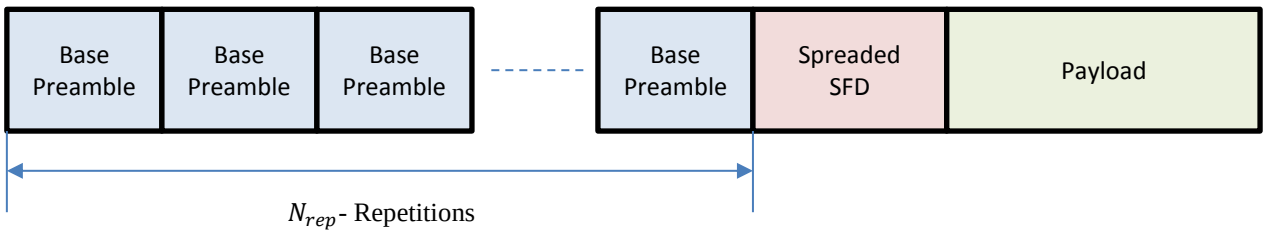

Figure 4.9-1 Preamble and SFD Structure.

The values for base preamble and N_{rep} are given below in Table 4.9-1.

Table 4.9-1 Definitions related to preamble.

Preamble Defn.	Spreading Factor (SF)	Base Preamble Sequence	Number of Repetitions (N_{rep})
P1	2	-1 0 -1 0 1 0 1 0 -1 0 -1 0 1 0 -1 0 1 0 1 0 1 0 -1 0 -1 0 1 0 -1 0 -1 0	2
P2	4	1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 -1 -1 0 0 1 -1 0 0 1 -1 0 0 1 -1 0 0 -1	4

P3	8	1 0 -1 0 0 -1 0 -1 1 0 1 0 0 -1 0 1 1 0 1 0 0 -1 0 1 -1 0 1 0 0 1 0 1	8
P4	16	-1 0 -1 0 -1 0 -1 0 0 -1 0 1 0 1 0 -1 -1 0 1 0 -1 0 1 0 0 1 0 1 0 -1 0 -1	16

Final sequence of spreaded SFD is obtained by spreading the 8 chip sequence [0 1 0 1 1 0 0 1] by a spreading code. The spreading codes for different SFDs are given in Table 4.9-2. These spreading codes are referred as S1, S2, S3 and S4.

Table 4.9-2 Spreading sequences for SFD

Spreading Factor (SF)	Spreading sequence for SFD (for bit 1 and bit 0)
S1 (2)	[10]/[0 -1]
S2 (4)	[1 0 0 1]/ [0 -1 -1 0]
S3 (8)	[1 0 -1 0 0 -1 0 1]/ [0 -1 0 1 1 0 -1 0]
S4 (16)	[1 0 -1 0 -1 0 1 0 0 1 0 -1 0 -1 0 1] / [0 -1 0 1 0 1 0 -1 -1 0 1 0 1 0 -1 0]

4.10 Data Rates Supported

The data rates supported for 2.4 GHz and 900 MHz are listed in Table 4.10-1. The chip rate considered for 2.4 GHz and 900 MHz bands are 1 MCPS and 600 KCPS respectively. The Preamble and SFD to be used for these data rates are mentioned as well in the Table 4.10-1. We propose to have data rates D5 and D7 (given below) as the mandatory data rates to support control information.

Table 4.10-1 Preamble, SFD and modulation combinations and corresponding data rates.

Data Rate Number	Code used	Modul-ation Duty Cycle	Inter-leaver depth (d)	M (bits per Symb)	L (chips Per Symb)	Data Rate in 2.4 GHz (kbps)	Data Rate in 900 MHz (kbps)	Pream-ble Used	SFD Spread-ing used
D1	1/1-TOOK	0.50	1	1	1	809.5	485.7	P2	S2
D2	2/4-TOOK	0.25	2	2	4	404.8	242.8	P2	S2
D3	3/8-TOOK	0.50	3	3	8	303.6	182.1	P3	S3
D4	1/4-TOOK	0.50	1	1	4	202.4	121.4	P3	S3
D5	4/16-TOOK	0.50	4	4	16	202.4	121.4	P3	S3
D6	5/32-TOOK	0.50	4	5	32	126.5	75.9	P4	S4
D7	1/8-TOOK	0.50	1	1	8	101.2	60.7	P4	S4

Table 4.10-2 Payload efficiencies for 40 bytes of payload size

Data Rate Number	D1	D2	D3	D4	D5	D6	D7
Payload efficiency for 40 bytes (%)	69.69	82.14	83.63	82.14	82.14	78.63	82.14

4.11 Band Plan and Co-existence

The band plan proposal is exactly similar to that of **IEEE 802.15.4 2011** document to enable the co-existence with existing IEEE 802.15.4 physical layers and other standards. The band plans for 2.4 GHz and 900 MHz bands are as shown below.

For 2.4 GHz Band

$$F_c = 2405 + 5k\,, \qquad k = 0,1,\ldots,15. \qquad (4.11.1)$$

For 900 MHz Band

$$F_c = 906 + 2k\,, \qquad k = 0,1,\ldots,9. \qquad (4.11.2)$$

4.12 Power Spectral Density

The power spectral density of the modulated baseband signal for 1 MHz chip rate is as shown in Figure 4.12-1.

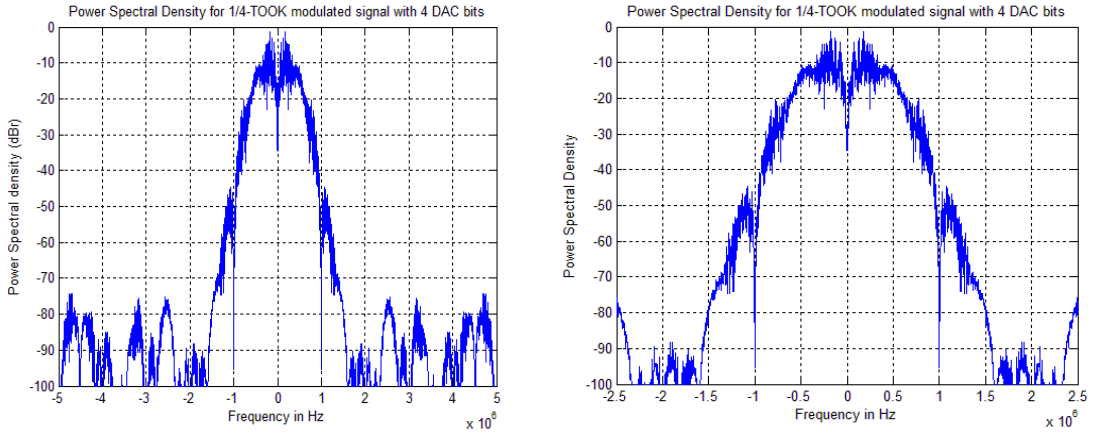

Figure 4.12-1 Power spectral density of baseband modulated signals.

Table 4.12-1 Out-of-band emissions.

POWER LEAKAGE RATIO	VALUE
Adjacent channel leakage ratio	-69 dB
Alternate channel leakage ratio	-72 dB

5 Receiver Architecture

The transmission protocol proposed allows both the coherent and non-coherent form of reception. However, in this article, unless mentioned, the architecture and the results presented hold for non-coherent receiver. For benchmarking, results for ideal coherent receiver are also published.

5.1 Receiver Block Diagram

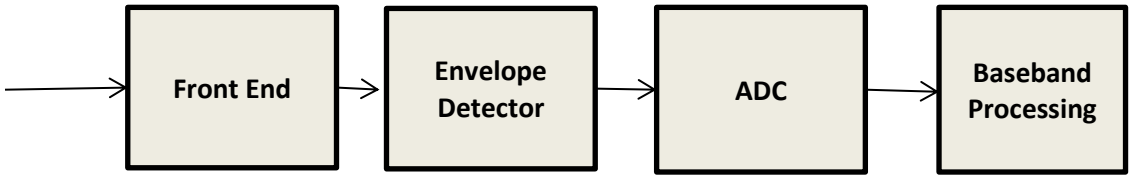

Figure 5.1-1 Non-coherent receiver architecture.

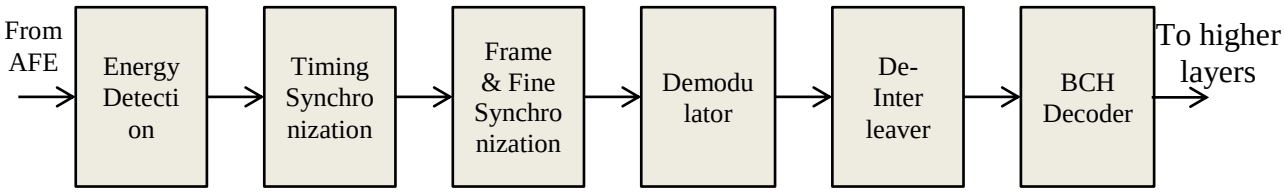

Figure 5.1-2 Block diagram of baseband processing at the receiver.

The receiver front-end used for the non-coherent reception of data is based on the super-regenerative principle.

5.1.1 Energy Detection

Energy detector detects the presence of useful signal. This is performed by accumulating signal energy of 16 chips and then comparing it against a pre-computed threshold.

$$signal\ present = \begin{cases} 1 & if \sum_{n=1}^{16} y(n)^2 \geq \gamma_{TH} \\ 0 & otherwise \end{cases} \qquad (5.1.1)$$

5.1.2 Timing Synchronization

Timing synchronization is performed by sliding correlation of input signal in unipolar mode with preamble template in bi-polar mode. Length of each correlation window is N_p chips. The Time at which the maximum correlation is achieved is taken as symbol timing estimate, $\hat{\tau}$, given by

$$\hat{\tau} = \underset{j}{\operatorname{argmax}} \sum_{i=1}^{N_p} x[i]y[i+j] \qquad (5.1.2)$$

$\left[x[1], x[2] \ldots, x\left[N_p\right]\right]$ – preamble template at Rx

$\{y[1], y[2] \ldots, \}$ – baseband samples at Rx

5.1.3 Frame Synchronization

Once timing synchronization is obtained through preamble, SFD is used for the re-confirmation of the timing estimate. This is achieved by decoding the SFD field bit-by-bit, and then comparing the resultant bit-pattern with the actual SFD bit-pattern.

5.1.4 Demodulator

The demodulator detects the transmitted symbol based on correlation of spreading sequences. The demodulator calculates the correlation metric of the received sequences with all possible chip sequences. The transmitted symbol is detected as the symbol corresponding to the chip sequence which gives the maximum correlation.

Symbol estimate at epoch n, $\widehat{m}_n$

$$\widehat{m}_n = \underset{m \in \{0, \ldots, M-1\}}{\operatorname{argmax}} \mathbf{s}_m^T \mathbf{y}_n$$

$\mathbf{y}_n = [y_n[1], \ldots, y_n[L]]$ – received samples corresponding to symbol at epoch *n*

$\mathbf{s}_m^T = \left[s_m[1], \ldots, s_m[L]\right]$ – spreading sequence corresponding to the symbol *m.*

5.1.5 De-Interleaver

This block performs the inverse operation of interleaver described in the transmitter section, and recovers the encoded bits from interleaved data.

The following procedure is followed for one round of de-interleaving:

a. Collect $d \cdot N_{new}$bits.
b. Write them **column-wise** in a $d \times N_{new}$ dimensional array.
c. Read the array **row-wise** and output the data sequentially.

5.1.6 BCH decoder

The BCH decoder recovers the message bits from the received codewords. During the process of decoding, the decoder corrects bit-errors induced by the channel. We employ a BCH$(63 - \ell, 51 - \ell)$ decoder which can correct up to 2 bit errors per codeword. More details on decoding process and algorithms can be found in classical texts such as [1].

6 Performance Curves

This section describes the performance of the proposed system for various proposed modulation formats under various channel conditions.

6.1 Performance in AWGN Channel

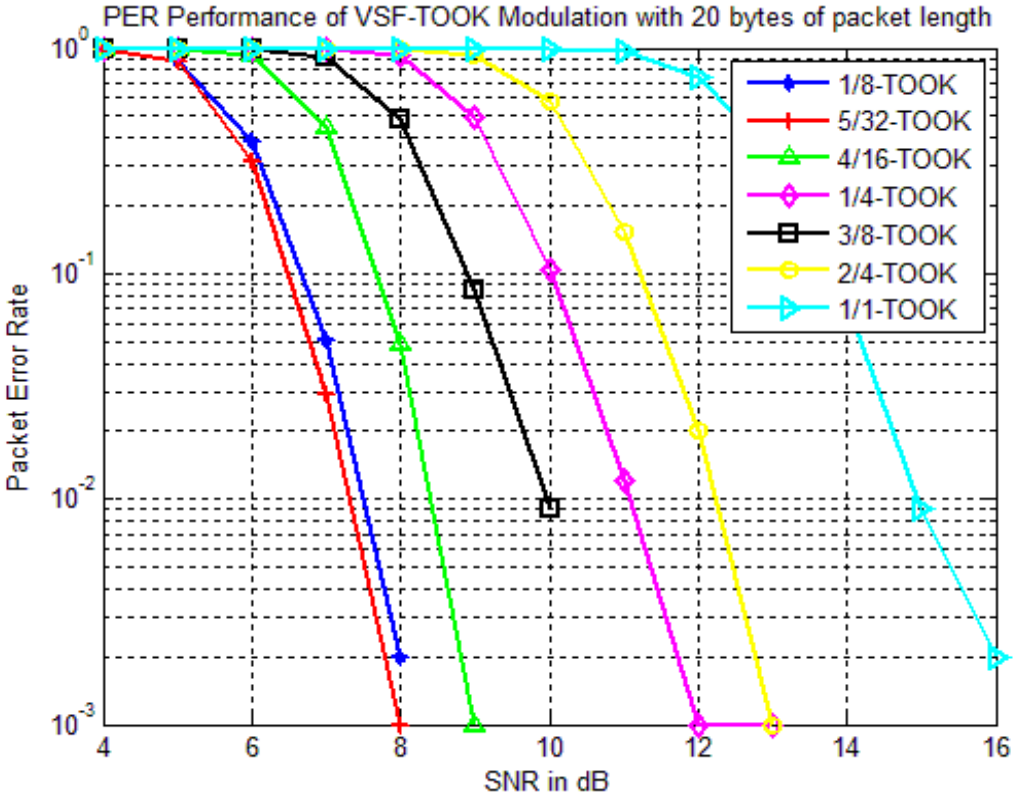

Figure 6.1-1 Packet error rate (PER) vs. SNR curves under AWGN for the non-coherent reception.

Table 6.1-1 List of required SNRs for different modulations to meet a target PER of 1%.

Modulation Scheme	SNR (dB) @ PER=1%.
1-TOOK	15
2/4-TOOK	12
1/4-TOOK	11
3/8-TOOK	10
4/16-TOOK	8.5
1/8-TOOK	7.5
5/32-TOOK	7.25

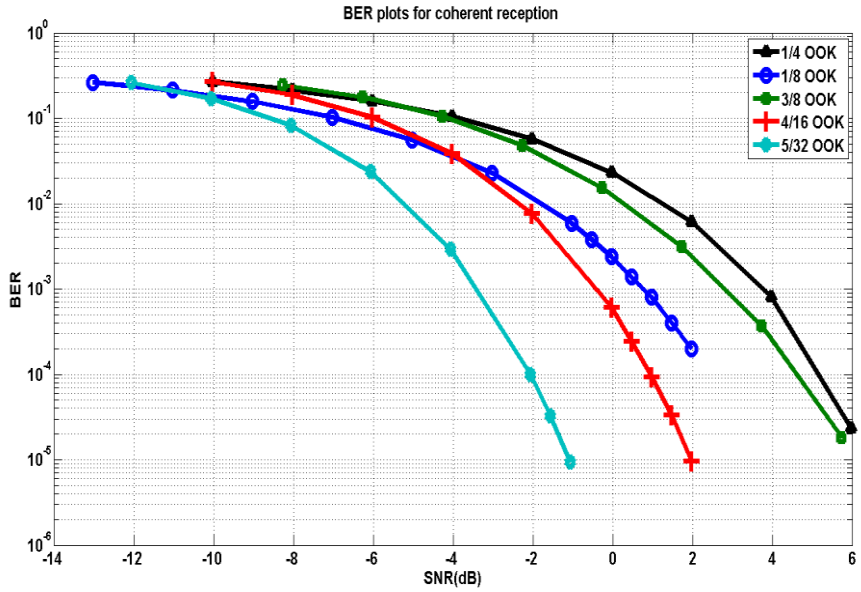

Figure 6.1-2 Bit error rate (BER) vs. SNR curves for coherent reception in AWGN channel.

6.2 Performance in AWGN with Homogeneous Interference

We evaluated the performance of our system in presence of homogenous interference. The two standard cases are considered. First one is the adjacent channel interference (ACI), where the interference is due to the transmissions from the adjacent channel, i.e., the channel spaced 5 MHz apart from the operating center frequency. Second scenario is the alternate channel interference (ALCI) where the interference is due to the transmissions from the alternate channel, i.e., channel spaced 10 MHz apart from the operating center frequency. For simulation purposes, the interference patterns were generated by simulating the transmitter using pseudorandom message bits. The performance evaluation considers the combined performance of both synchronization as well as demodulation blocks. The following plots show the performance of various modulation schemes in different interference scenarios.

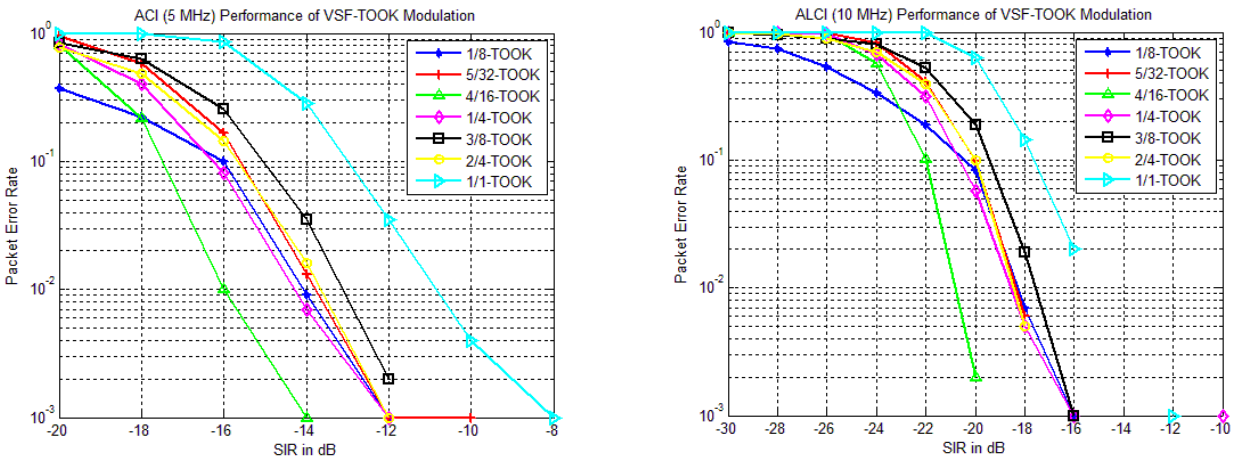

Figure 6.2-2 Performance curves under AWGN corrupted with a) Adjacent channel interference (ACI); b) Alternate channel interference (ALCI).

Table 6.2-1 Out of Band Interference Rejection capability

Interference Rejection	Value (dB)
Adjacent Channel Rejection	13
Alternate Channel Rejection	20

6.3 Synchronization Performance of the Preambles

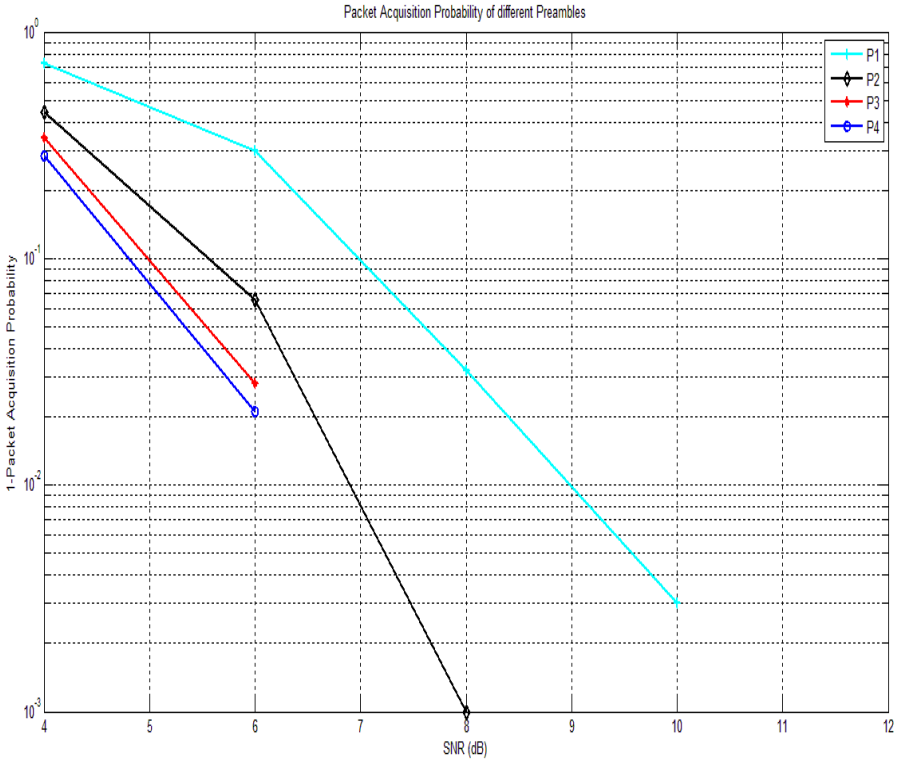

Figure 6.3-1 Packet acquisition probability vs. SNR curves for different preambles.

7 Link Budget Calculations

We present link-budget calculations for free-space and indoor environments.

Table 6.3-1 Link budget table for free-space propagation environment.

Parameter	Value for D7 (1/8-TOOK)	Value for D5 (4/16-TOOK)	Value for D1 (1/1-TOOK)
Transmitter Budget			
Payload Data Rate (R_b) in kbps	101.2	202.4	809.5
Distance (d) in m	30	30	30
Bandwidth (B) in MHz	1	1	1
Tx Antenna Gain (G_T) in dB	0	0	0
Center Frequency (F_C) in MHz	2450	2450	2450
Average Transmit Power (P_t) in dBm	-5	-5	-5
Receiver Budget			
Path Loss at distance d m	69.77	69.77	69.77
Rx Antenna Gain (G_R) in dB	0	0	0
Received Power (P_{rx}) in dBm	-74.77	-74.77	-74.77
Average Noise Per bit (N) in dBm	-123.94	-120.93	-114.91
System Noise Figure (NF) in dB	10	10	10
Minimum Eb/No Required in dB	14	14.5	16
Implementation Loss (I) in dB	3	3	3
System Performance			
Link Margin (LI) in dB	22.17	18.66	11.14
Receiver Sensitivity (S) in dBm	-96.94	-93.43	-85.91

Table 6.3-2 Link budget table under indoor environment.

Parameter	Value for D7 (1/8- TOOK)	Value for D5 (4/16-TOOK)	Value for D1 (1/1-TOOK)
Transmitter Budget			
Payload Data Rate (R_b) in kbps	101.2	202.4	809.5
Distance (d) in m	10	10	10
Bandwidth (B) in MHz	1	1	1
Tx Antenna Gain (G_T) in dB	0	0	0
Center Frequency (F_C) in MHz	2450	2450	2450
Average Transmit Power (P_t) in dBm	-5	-5	-5
Receiver Budget			
Path Loss at distance d m	69.6	69.6	69.6
Rx Antenna Gain (G_R) in dB	0	0	0
Received Power (P_{rx}) in dBm	-74.6	-74.6	-74.6
Average Noise Per bit (N) in dBm	-123.94	-120.93	-114.91
System Noise Figure (NF) in dB	10	10	10
Minimum Eb/No Required in dB	14	14.5	16
Implementation Loss (I) in dB	3	3	3
System Performance			
Link Margin (LI) in dB	22.34	18.83	11.31
Receiver Sensitivity (S) in dBm	-96.94	-93.43	-85.91

8 Power Consumption Table

The power consumption of the transmitter at -5 dBm EIRP is around 5 mW. The power consumption of the receiver is less than 4 mW and is measured at 3 dB above receiver sensitivity. The power consumption is measured both at the transmitter and at the receiver with ¼-TOOK modulation scheme with a packet size of 20 bytes.

Table 6.3-1 Power consumption table: i. Transmitter ii. Receiver.

Tx Component	Power (μW) @ -5 dBm
Baseband	1000
VCO	322
Power Amplifier	2982
PLL + Freq Synthesizer	1000
Total	5304

Rx Component	Power (μW)
LNA+SRO	638
ED+VGA	33
ADC (8 bit)	7.5
Baseband	1500
PLL + Freq Synthesizer	1000
Total	3178.5

9 Summary

Samsung's PHY proposal to IEEE 802.15.4q amendment is presented in this document. The transmission protocol, receiver architecture and performance results for the proposed modulation schemes are described. The proposed protocol offers data rates scalable from 100 kbps to 870 kbps. The applicability of the protocol to both coherent and non-coherent receiver architectures is demonstrated. Link budget calculations for 30 m range are provided for both free-space and indoor propagation scenarios. The tabulated power consumption values, both at the transmitter and at the receiver, are less than 15 mW, in conformance with the technical guidance document.

10 Bibliography

[1] S. Lin, D. J. Costello, Error control coding., Englewood Cliffs, NJ.: Prentice-hall, 2004.