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Submission Title: The Next Frontier for Circuit Designers: CMOS THz Systems

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Abstract: There has been a growing interest in mm-wave and Terahertz frequencies for communication, imaging, and sensing applications. In this talk, we will look into recent advances in CMOS implementation of various building blocks. First, we show how to implement mW-level signals up to 500GHz. Then we show different amplifiers as well as two transmitters at 260GHz and 350GHz.

Purpose: Information to IEEE 802.15 IG THz

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The Next Frontier for Circuit Designers: CMOS THz Systems



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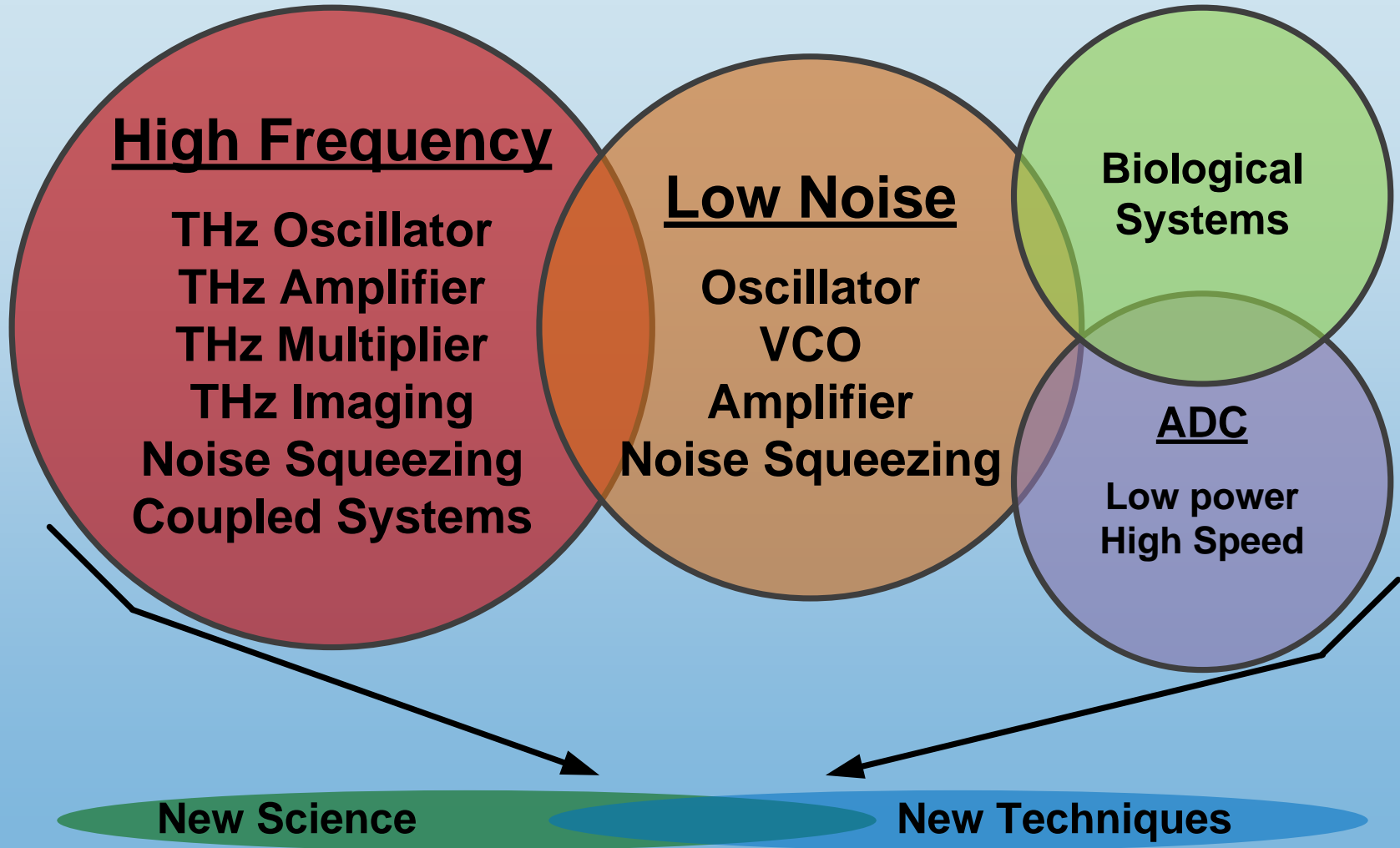
November 2012

Acknowledgement



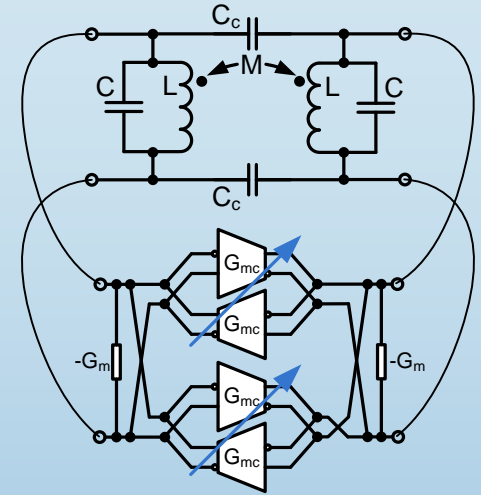
- The people who actually make it happen!

Our Research



Other Projects

- Low phase noise oscillators:
 - Dual mode,
 - Quadrature.
- Wideband low phase noise VCO:
 - 2.4GHz – 5.6GHz that satisfies ALL cellular specifications
- Low power, high speed ADC
 - 8GS/sec, 4b with 32mW
 - 1.2GS/sec, 4b with 2mW
- Narrow pulse generation on CMOS
 - 1.6ps pulse on standard 65nm CMOS
- A 260GHz Amplifier
 - 9.2dB gain
 - -4dBm Psat



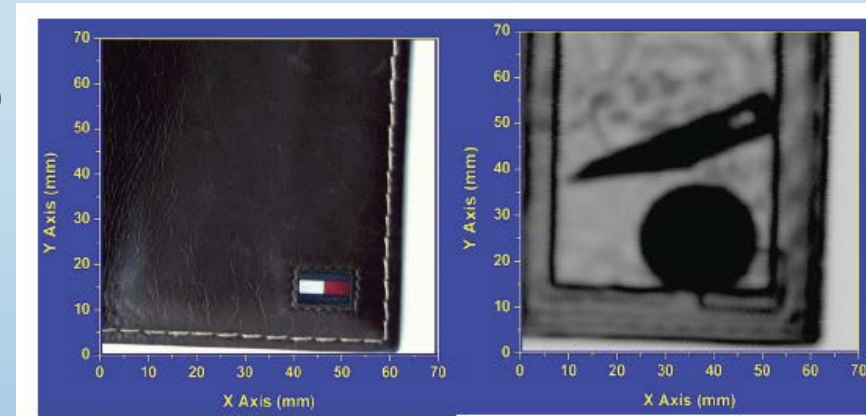
Process	65nm Low Power CMOS					
Vdd (V)	VCO Core: 0.6 V; Digital Control: 1.2V					
Tuning Range	2.48GHz~5.62GHz continuous tuning					
Chip Area	0.294 mm ²					
Phase Noise (dBc/Hz)	Odd Mode			Even Mode		
	Low	Middle	High	Low	Middle	High
Freq (GHz)	2.517	3.696	3.880	3.312	4.463	5.515
Idc (mA)	23.61	17.43	16.49	25.27	20.97	16.43
PN@100kHz	-101.1	-96.44	-94.42	-105.3	-96.03	-89.3
PN@300kHz	-114.4	-112.7	-112.3	-117.5	-110.3	-105.1
PN@1MHz	-128.6	-128.3	-128.3	-129.5	-124.8	-121.3
PN@3MHz	-139.8	-137.1	-137.2	-139.5	-134.6	-130.7
PN@10MHz	-151.9	-151.4	-151.9	-150.2	-147.6	-145.8
PN@20MHz	-156.8	-156.6	-156.7	-155.5	-153.1	-151.7
FoM@10MHz	189.4	192.5	193.7	188.8	189.6	190.7

Outline

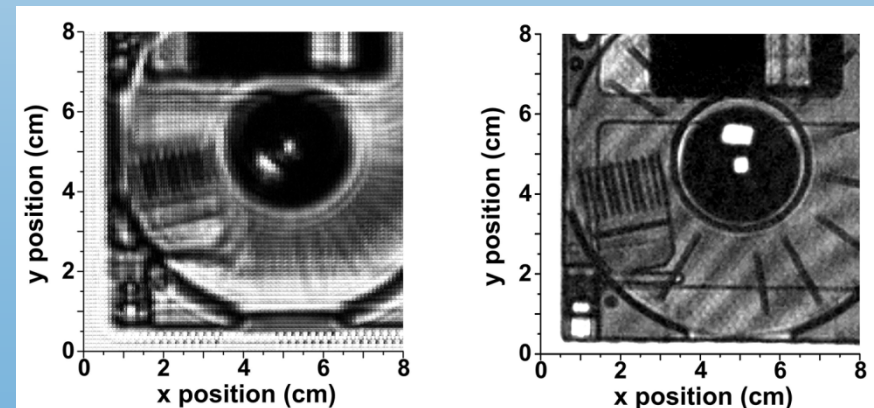
- Motivation
- Terahertz Frequency Multipliers
- High Power Terahertz Oscillator Design
- A High Power THz VCO
- THz Radiator Arrays
- Conclusion

Application of THz Systems

- Imaging (e.g., detection of concealed weapon, cancer diagnosis, and semiconductor wafer inspection)
- Compact range radars
- High data rate communication (e.g., 100 Gbps)



High power is needed for these applications



Application of THz Systems

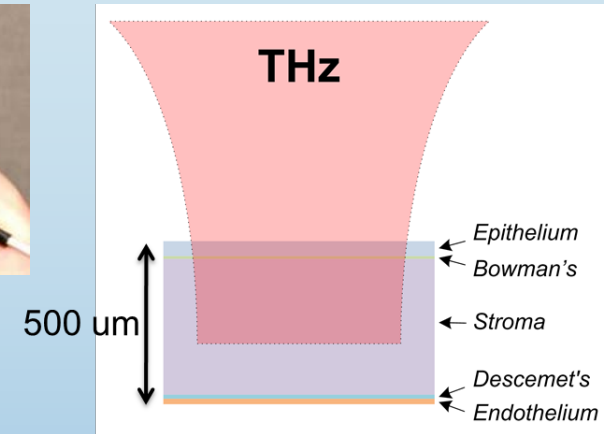
- Skin cancer detection:
 - Large tumors can extend 15mm beyond the visible border
 - Significant number occur on face
 - Existing techniques can have high false negative rates and is time and personnel intensive
 - At 700GHz, we can have 40 μ m depth resolution and 1mm penetration
- Tooth decay:
 - Small cavities are hard to detect
 - Earlier detection equates to better outcomes
 - X-ray has limited resolution

Application of THz Systems

- Corneal hydration sensing:

- Diseases and procedures:

- Corneal Graft surgery
- Fuch's Dystrophy
- Keratoconus
- Glaucoma
- LASIK



- Current methods based on ultrasonic or optical thickness measurements

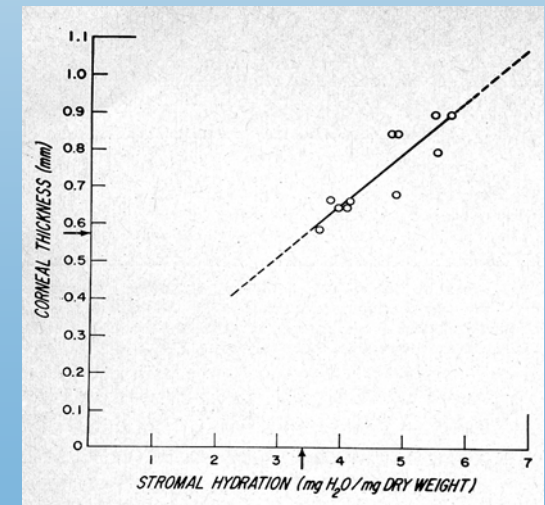
- Thickness measurement very accurate ($\sim 9 \mu\text{m}$)

- Mapping from thickness to hydration very inaccurate ($\pm 5\%$ by volume)

- Physiologic variation confounds measurement

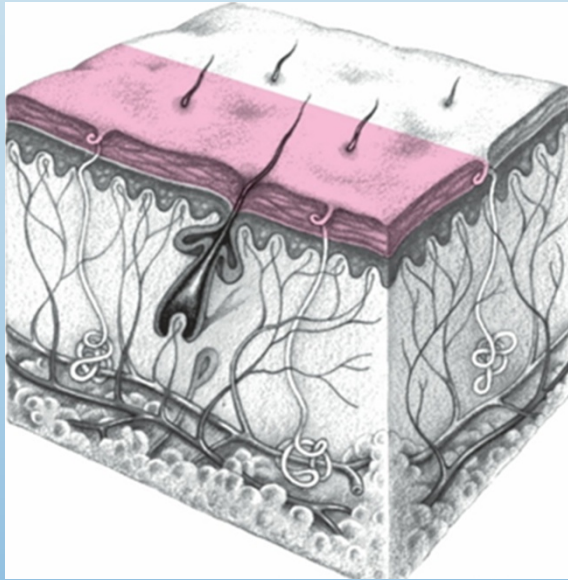
- Listed diseases and procedures need hydration sensitivity in the range of 0.8% - 3% depending on application

- THz imaging results in better than 0.2% sensitivity

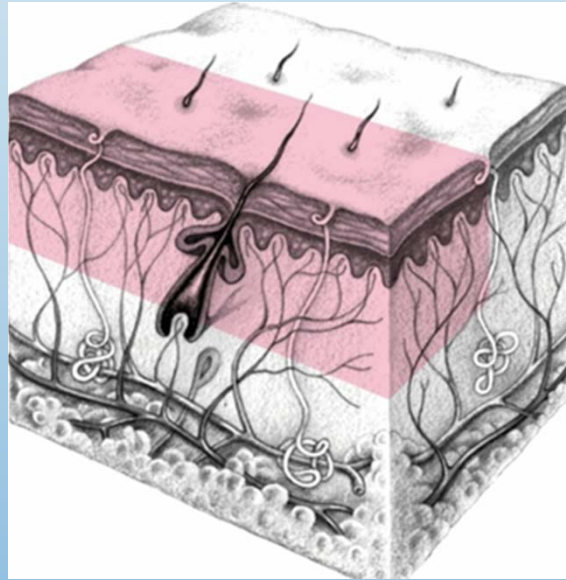


Application of THz Systems

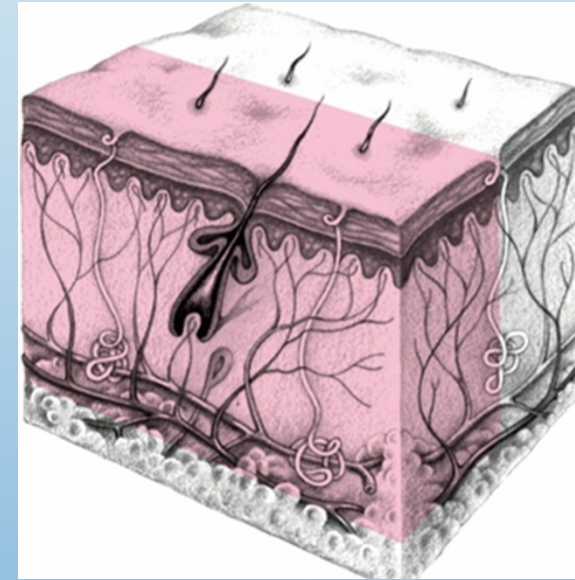
Partial (superficial)



Deep Partial



Full

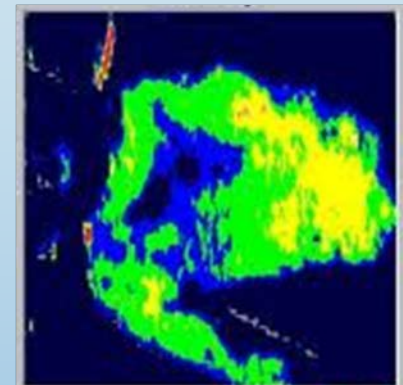


No Surgery

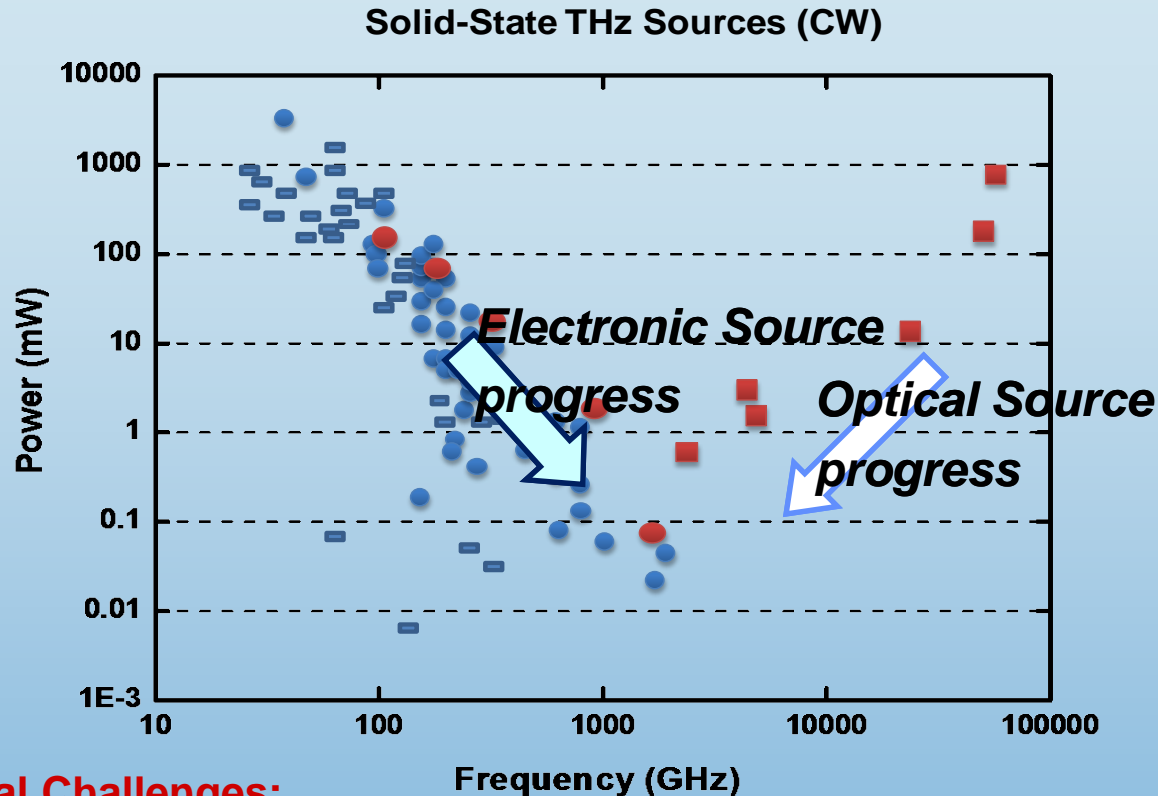
Surgery

Application of THz Systems

- Current clinical methods rely on visual and tactile assessment of burned skin
- Current imaging methods lack dynamic range for margin detection
 - Laser Doppler Imaging
 - Vital Dyes
 - PS-OCT
 - Thermal Imaging
- THz imaging results in mm-resolution detection.



Challenge



Fundamental Challenges:

- Transistors offer no power gain above f_{max}
- Limited power efficiency of devices
- Limited break down voltage
- Quality factor of passives is low

High power signal generation is the main challenge in realizing CMOS THz systems.

Terahertz Electronic Sources

- Travelling electron beams

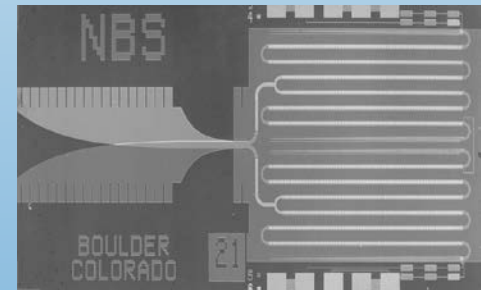
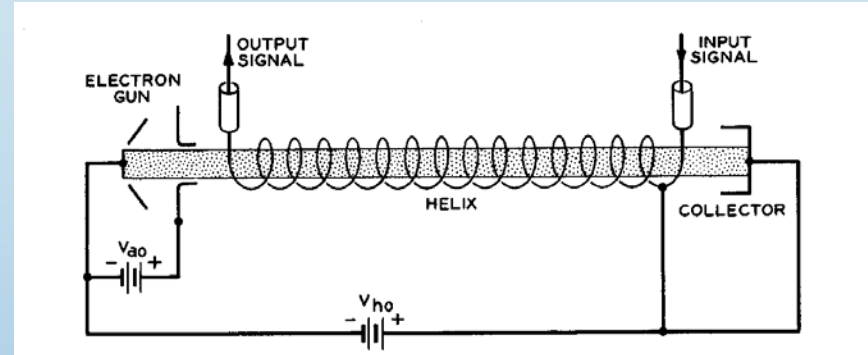
- Example: BWO
- Up to 1 mW around 1 THz
- Very bulky and expensive

- Josephson arrays

- Quantum tunneling in superconductors
- Cryogenic temperatures
- $< 1\mu\text{W}$ power levels

- Solid-state devices

- Limited by electron scattering
- InP devices: 100 μW to 1 mW around 400 GHz



Solid-State Devices for Terahertz

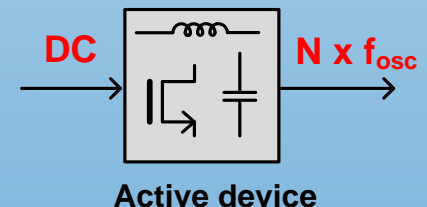
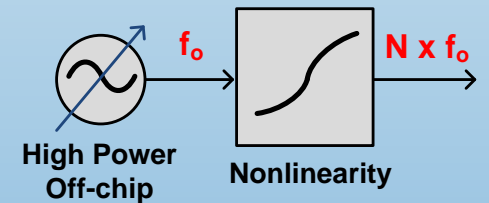
- Diodes (Gunn, IMPATT, Tunneling, etc.)
- Compound semiconductor transistors (InP HBT, GaN HEMT, etc.)
 - ✓ Large breakdown voltages (i.e. GaN > 20 V)
 - ✓ High cut-off frequency ($f_{max} \sim 1$ THz)
 - ✗ Expensive material
 - ✗ Not suitable for large scale integration
- CMOS transistors
 - ✓ Cheap and versatile technology
 - ✗ Low supply voltage (~ 1.2 V)
 - ✗ Low cut-off frequency ($f_{max} < 0.25$ THz)



A CMOS Terahertz solution is highly desirable but *challenging*

Signal Generation Above Cut-off

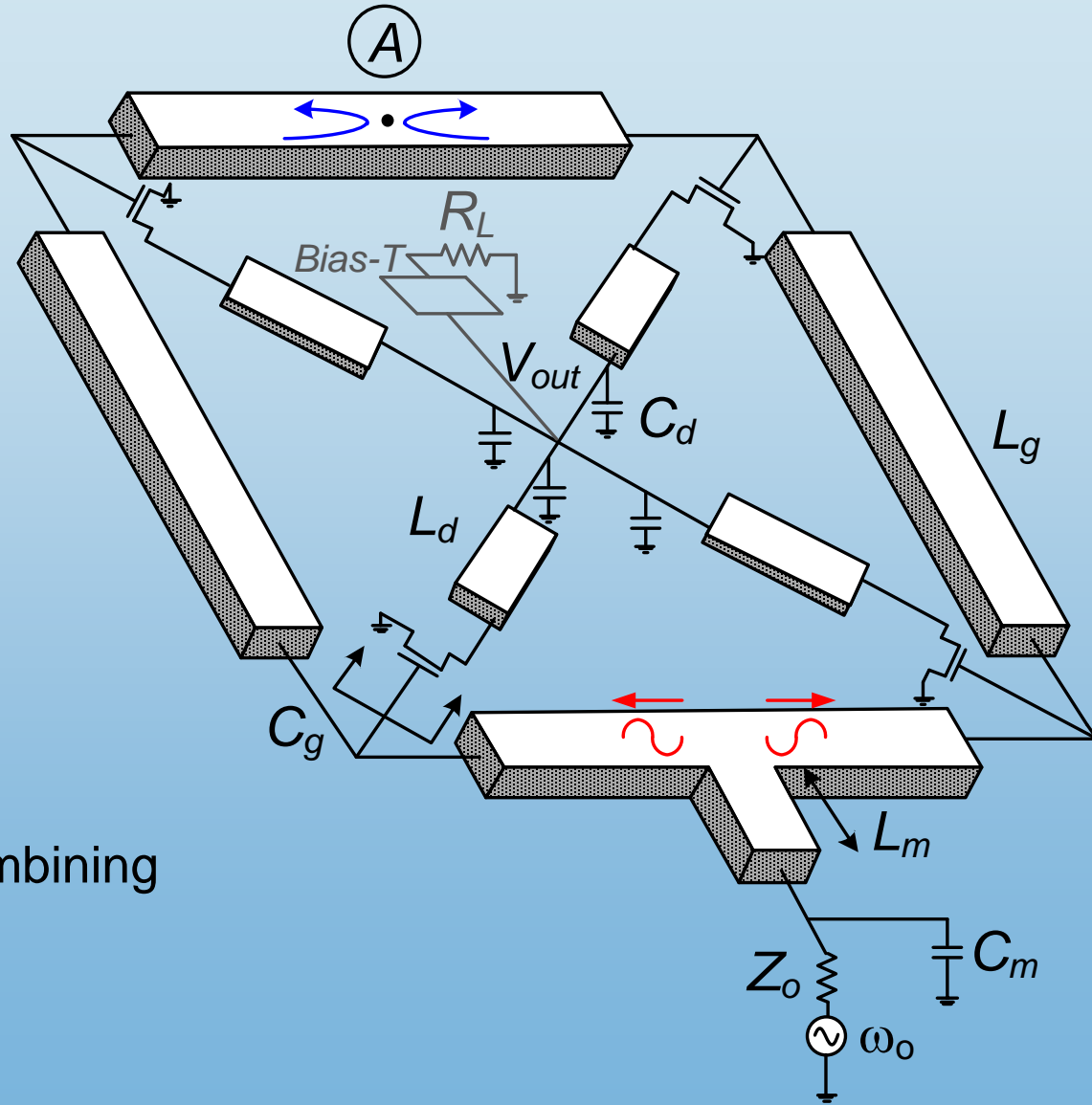
- A nonlinear process generates harmonics of the fundamental frequency above f_{max} .
- Device nonlinearity can be exploited
 - Diodes: IMPATT, Gun, Tunneling, Schottky
 - Transistors: HBT, HEMT, CMOS
- Two approaches:
 - Multiplier : a high power source is normally provided off-chip.
 - Harmonic oscillator : The oscillator is implemented on chip
- On-chip implementation is the ultimate solution



Outline

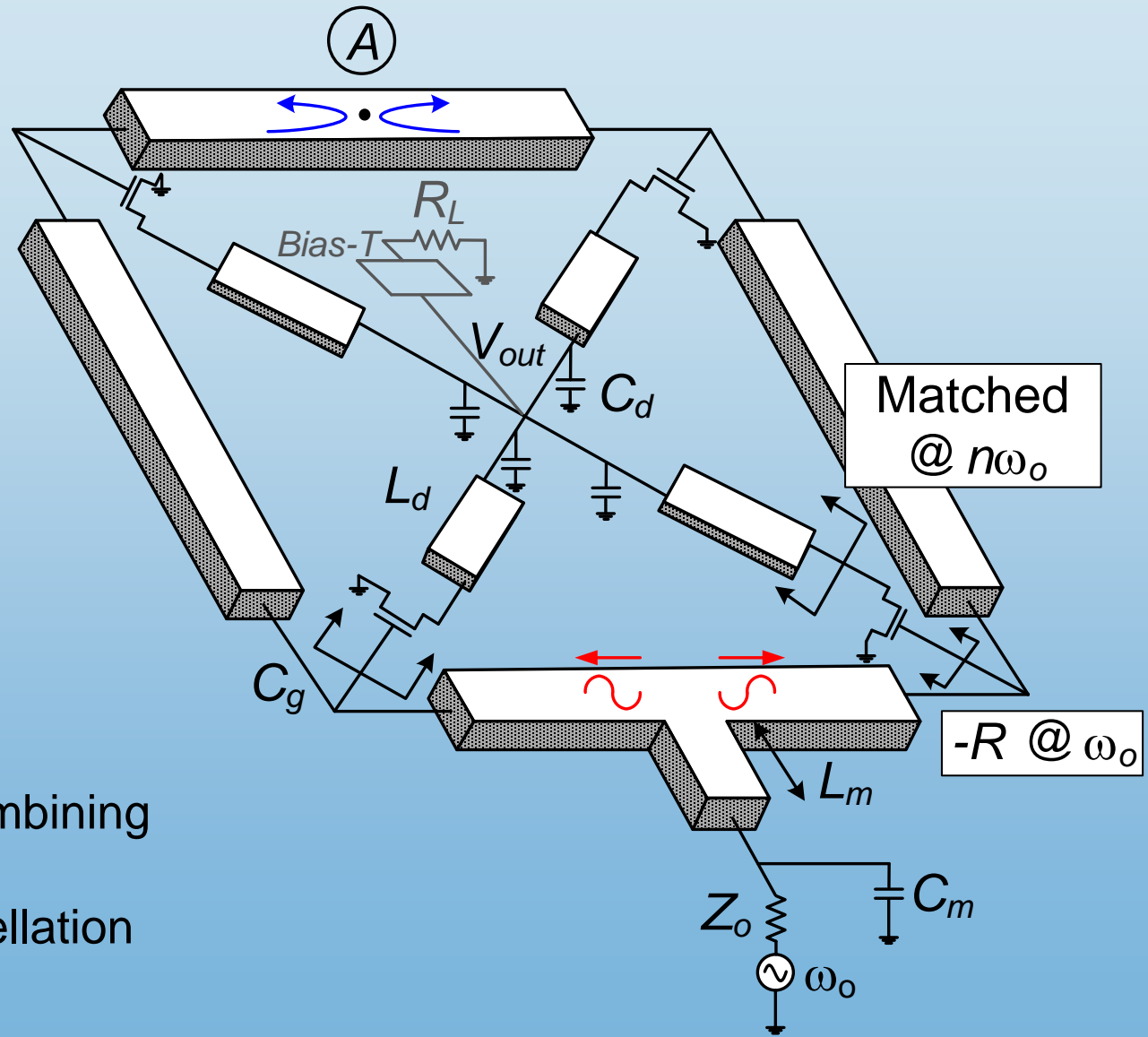
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Basic Idea



- Effective harmonic generation and combining

Basic Idea

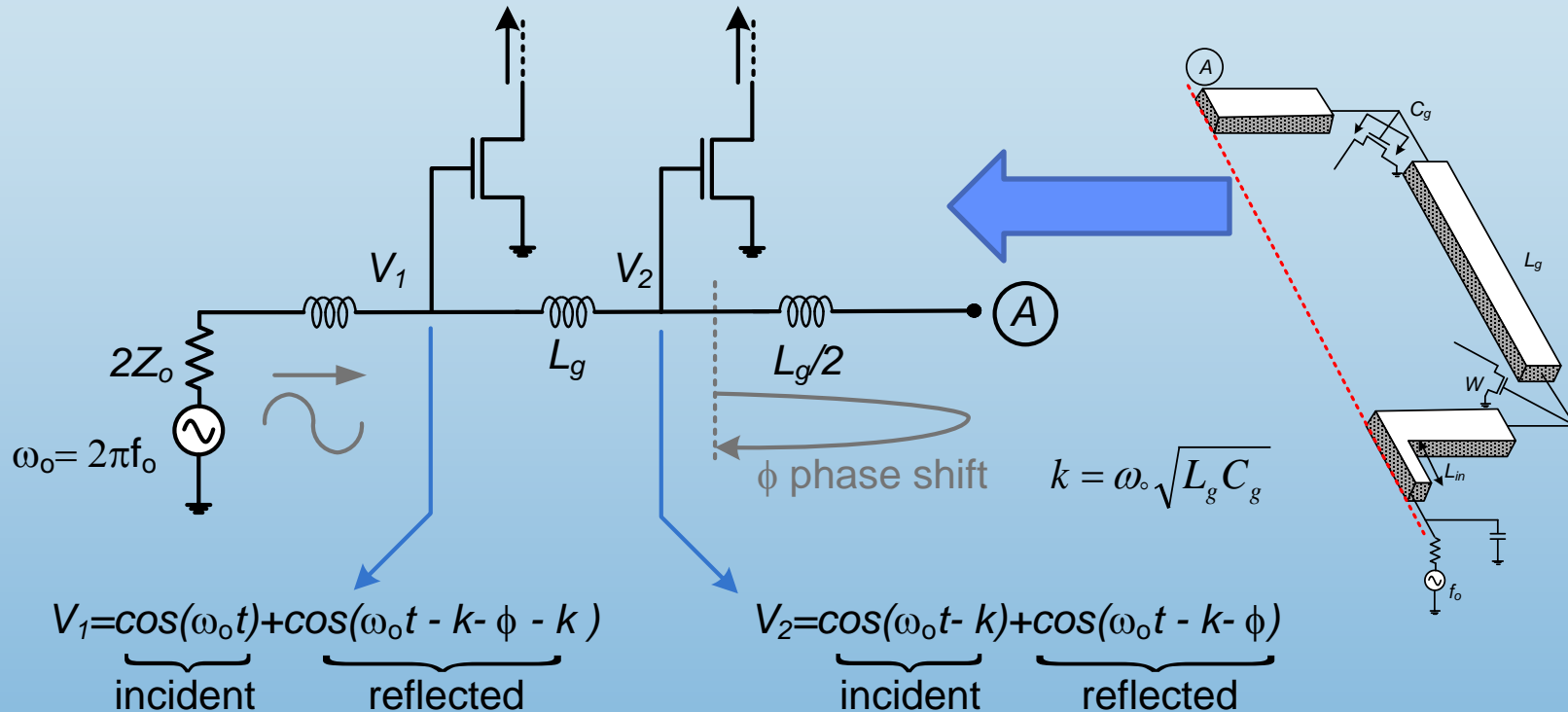


- Effective harmonic generation and combining
- Efficient loss cancellation

Theory

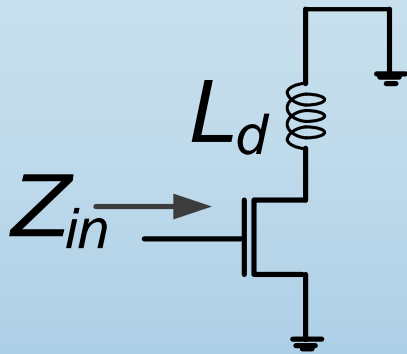
$$I_1 = a_1 V_1 + a_2 V_2^2 = \dots + a_2 \cos(2\omega_0 t - 2k - \phi) + \dots$$

$$I_2 = a_1 V_2 + a_2 V_2^2 = \dots + a_2 \cos(2\omega_0 t - 2k - \phi) + \dots$$



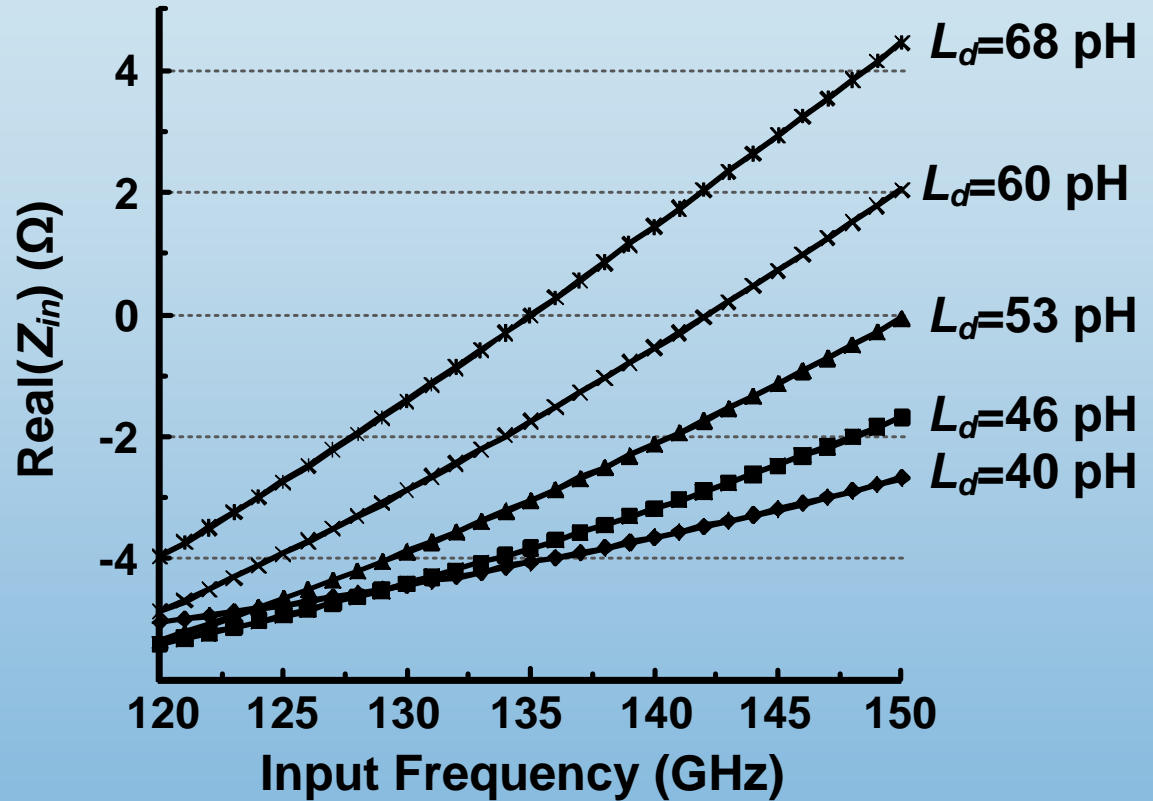
- The second harmonics add in phase at the output
- The basic principle is independent of frequency

Negative Input Impedance



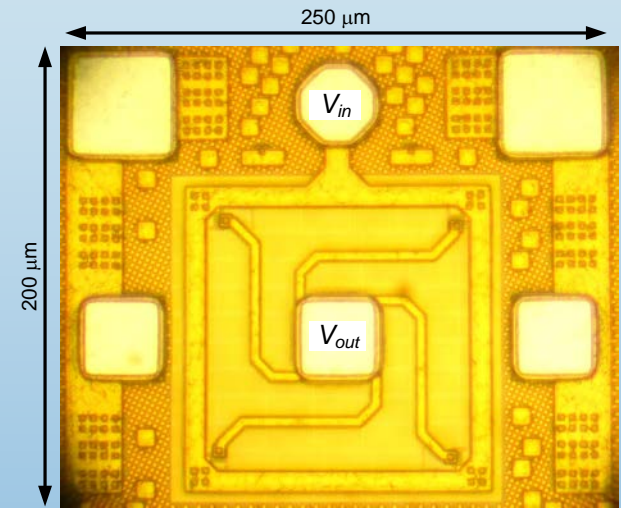
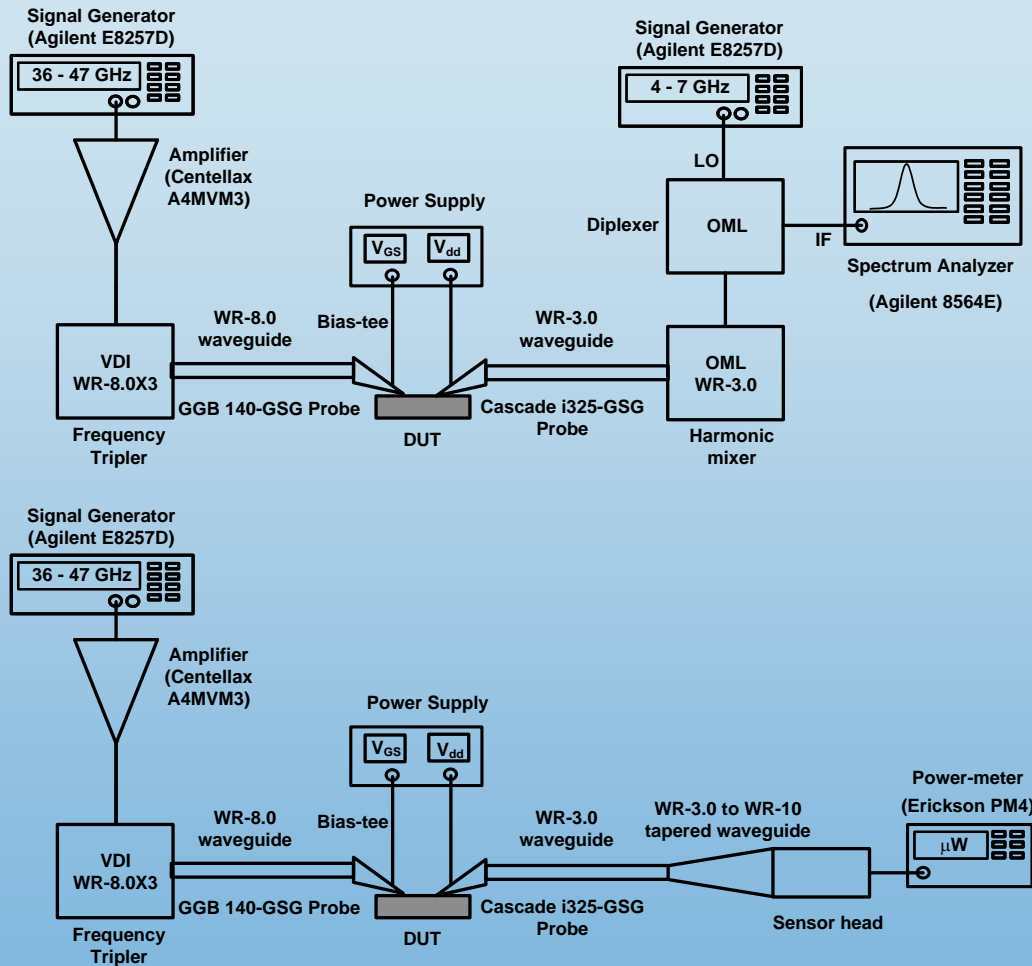
$$L_d \omega_o^2 (C_{gd} + C_{ds} + \frac{C_{gd}}{R_o g_m}) < 1$$

➡ $Real(Z_{in}) < 0$



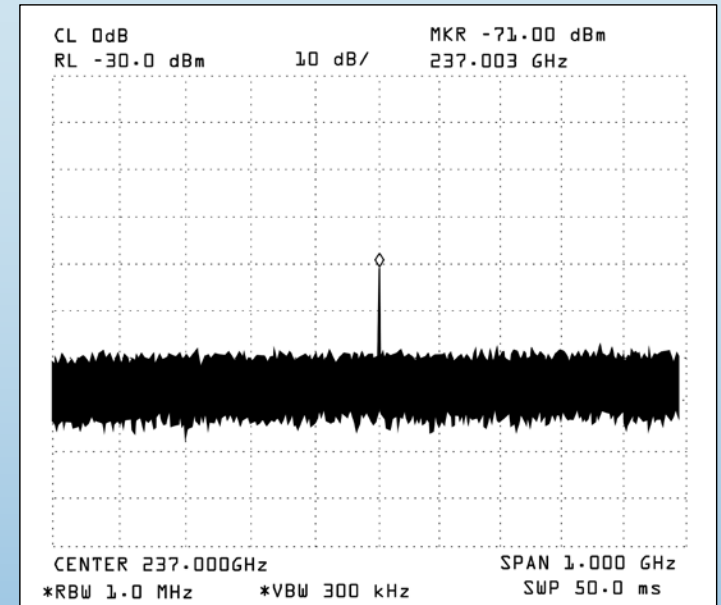
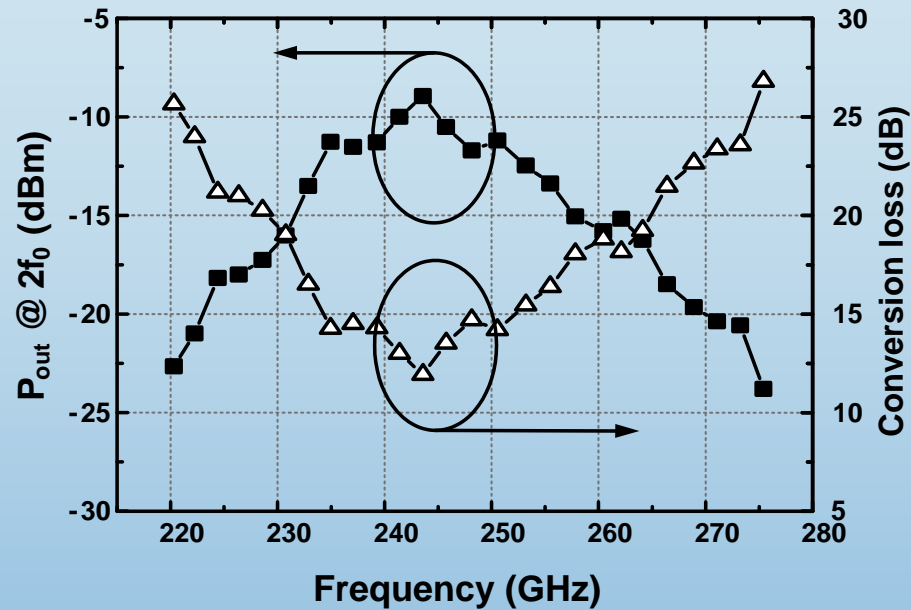
- There is a trade-off between better output matching and higher input voltage swing.

Implementation



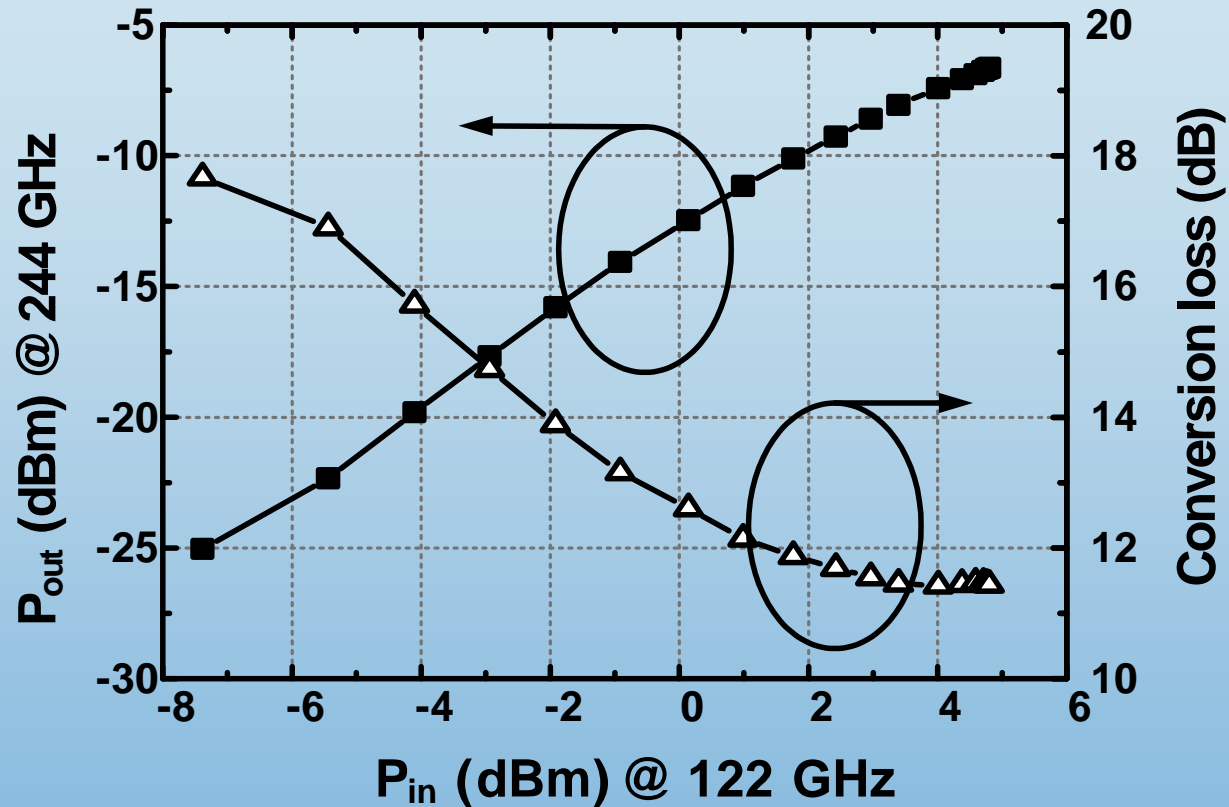
- The power and frequency test setups

Results



- In this case the input power is kept at 3dBm

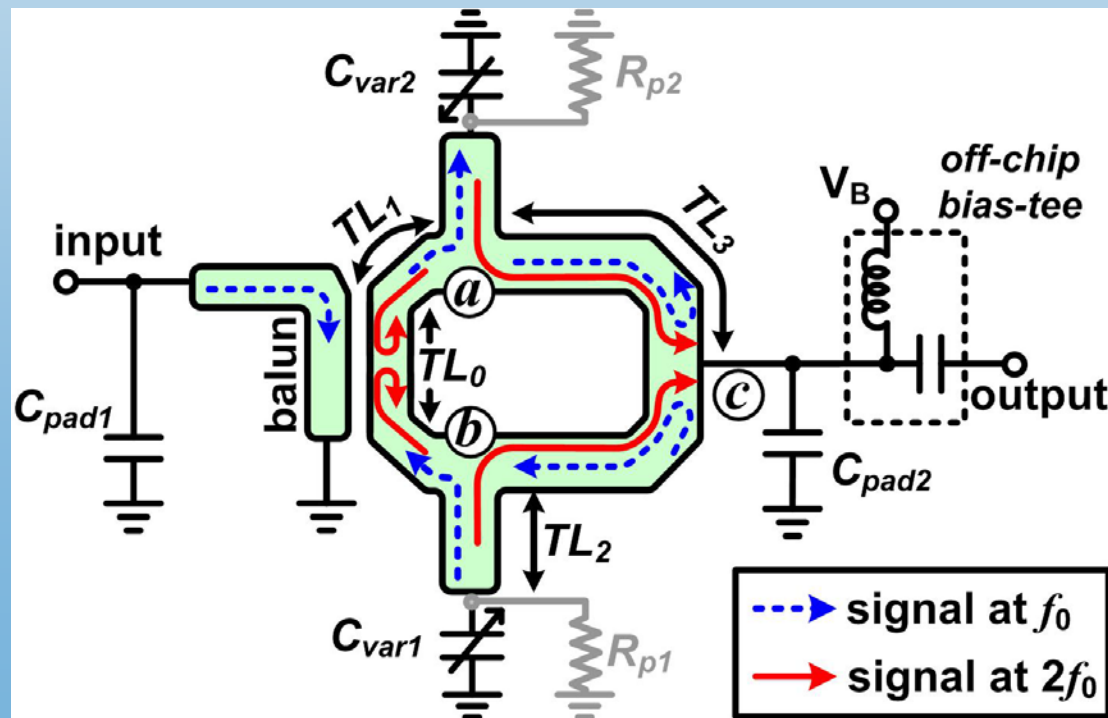
Results



- The output power is not saturated
- A maximum of -6.6dBm is achieved at 244GHz

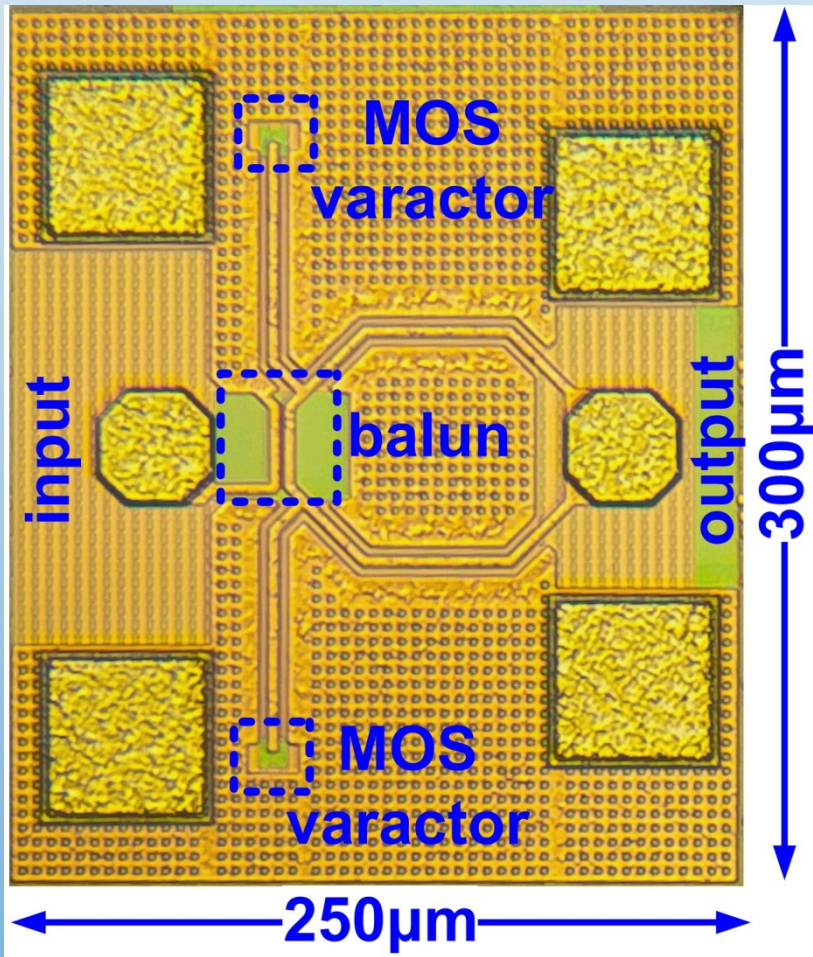
A 480 GHz Doubler

- Main structure: a compact partially-coupled ring
- Simultaneous matching at fundamental (input) and 2nd harmonic (output)

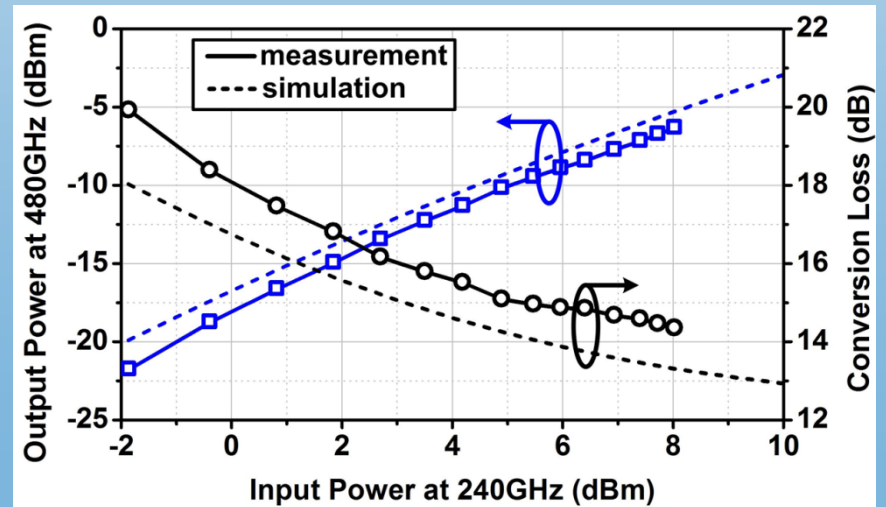
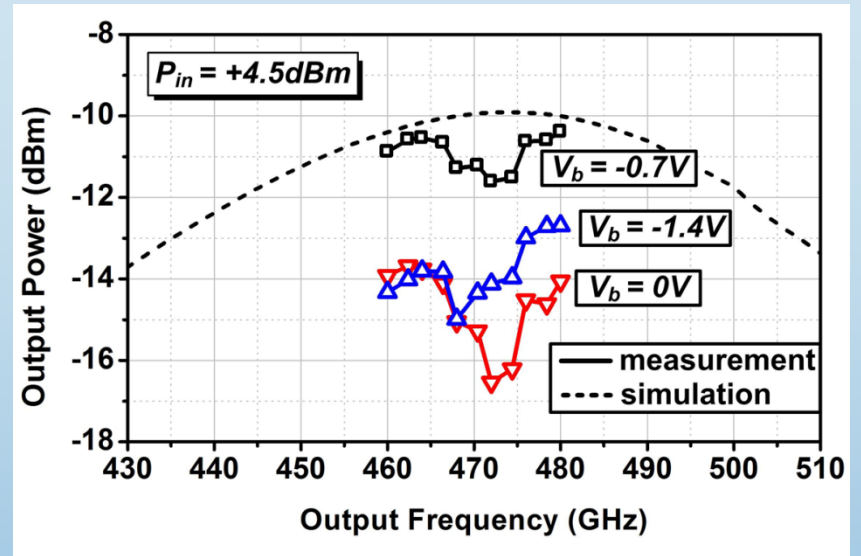


- Pads are part of the input/output matching
- R_{p1} and R_{p2} : leakage paths for accumulative charge to avoid oxide breakdown

Experimental Results



– 65nm Bulk LP CMOS



Outline

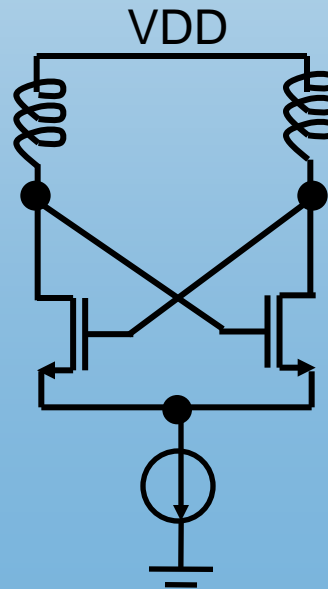
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Fundamental Limit?

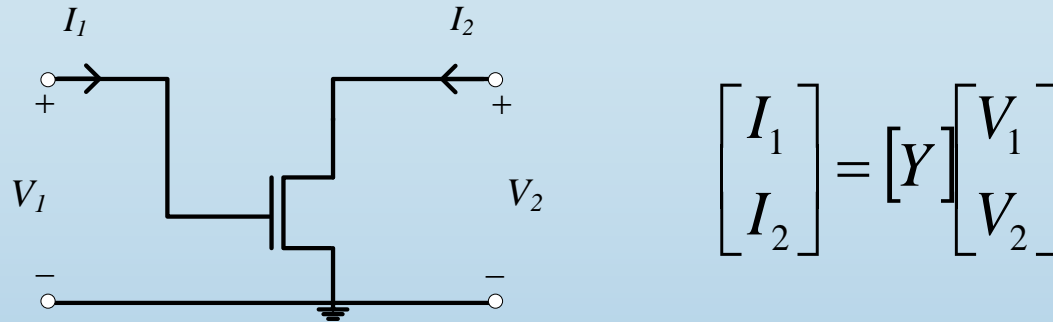
- Most of the fundamental oscillators have the oscillation frequency in the order of the half of the f_{max} of the transistors. Why not higher?
- What is the maximum oscillation frequency of a circuit topology, considering the quality factor of the passive components?
- For a fixed frequency, what is the topology that results in maximum output power?

Fundamental Limit

- Example: IBM 130 nm CMOS process:
 - f_{max} : simulated: 174 GHz
 - f_{max} : measured: ~135 GHz
- Regular Cross-Coupled oscillator:
 - Maximum achievable frequency (simulation): 120 GHz
 - This is with IDEAL inductors!



Activity Condition



- Normalized real power flowing out of the device:

$$\Rightarrow G_m = \frac{P_R}{|V_1||V_2|} = -(A^{-1}G_{11} + AG_{22}) - |Y_{12} + Y_{21}^*| \cos(\angle(Y_{12} + Y_{21}^*) + \varphi)$$

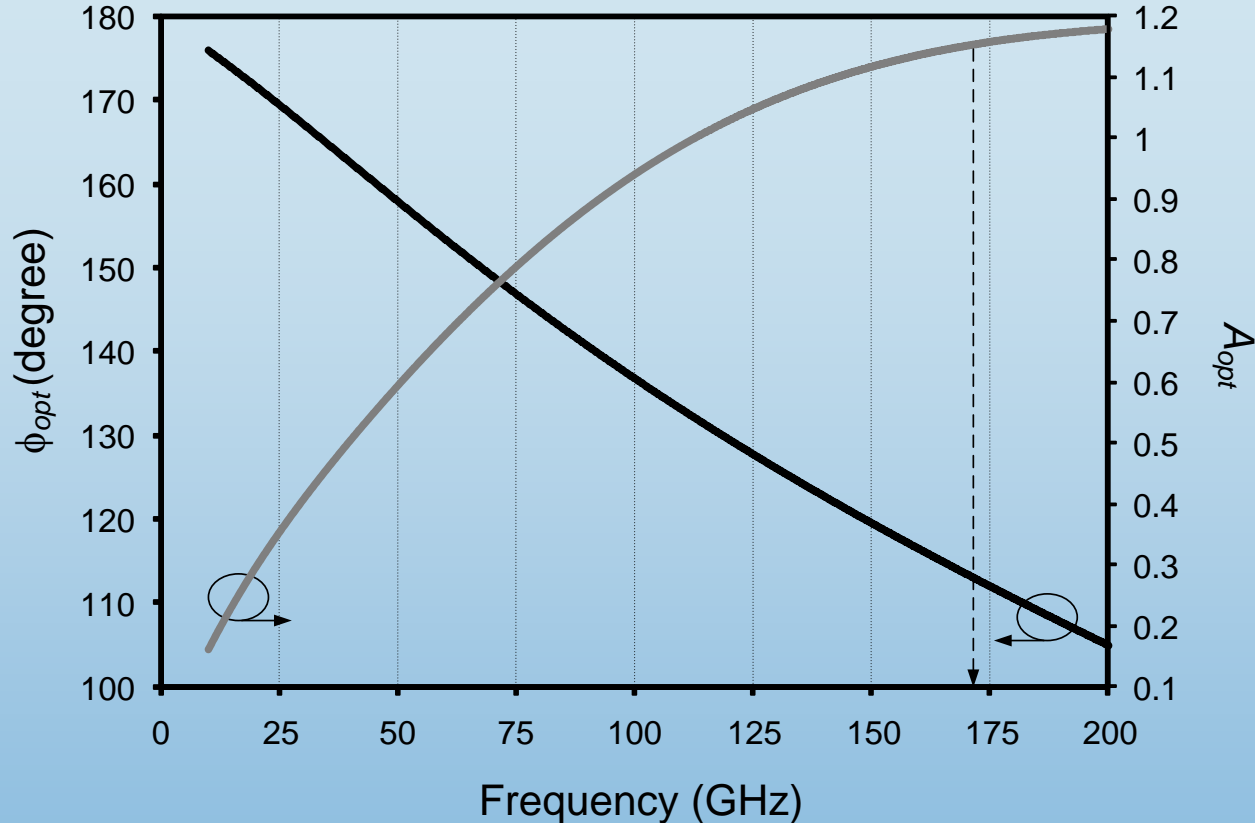
$$G_{11} = \text{real}(Y_{11})$$

$$G_{22} = \text{real}(Y_{22})$$

$$A = \left| \frac{V_2}{V_1} \right| \& \varphi = \angle\left(\frac{V_2}{V_1}\right)$$

- G_m is the maximum conductance that can be placed across the transistor and maintain the oscillation.

Maximum Activity



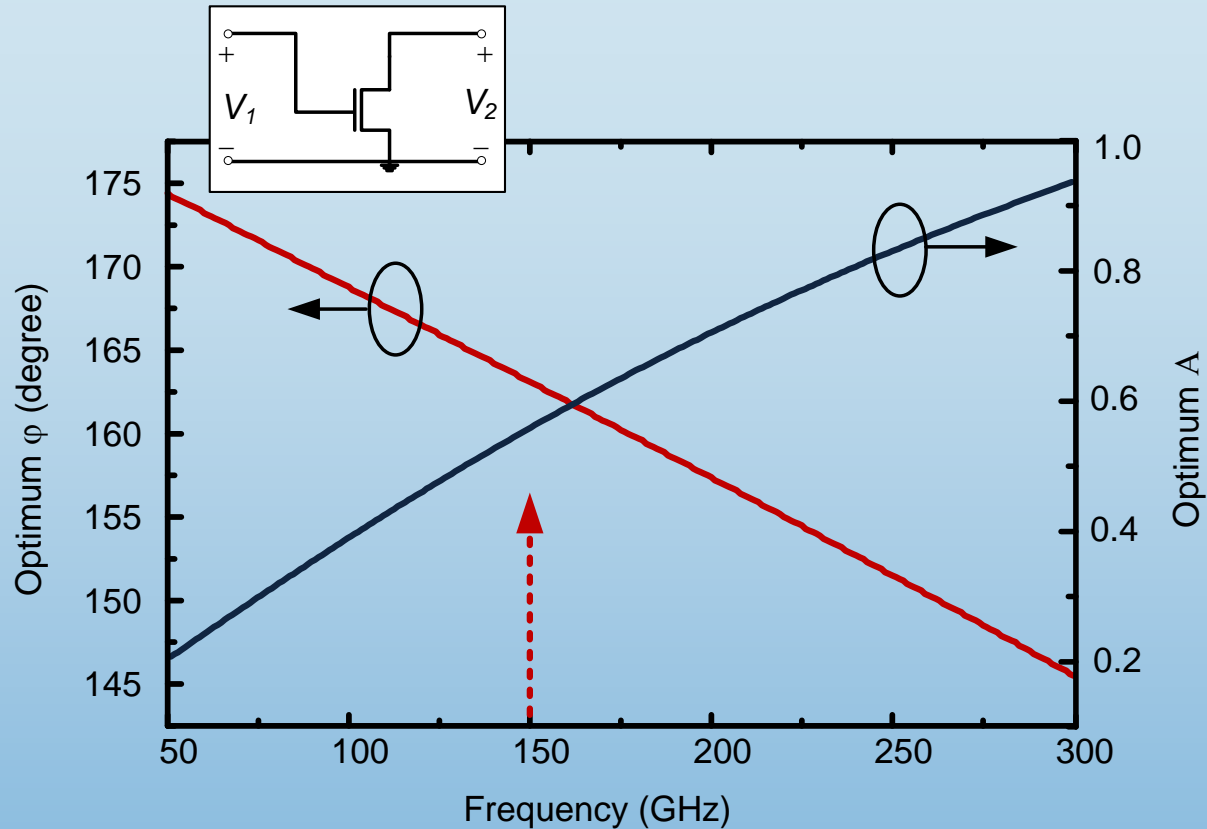
- Optimum gain and phase conditions for maximum generated power (maximum oscillation frequency)

$$\varphi = \varphi_{opt} = (2k + 1)\pi - \angle(Y_{12} + Y_{21}^*) \quad A = A_{opt} = \sqrt{\frac{G_{11}}{G_{22}}}$$

Higher Frequency: Harmonics

- In order to achieve higher frequencies, we need to generate strong harmonics
- This means we should maximize the swing at the fundamental frequency
- It might be better to back off from the maximum possible oscillation frequency to boost the harmonic generation
- We need to maximize “ G_m ”

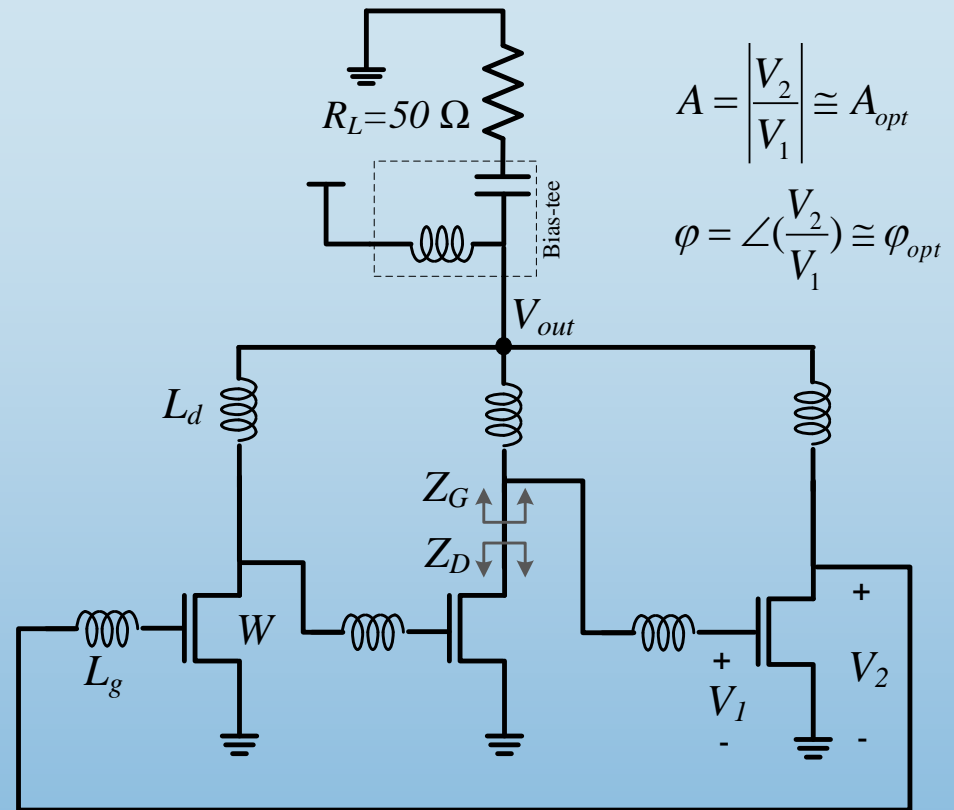
Optimum Conditions



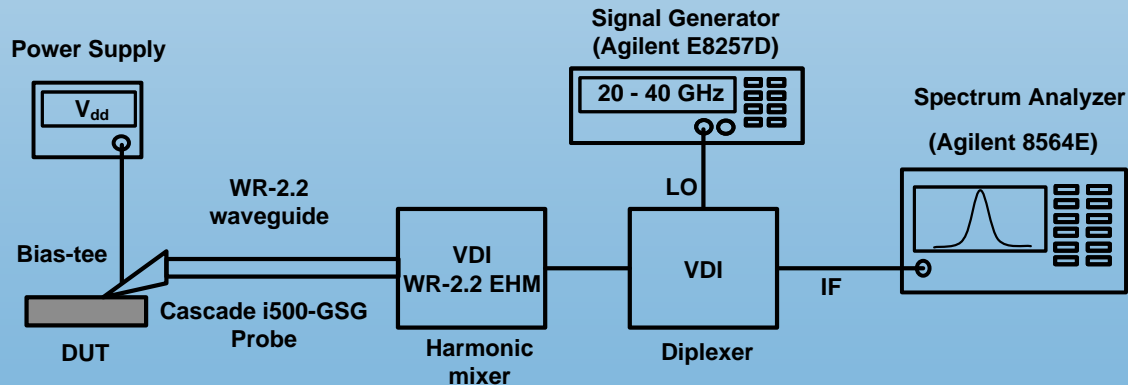
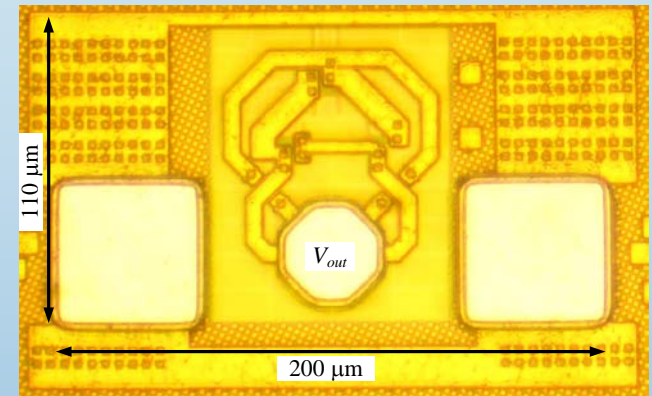
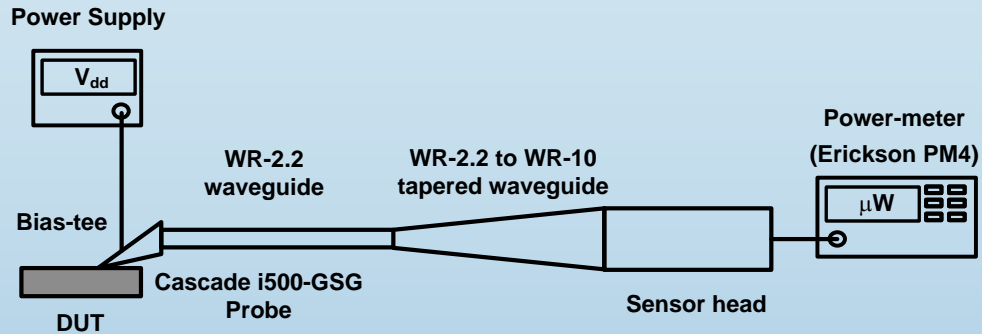
- Optimum phase and voltage conditions in a 65nm process
- Target frequency is 450 GHz

Triple Push Oscillator

- The gate inductor helps with both amplitude and phase conditions:
 - It resonates with C_{gs} to boost the gate-source voltage, resulting in lower A across the device
 - It also delays the voltage to increase the phase shift from 120.

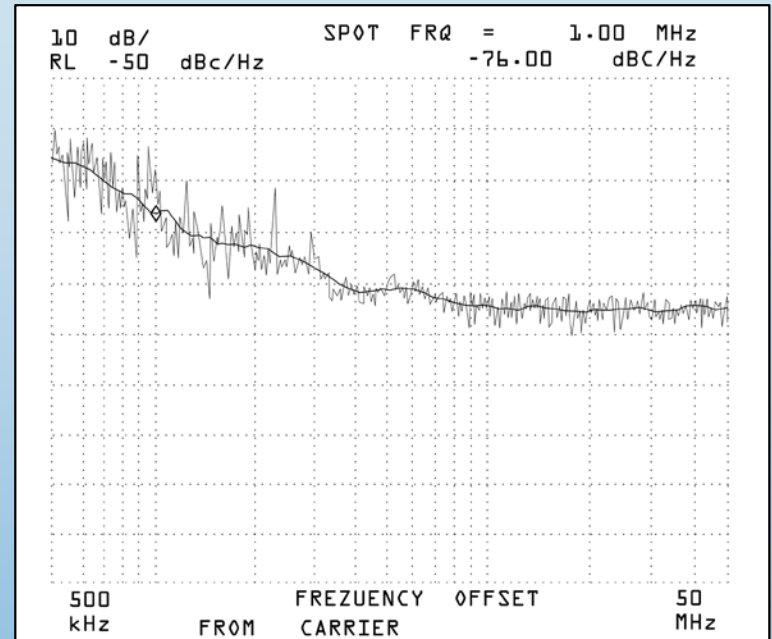
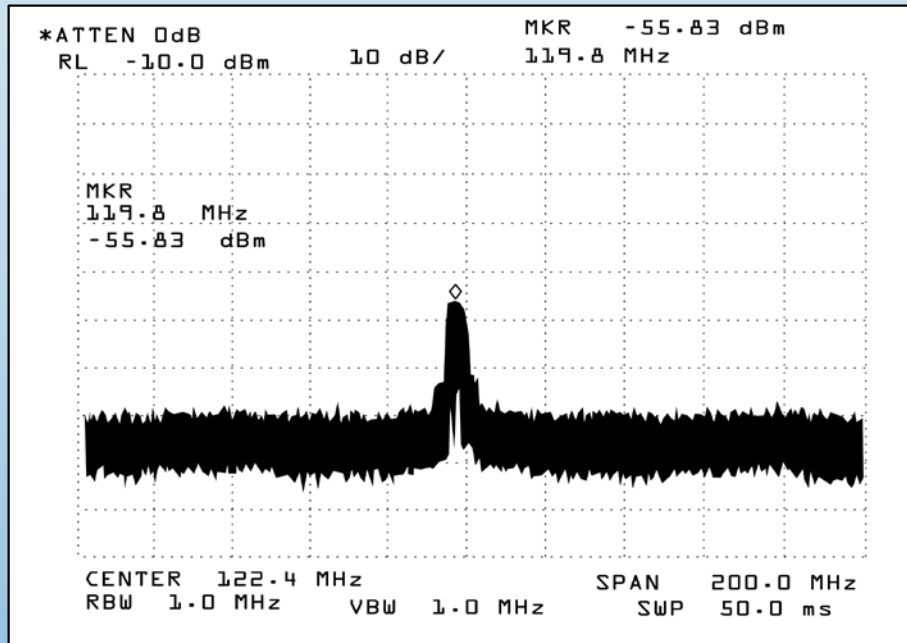


Implementation



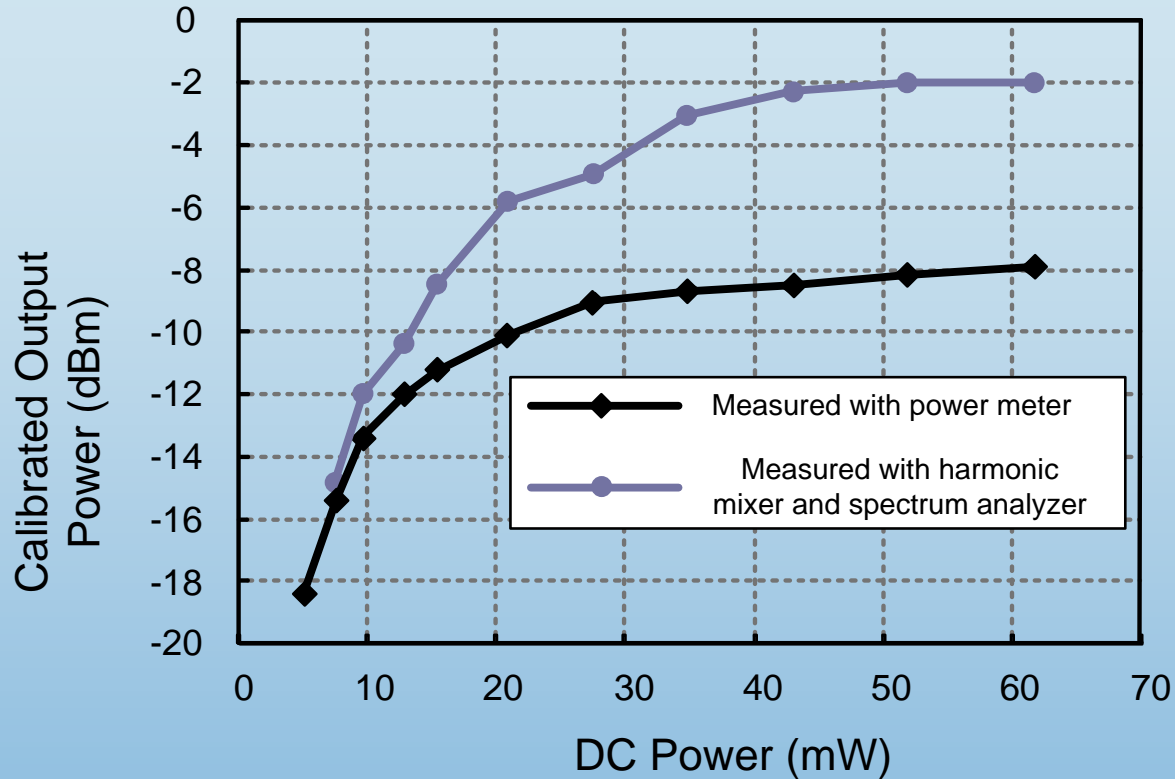
- The power and frequency test setups

Results: Spectrum



- The second harmonic is 15.5dB lower than the third harmonic
- Output frequency is 482GHz

Results: Power



- Measured output power using both setups

Outline

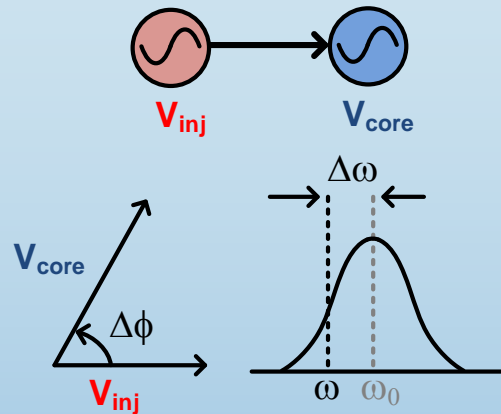
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Challenge: Terahertz VCO

- At mm-wave and terahertz frequencies it is challenging to get high tunability with varactors due to dominance of device parasitics
- Varactors are very lossy at mm-wave and are not desirable in mm-wave and terahertz signal generation

Ref.	Technology	Fundamental (GHz)	Output frequency (GHz)	Power (dBm)	Tunability
JSSC '06	130nm CMOS	102GHz	102 GHz	-25 dBm	0.2%
ISSCC 09	32nm CMOS SOI	102GHz	102GHz	N/A	4.2%
ISSCC `08	45nm CMOS	205GHz	410GHz	-47 dBm	-
ISSCC '11	45nm CMOS	150GHz	300GHz	-19 dBm	-
JSSC '11	65nm CMOS	160GHz	480GHz	-8 dBm	-

Coupling: Adler's Model



Adler's equation*:

$$\frac{d\phi_{core}}{dt} = \omega_0 + K \sin(\phi_{inj} - \phi_{core})$$

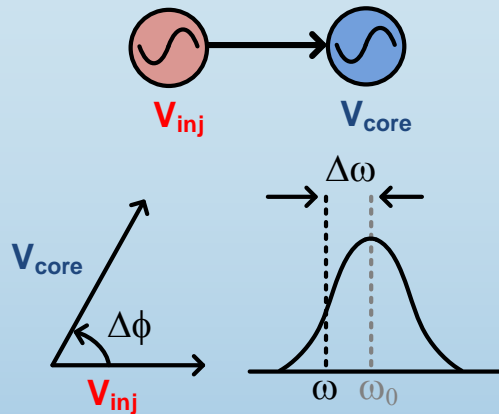
In locking mode:

$$\Delta\phi = \sin^{-1} \left(\frac{\Delta\omega}{K} \right)$$

$$\frac{V_{inj}}{V_{core}} \frac{\omega_0}{2Q}$$

- Adler's model assumes sinusoidal weak coupling.
- A good coupling model around resonance.
- Two oscillators with close center frequencies will frequency lock.
- Depending on the original frequency difference, a phase lag (lead) is developed between the source and core.

Tuning the Locking Frequency



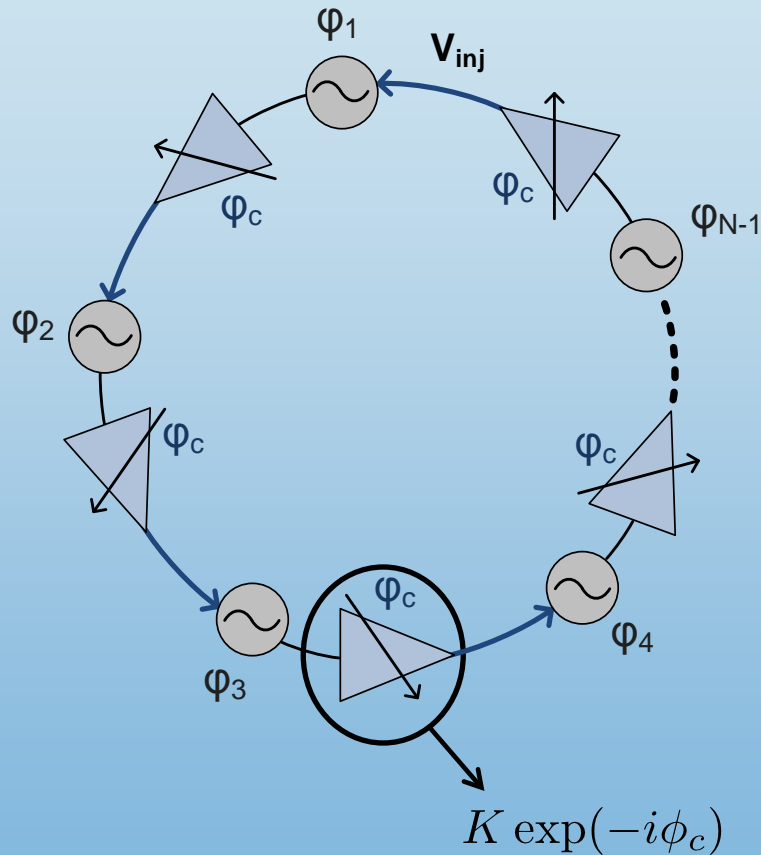
$$\Delta\phi = \sin^{-1} \left(\frac{\Delta\omega}{K} \right)$$



$$\Delta\omega = K \sin(\Delta\phi)$$

- **Observation** : If the locking phase shift is modified, the locking frequency will be different.
- A injection locking scheme enforces the frequency and phase shift.
- We propose a structure with additional degrees of freedom to control the phase shift.

Delay Coupled Oscillators



- N core oscillators coupled in a unidirectional ring
- N oscillators and N coupling blocks are similar
- The tuning mechanism is based on tuning the coupling block
- We assume weak coupling close to resonance

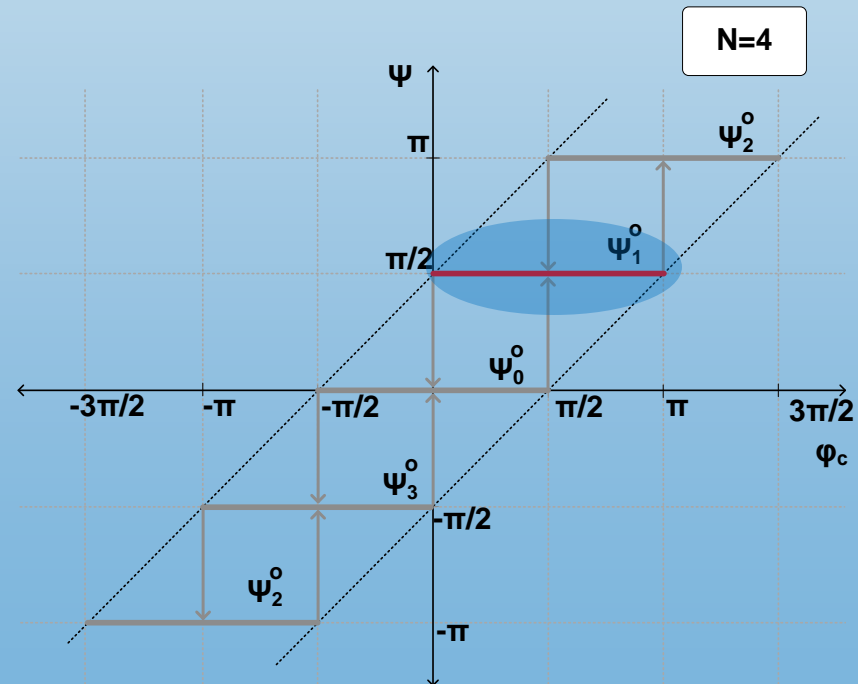
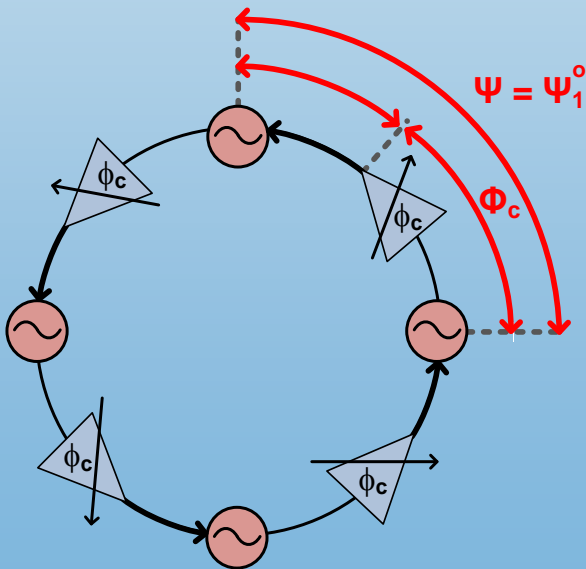
Governing dynamic equations

$$\dot{\phi}_i = \omega_0 + K \sin(\phi_{i-1} + \phi_c - \phi_i)$$

Approach to Frequency Tuning

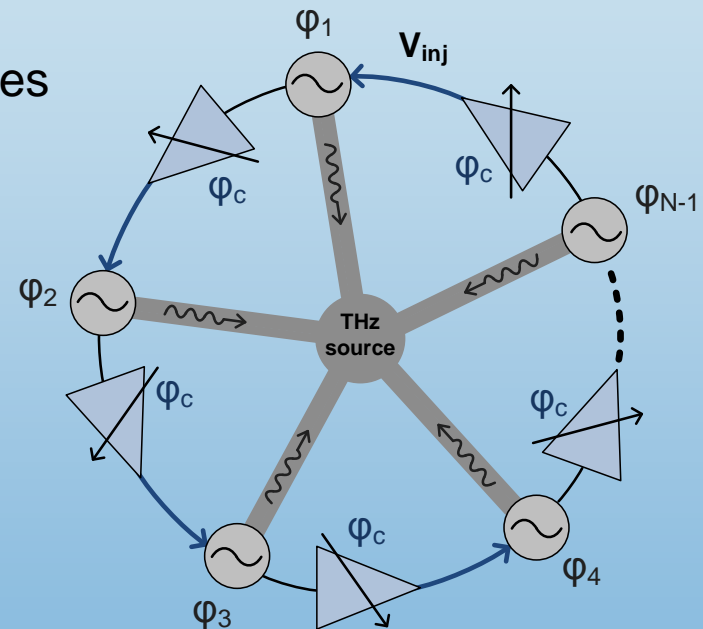
- In a given coupling mode Ψ is fixed
- Changing Φ_c results in change in the locking frequency

$$\dot{\phi}_i = \omega_0 + K \sin(\phi_{i-1} + \phi_c - \phi_i) \quad \omega = \omega_0 + K \sin(\phi_c - \psi_k^o)$$



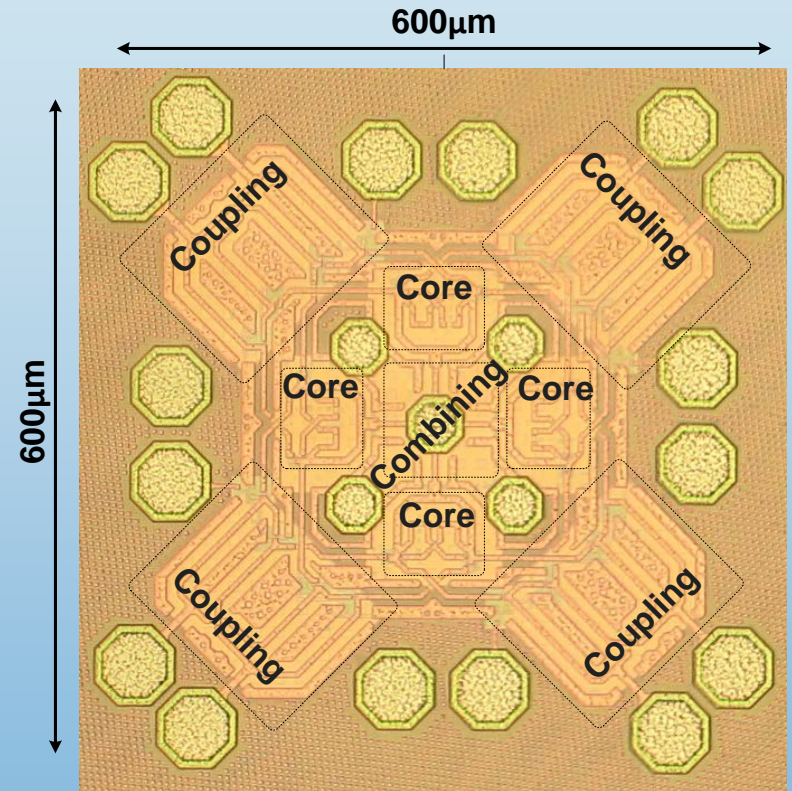
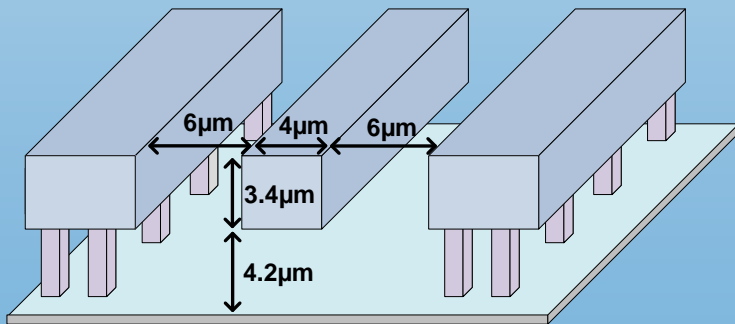
A Terahertz Tunable Source

- Features of the proposed source
 - ✓ Efficient harmonic generation
 - ✓ Power combining from multiple sources
 - ✓ Tuning separated from power generation
 - ✓ A scalable scheme
- Design steps
 - Choose the best harmonic frequency
 - Select the number of cores (N)
 - Design the coupling and combing blocks



Silicon Prototype

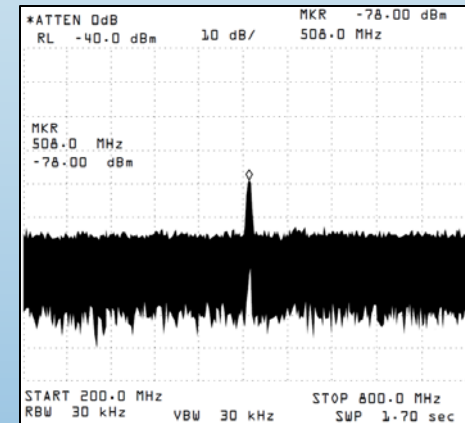
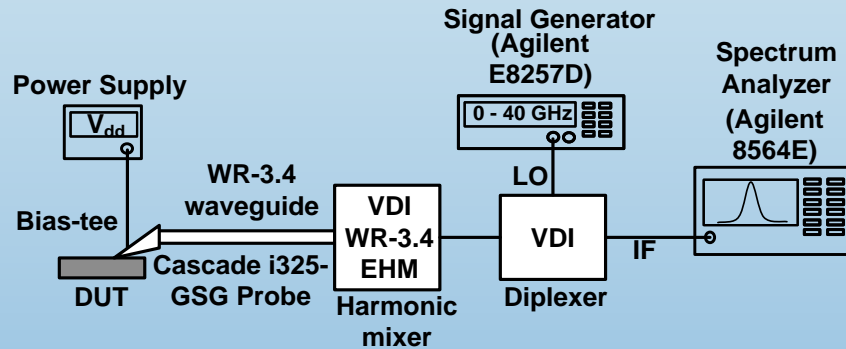
- Standard 65nm LP bulk CMOS
- Grounded CPW for lines
- Ground shielding between blocks
- Two versions are measured
 - A 290 GHz source
 - A 320 GHz source



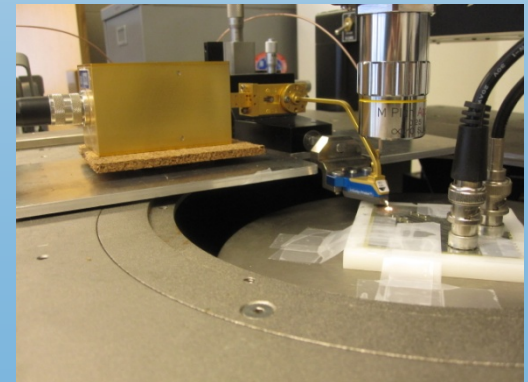
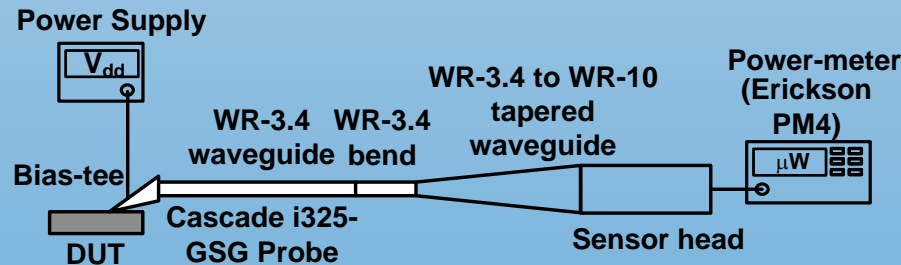
Measurement Setup

- Two setups for power and frequency.

a) Frequency setup



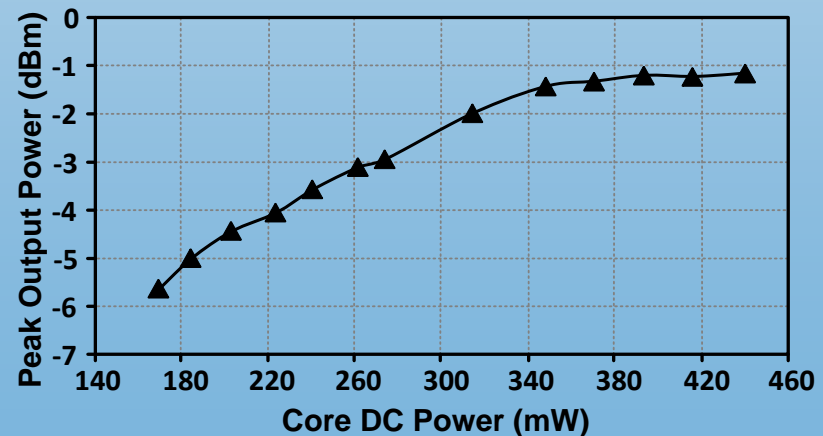
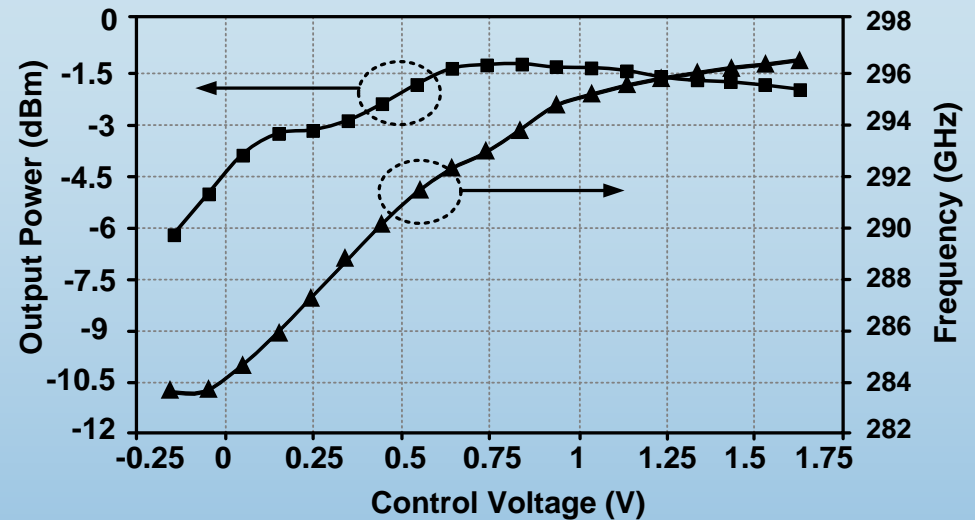
b) Power setup



The 290 GHz Source

- Chip performance summary

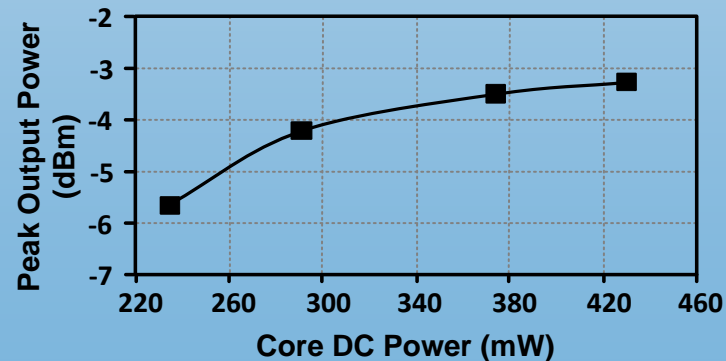
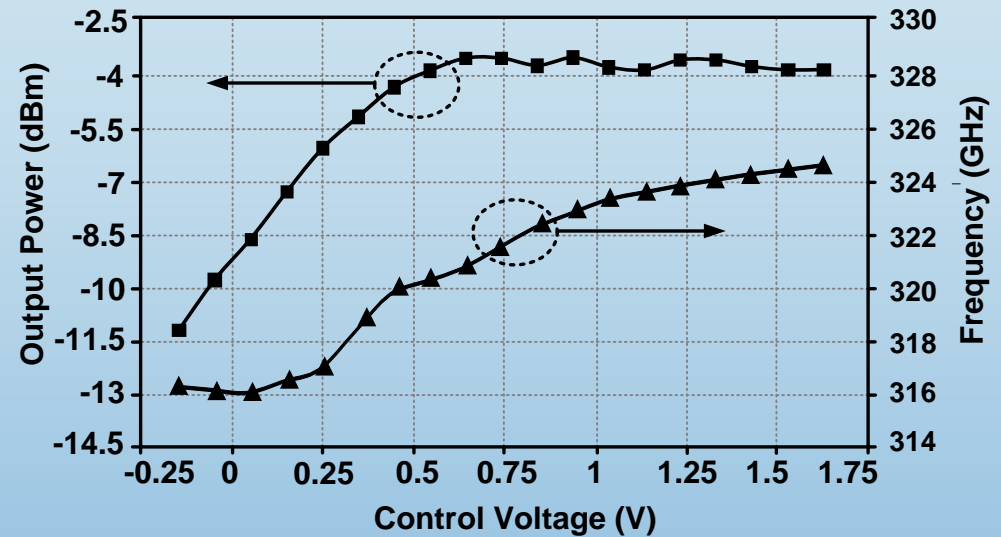
Center frequency	0.29 THz
Tuning range	13 GHz
Peak power	0.76 mW
Phase noise (@ 1 MHz offset)	-78 dBc/Hz
DC power	325 mW
Core supply	1.3 V
Coupling supply	1.1 V



The 320 GHz Source

- Chip performance summary

Center frequency	0.32 THz
Tuning range	8.4 GHz
Peak power	0.46 mW
Phase noise (@ 1 MHz offset)	-77 dBc/Hz
DC power	339 mW
Core supply	1.3 V
Coupling supply	1.1 V

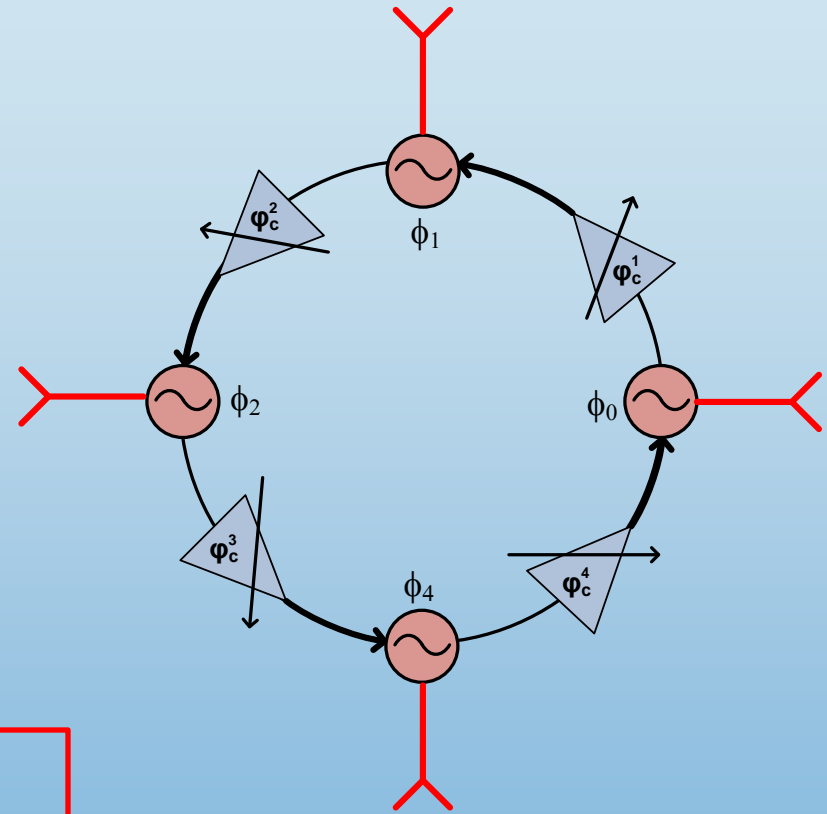


Outline

- Motivation
- Terahertz Frequency Multipliers
- High Power Terahertz Oscillator Design
- A High Power THz VCO
- THz Radiator Arrays
- Conclusion

A 2x2 Phased Array

- 4 coupled cores radiate separately
- Output power is spatially combined
- Consider two cases
 - Equal change in all Φ_c 's:
 - ✓ Frequency control
 - Differential change in Φ_c 's:
 - ✓ Phase control

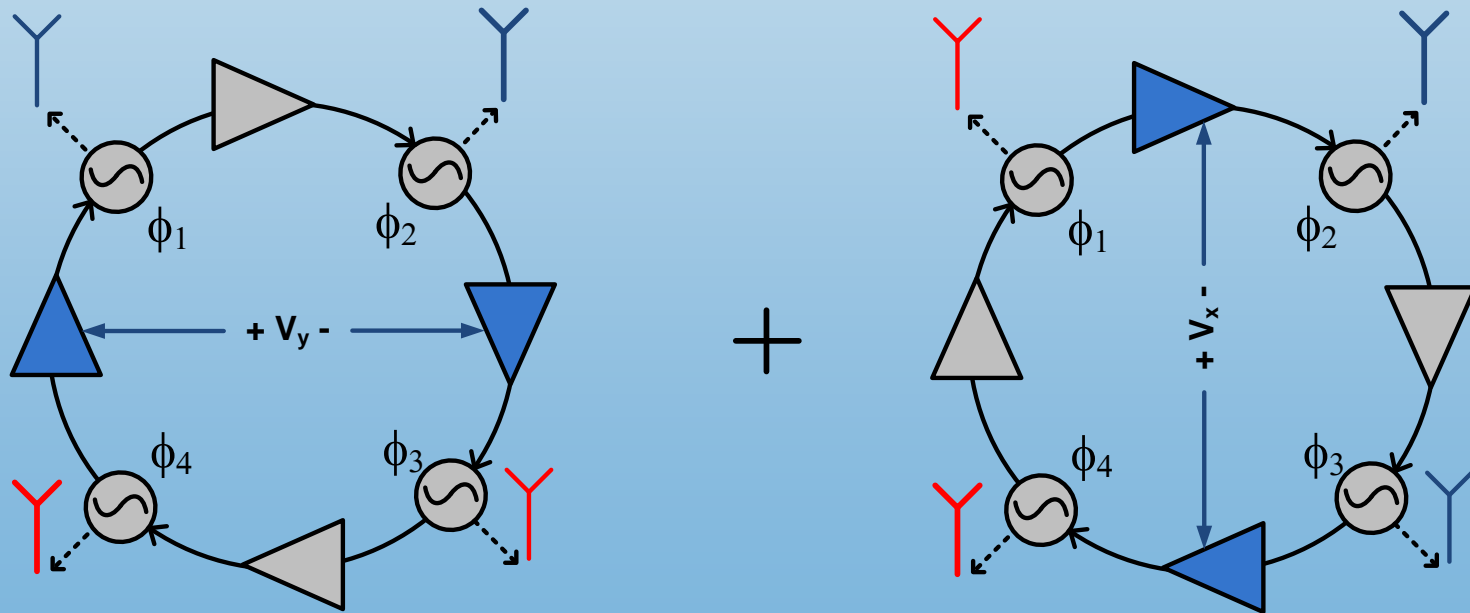


$$\psi_i^o = \frac{2k\pi}{N} - \frac{1}{N} \sum \phi_c^i + \phi_c^i$$

$$\omega = \omega_0 + K \sin\left(\frac{1}{N} \sum \phi_c^i - \frac{2k\pi}{N}\right)$$

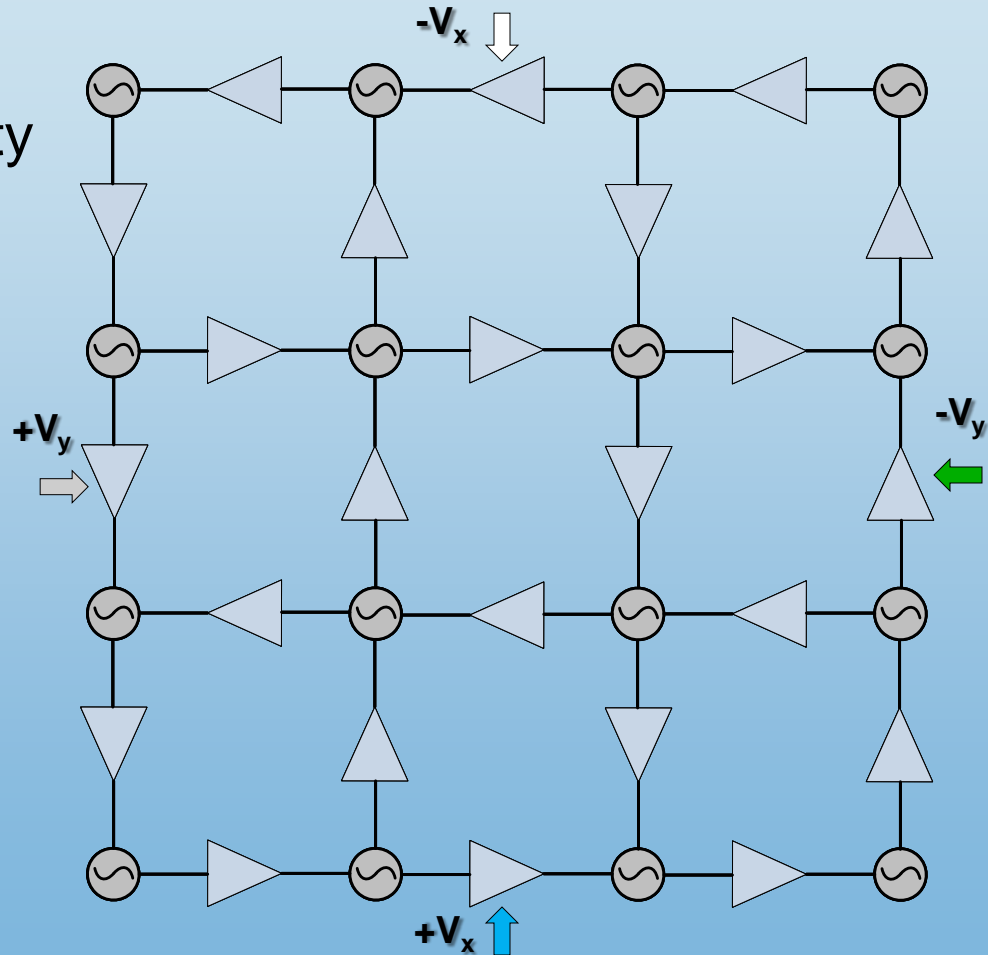
Example of Beam-Forming

- V_y : Beam steering in y direction
- V_x : Beam steering in x direction
- Superposition of two differential voltages : 2-D beam forming



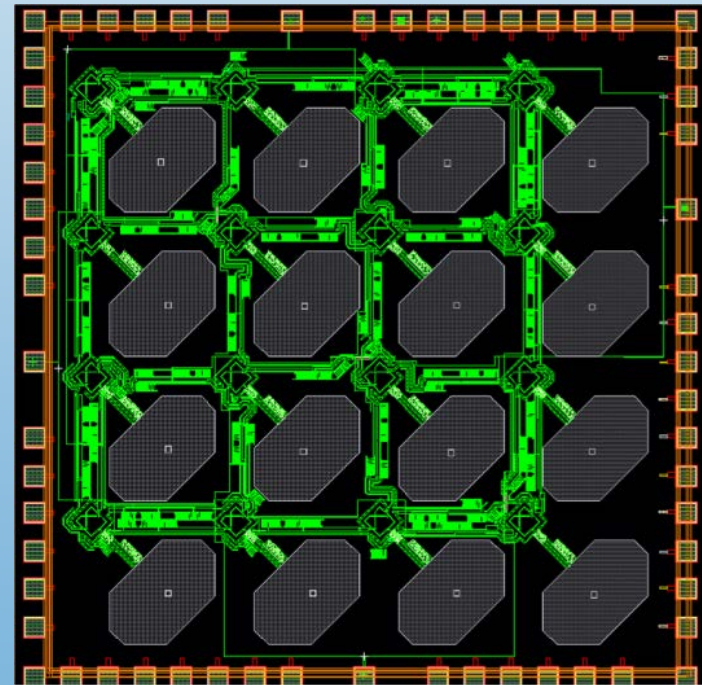
Scalable Architectures

- Scalability and stability
- Coupling topology
- 2-D beam forming
- Frequency tuning

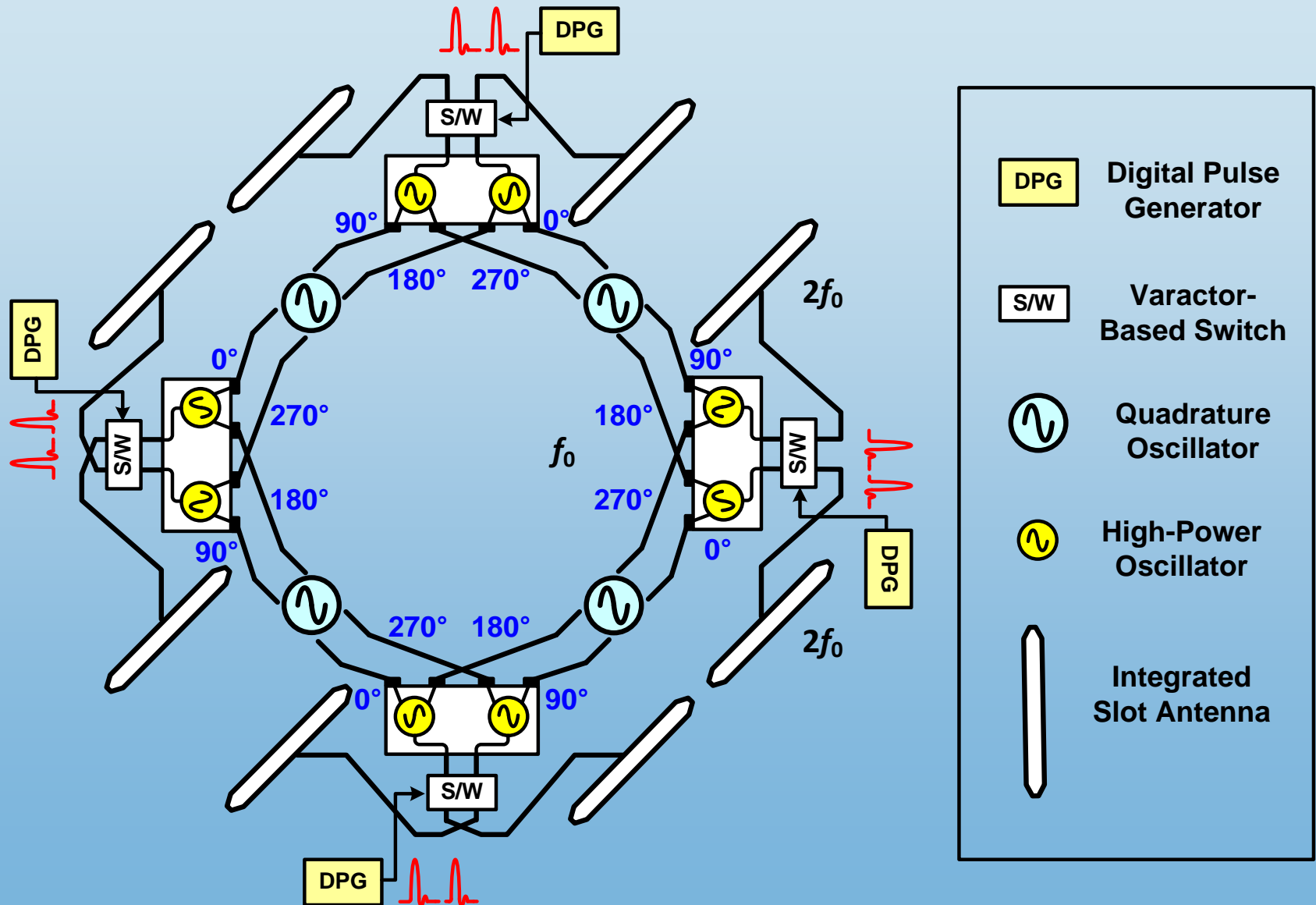


A 4x4 Terahertz Phased Array

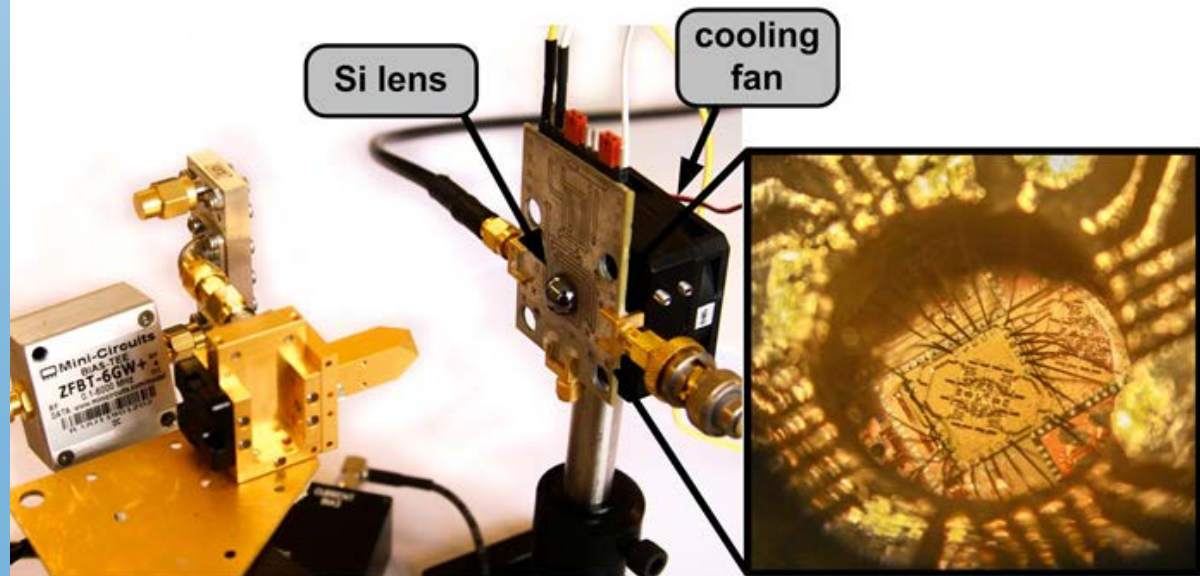
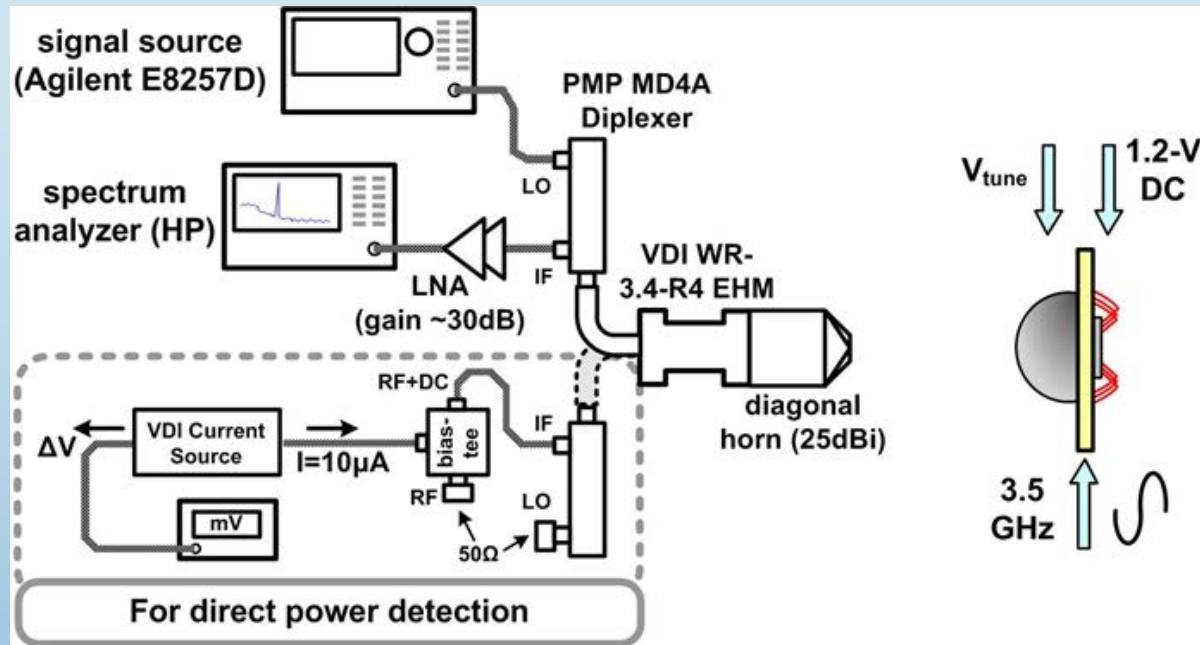
- ❑ Chip fabricated in a CMOS 65nm GP bulk process.
- ❑ Simulation results
 - Center frequency: 350 GHz
 - Tuning range: 8%
 - Generated power: 3.2 mW
 - Radiated power: 1.4 mW
 - EIRP > 100 mW
- ❑ 2-D beam forming
- ❑ Highly scalable
- ❑ No global routing



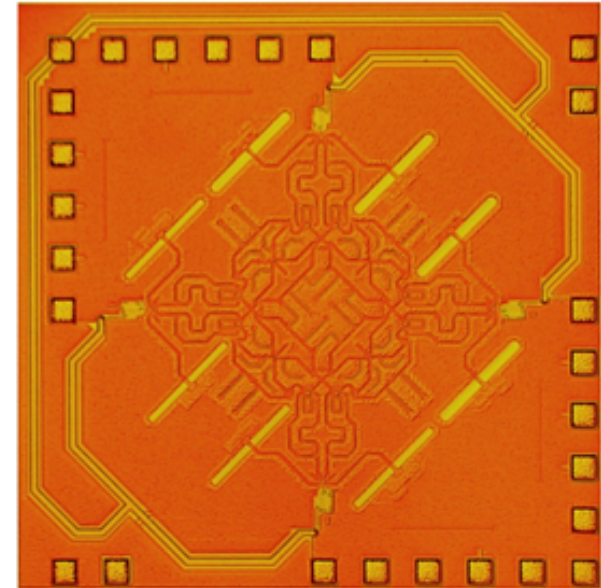
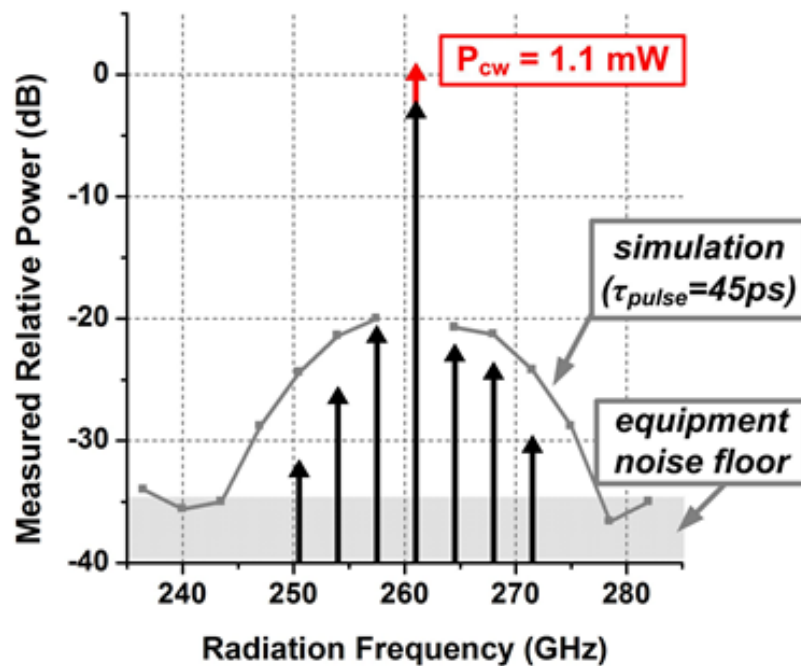
260-GHz Broadband Array



260-GHz Broadband Array

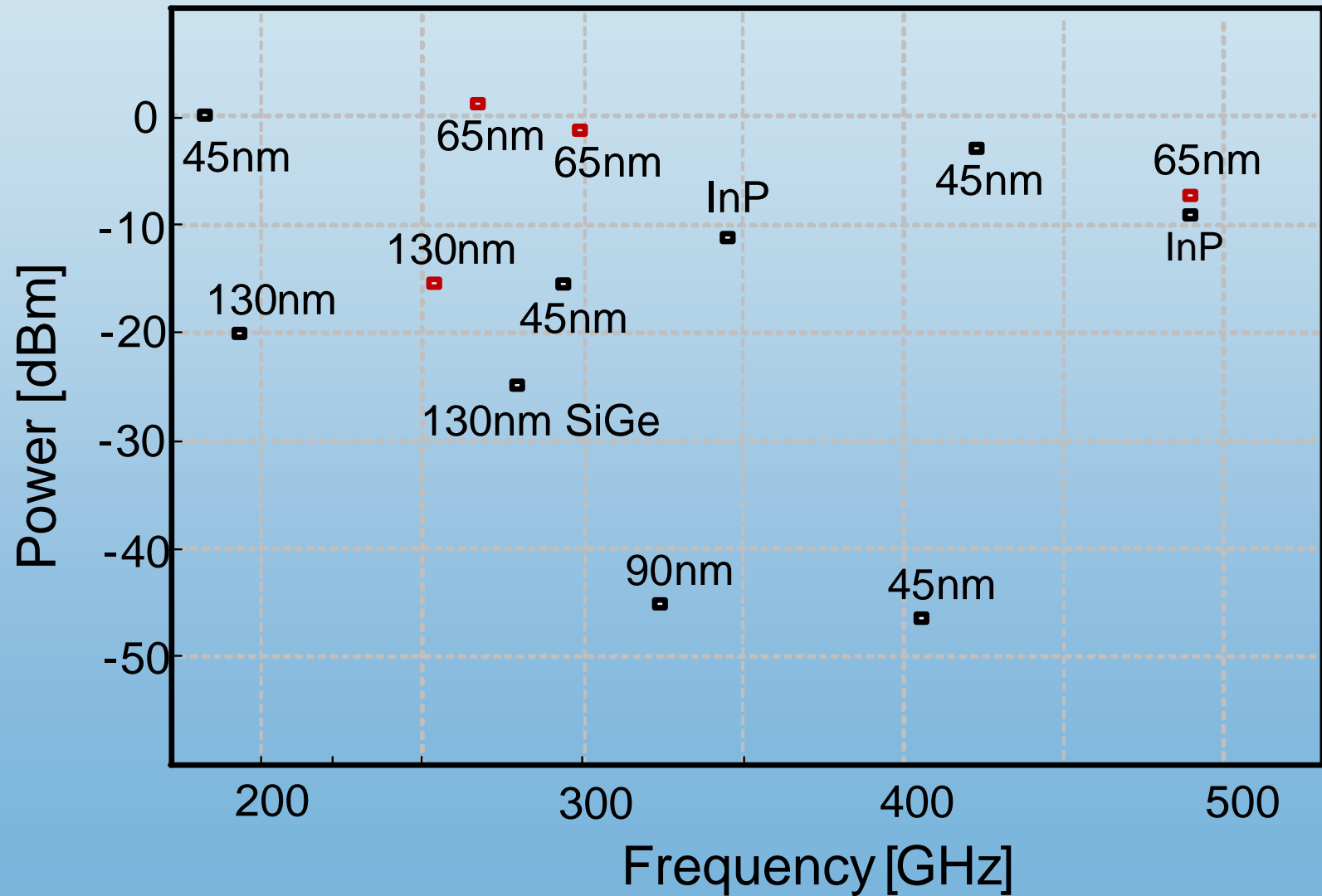


260-GHz Broadband Array



	<i>ISSCC 2012 [1]</i>	<i>ISSCC 2012 [2]</i>	<i>VLSI 2011 [3]</i>	<i>This Work</i>
Frequency (GHz)	290	280	380	260
Bandwidth (%)	4.5	3.2	4	9.5
EIRP (dBm)	N/A	9.4	-13	15.7
Total Output Power (dBm)	-1.2	-7.2	N/A	0.5
Phase Noise	-78dBc/Hz @ 1MHz	N/A	N/A	-78.3dBc/Hz @ 1MHz
DC Power (W)	0.32	0.81	0.36	0.8
Technology	65nm Bulk CMOS	45nm SOI CMOS	130m SiGe BiCMOS	65nm Bulk CMOS

Comparison



CMOS mm-Wave & THz Amplifiers

- Signal amplification is challenging in CMOS:
 - CMOS scaling is reaching its limit.
 - Operation frequency of these systems is close to the maximum oscillation frequency (f_{max}) of the transistors.
 - Maximum available gain (G_{ma}) of the transistors drops below useful level for most applications.
 - PAE drops as the gain drops at high frequencies.

We need to boost G_{ma} to its maximum possible value.

Optimum Conditions

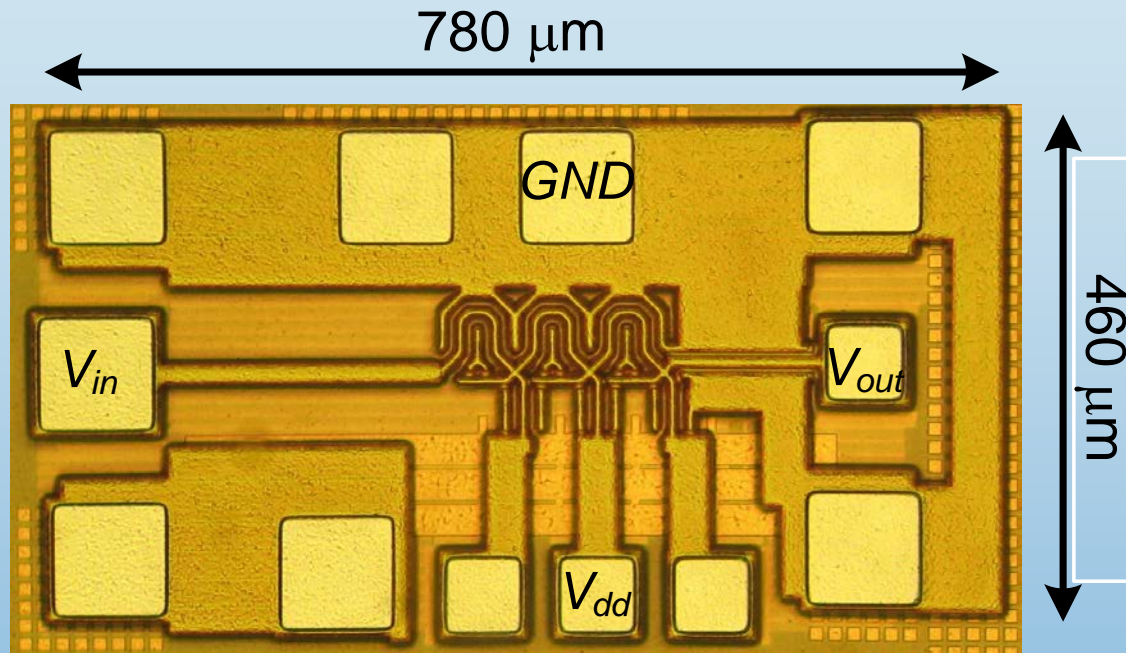
Assuming most of the input power flows from source to port 1 of the device and most of the output power flows to the load:

$$Gain \cong 1 + \frac{2}{G_{11}} \{ -(G_{11} + A^2 G_{22}) - A |Y_{12} + Y_{21}^*| \cos(\angle(Y_{12} + Y_{21}^*) + \varphi) \}$$

$$A_{opt} = \frac{|Y_{12} + Y_{21}^*|}{2G_{22}} \quad \varphi_{opt} = (2k + 1)\pi - \angle(Y_{12} + Y_{21}^*)$$

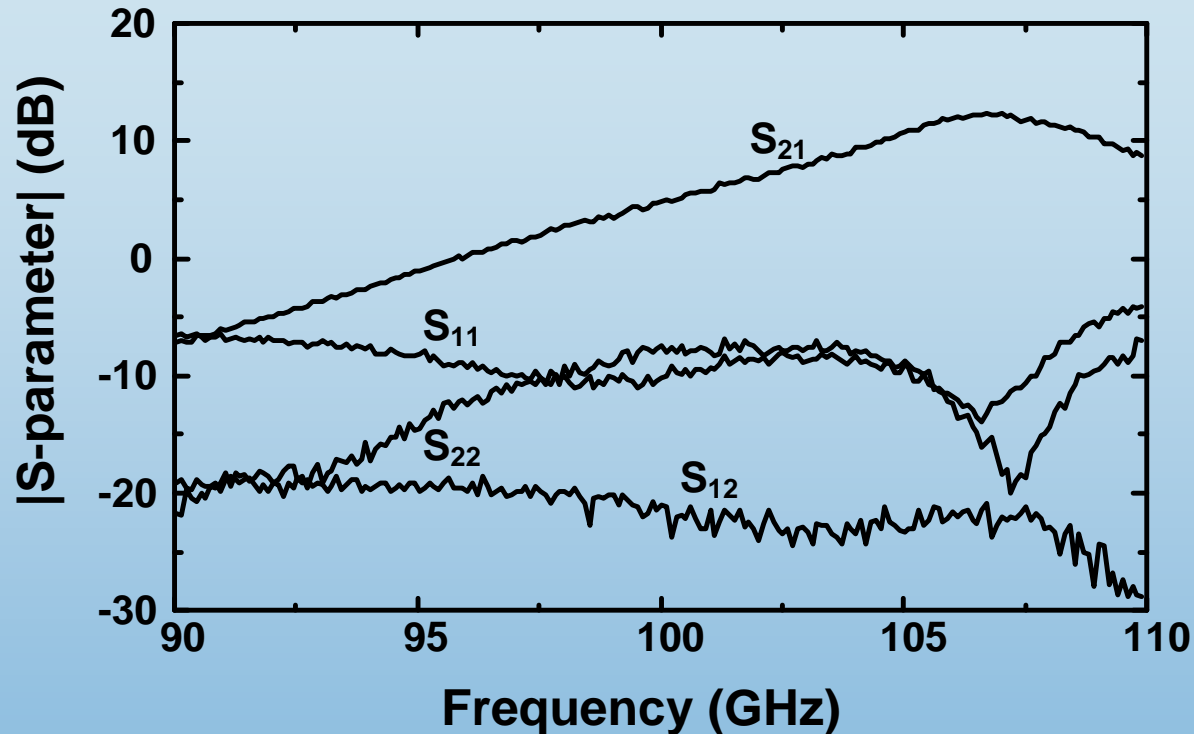
Gain is maximized by providing optimum voltage gain and phase conditions for the device.

Chip Photo



- Inductors are implemented using microstrip transmission lines.
- Capacitors are implemented using metal finger capacitors or the capacitance pads.

S-Parameter Measurement



- Power gain of 12.5 dB is achieved at 107 GHz.
- Input and output reflection coefficients are -13 dB and -19 dB, respectively.
- DC power consumption is 31 mW.

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Summary

- It is critical to have a good device understanding to squeeze out the maximum power/gain
- E/M modeling is critical
- Built-in self test is highly desirable
- RF engineers need to learn more microwave/device physics
- For some applications CMOS is not sufficient and compound semiconductors (especially GaN) show great potential.



The Next Frontier for Circuit Designers: CMOS THz Systems



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