# Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

**Submission Title:** MMIC Chip Sets for Wireless Communication up to 480 GHz
**Date Submitted: 15 July, 2012**
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**Re:** DCN 15-12-0323-00-0thz

**Abstract:** The architecture, implementation and performance of active MMIC-based transmit and receive frontends for sub-mmW communication are presented. A focus is on the generation of local oscillator signals for up- and down-conversion by frequency multiplication up to 480 GHz. Transmission experiments at a center frequency of 220 GHz achieve up to 25 Gbit/s data rate.

**Purpose:** Review of current progress on the implementation of active electronics-based transmitters and receivers for terahertz communication.

# MMIC Chip Sets for Wireless Communication up to 480 GHz

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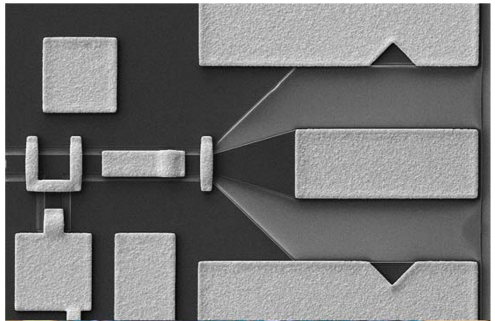
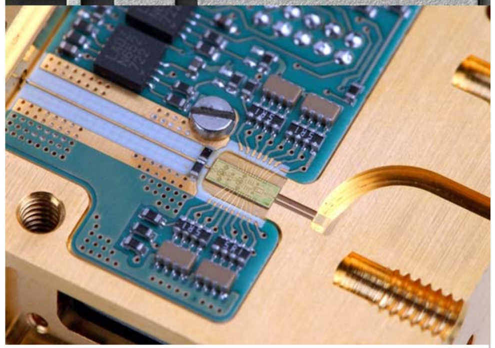
# Abstract

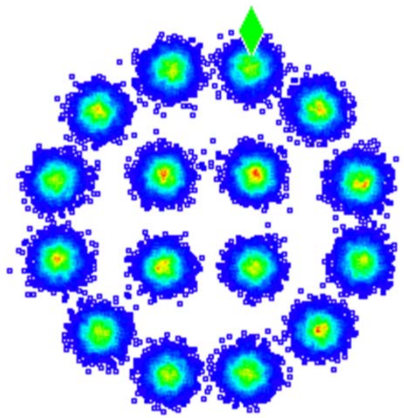




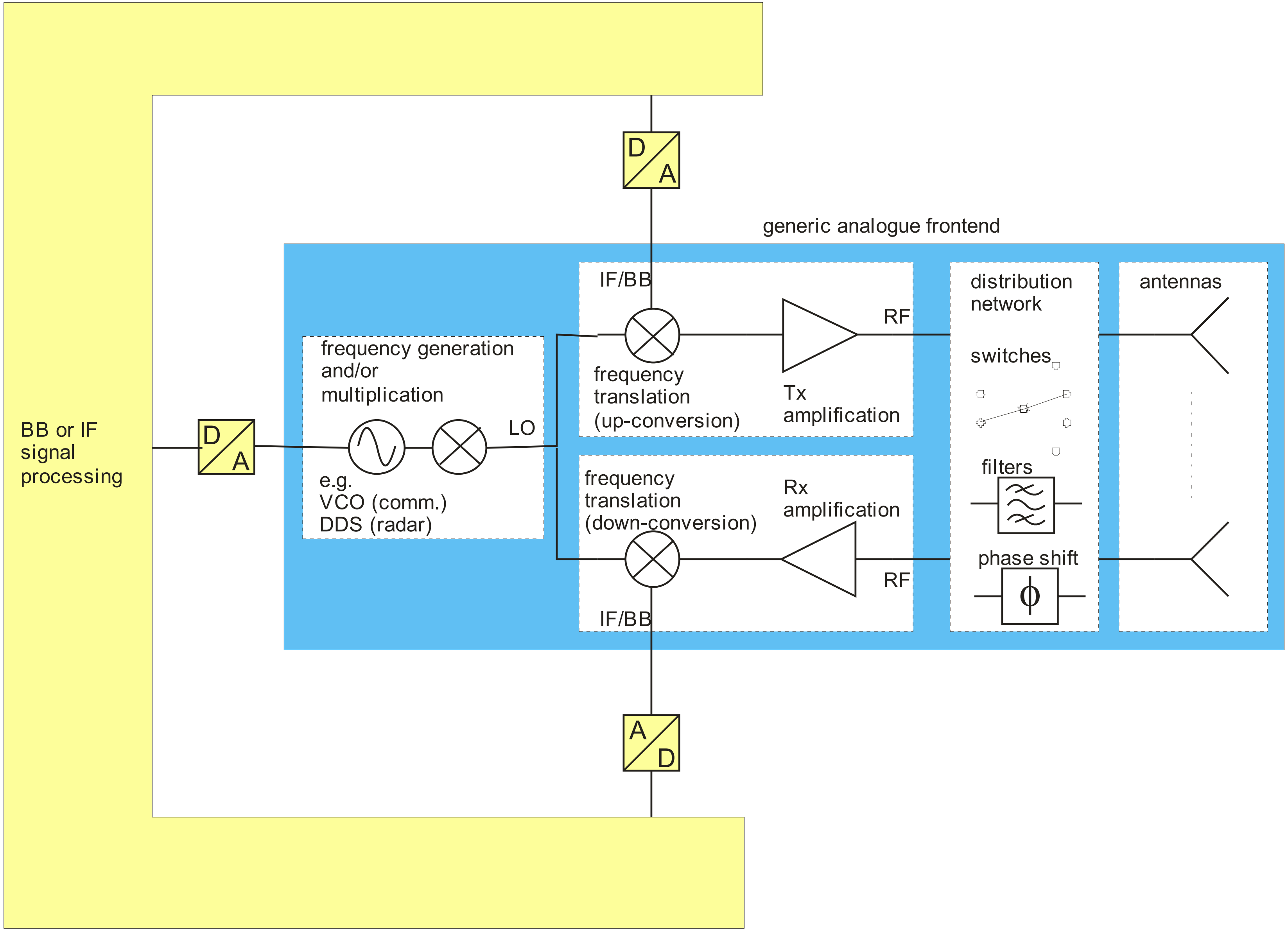
The architecture, implementation and performance of **active MMIC-based transmit and receive frontends** for sub-mmW communication are presented.

A focus is on the **generation of local oscillator signals** for up- and down-conversion by frequency multiplication up to 480 GHz.

**Transmission experiments** at a center frequency of 220 GHz achieve up to 25 Gbit/s data rate.



# Generic Millimeter-Wave Analog Frontend

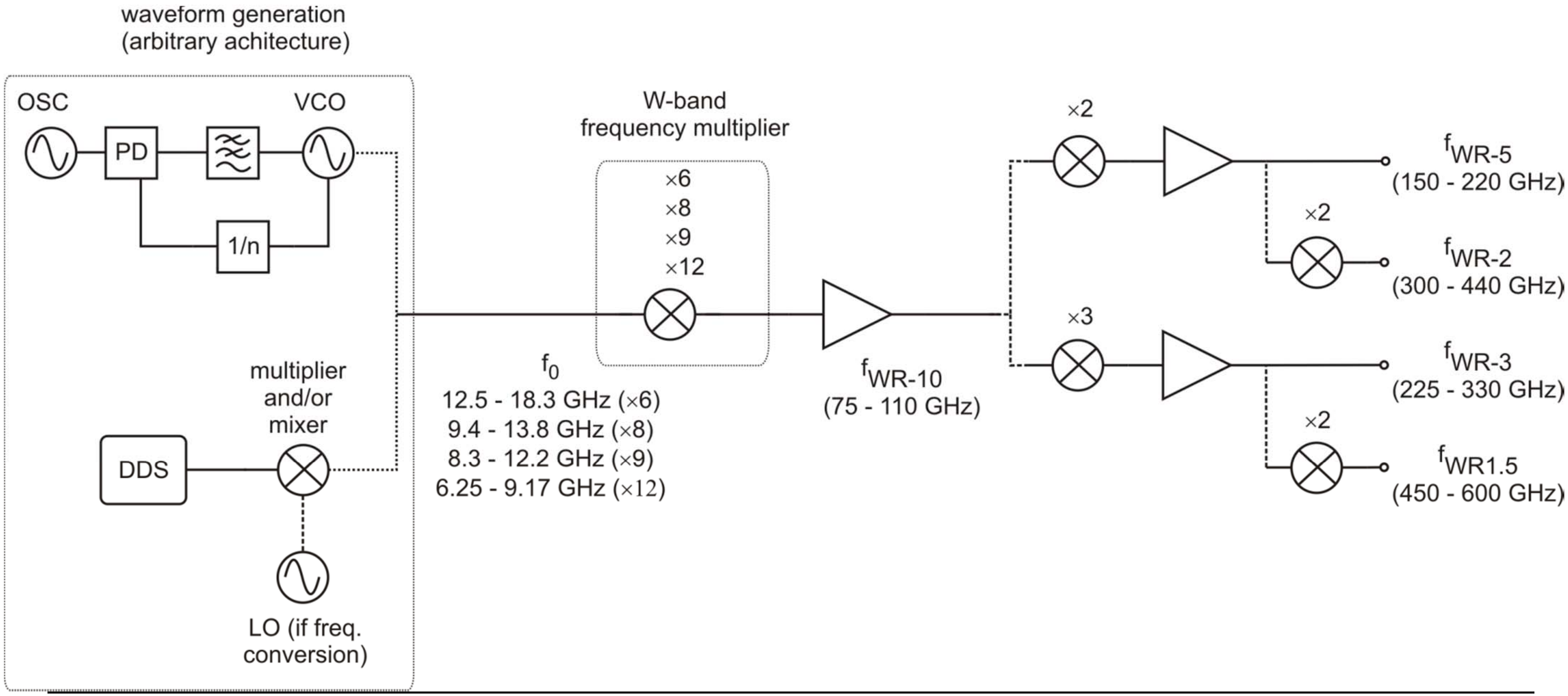


# MMIC-based sub-mmW frequency generation

frequency generation < 20 GHz

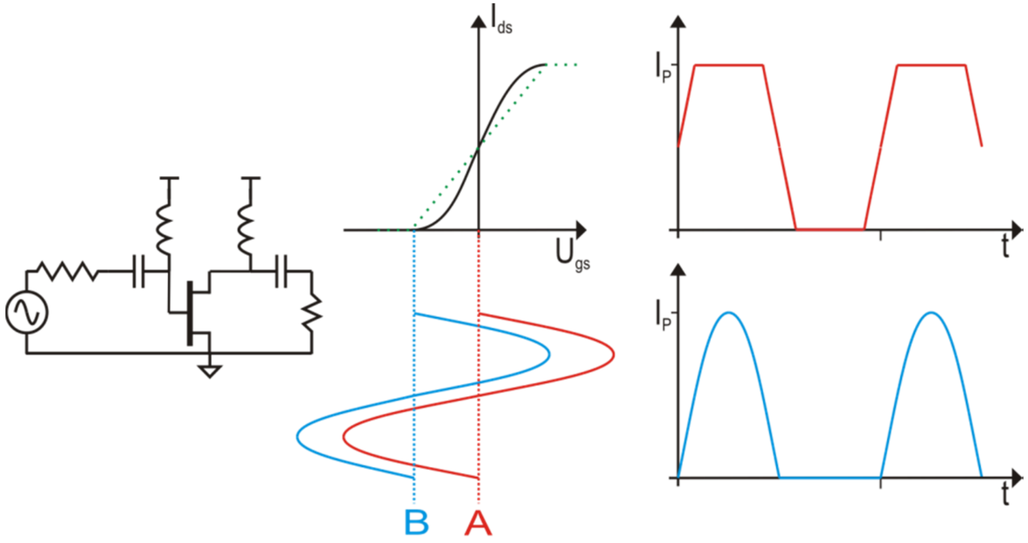
frequency platform in W-band

single-chip cascade of multiplication and amplification stages

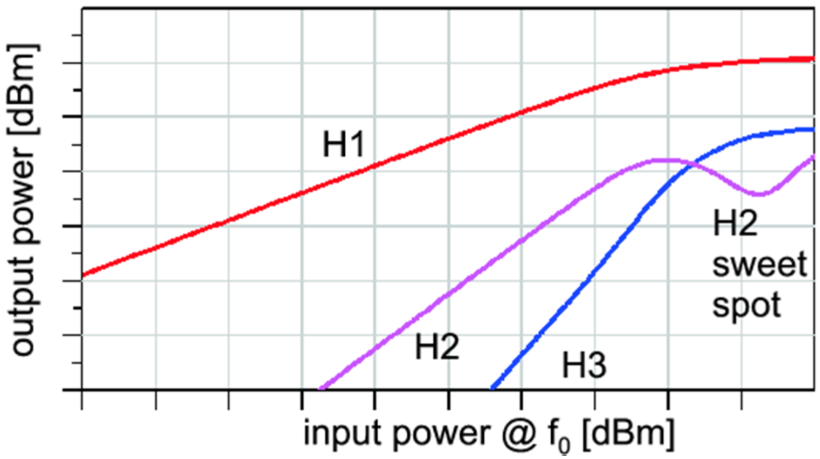


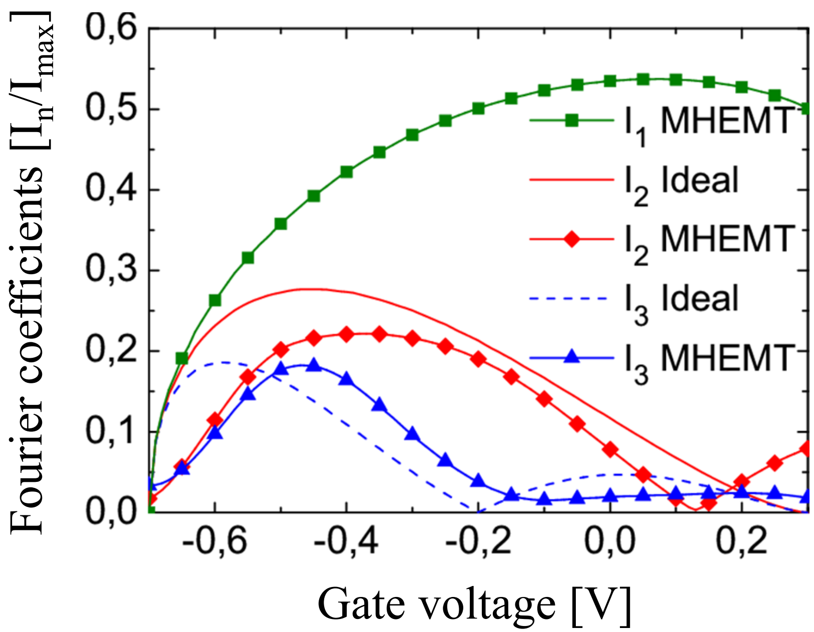
# FET Frequency Multipliers

Power compression




Conduction angle (class A-C)



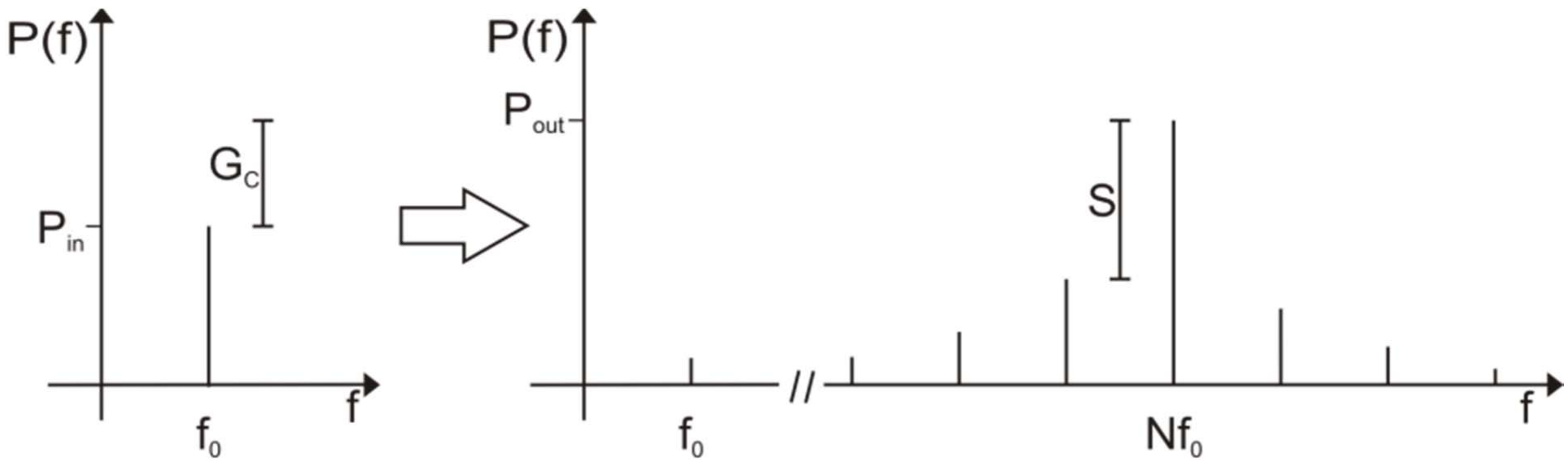



# Frequency Multiplier Figures of Merit

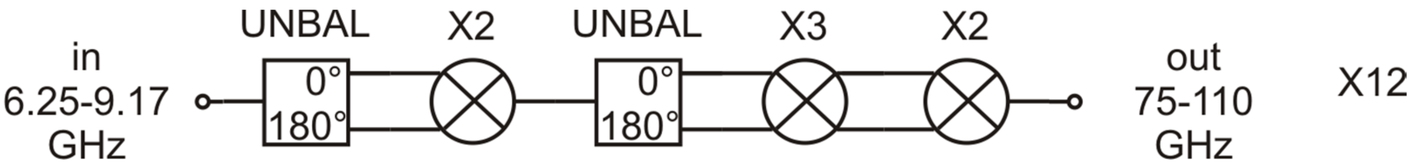
- Multiplication factor N
- Output power $P_{out}$
- Conversion Gain $G_C$
- Suppression of unwanted harmonics S
- Degradation of phase noise ≥20·logN
- DC power

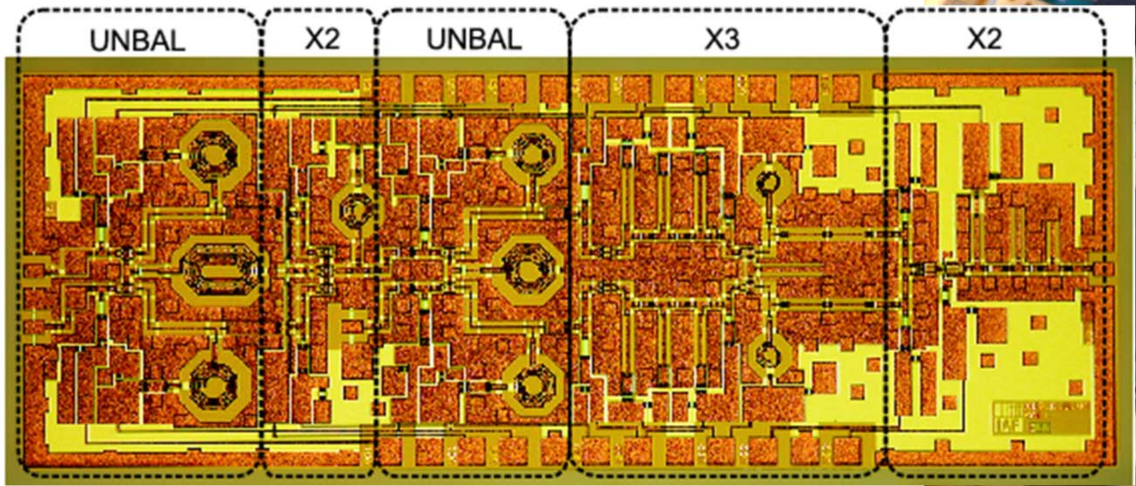
Phase / amplitude modulation

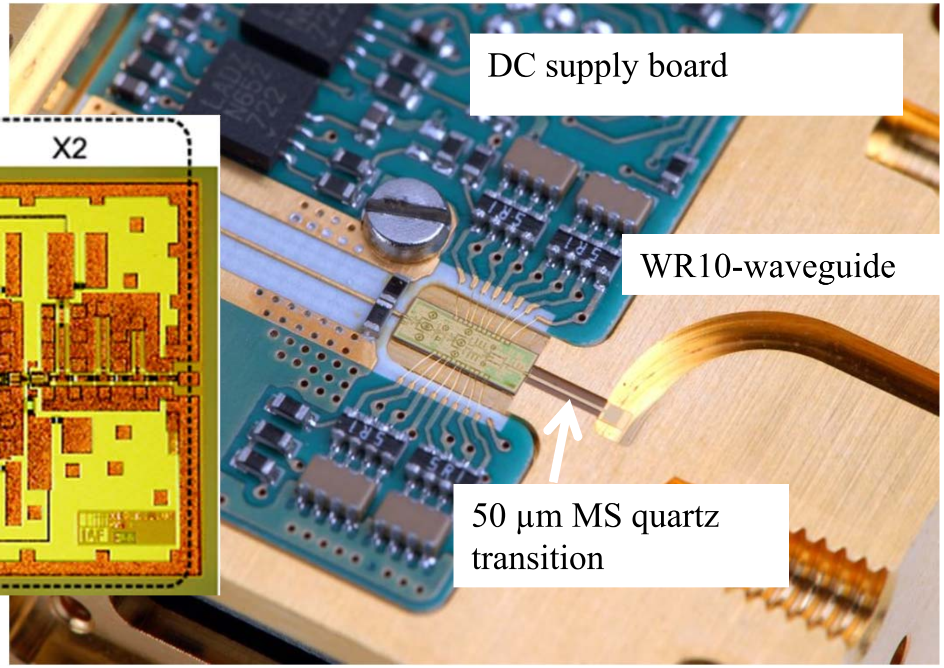
$$\begin{pmatrix} \theta_2 \\ m_2 \end{pmatrix} = \begin{pmatrix} T_{pp} & T_{pa} \\ T_{ap} & T_{aa} \end{pmatrix} \begin{pmatrix} \theta_1 \\ m_1 \end{pmatrix} = \begin{pmatrix} N & 0 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} \theta_1 \\ m_1 \end{pmatrix}$$



# W-Band Multiplier-by-Twelfe
# MMIC and Waveguide Module



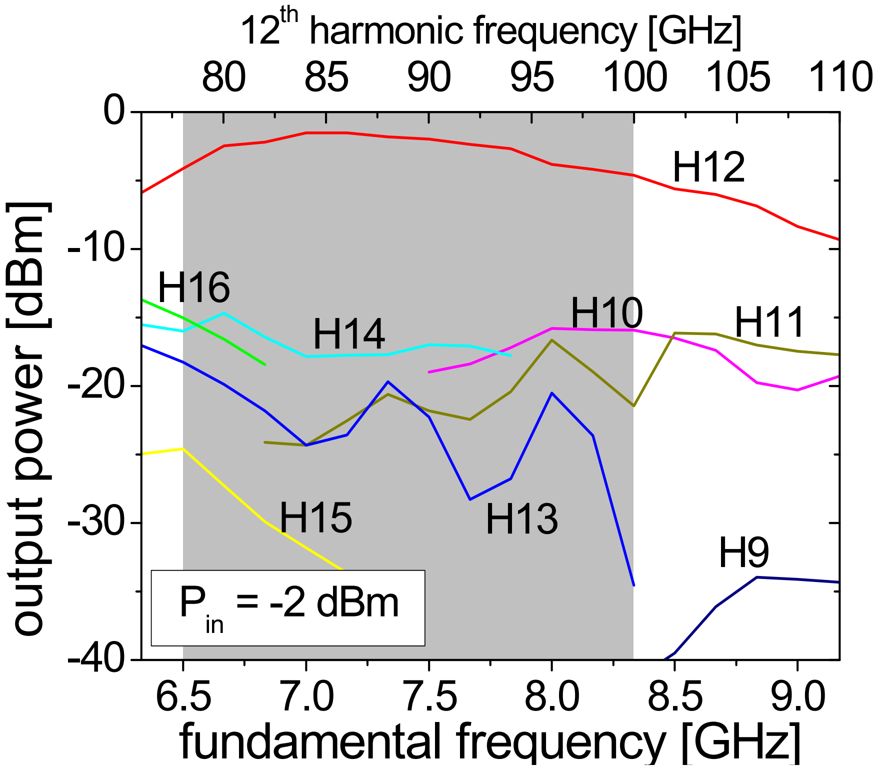



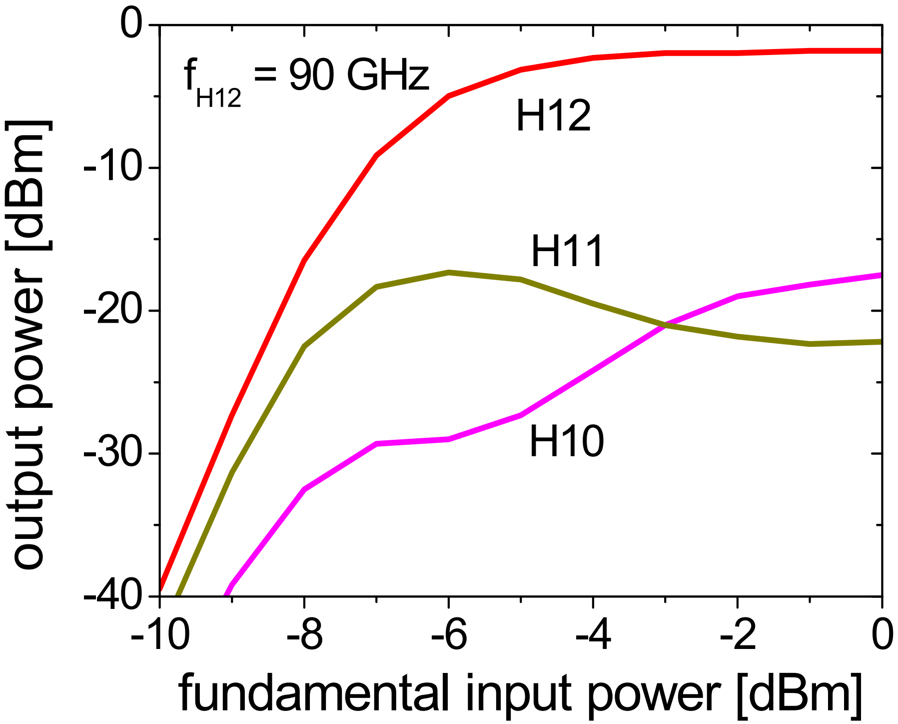

4 x 1.5 mm$^2$
100 nm mHEMT

Kallfass et. al. EuMIC 2011

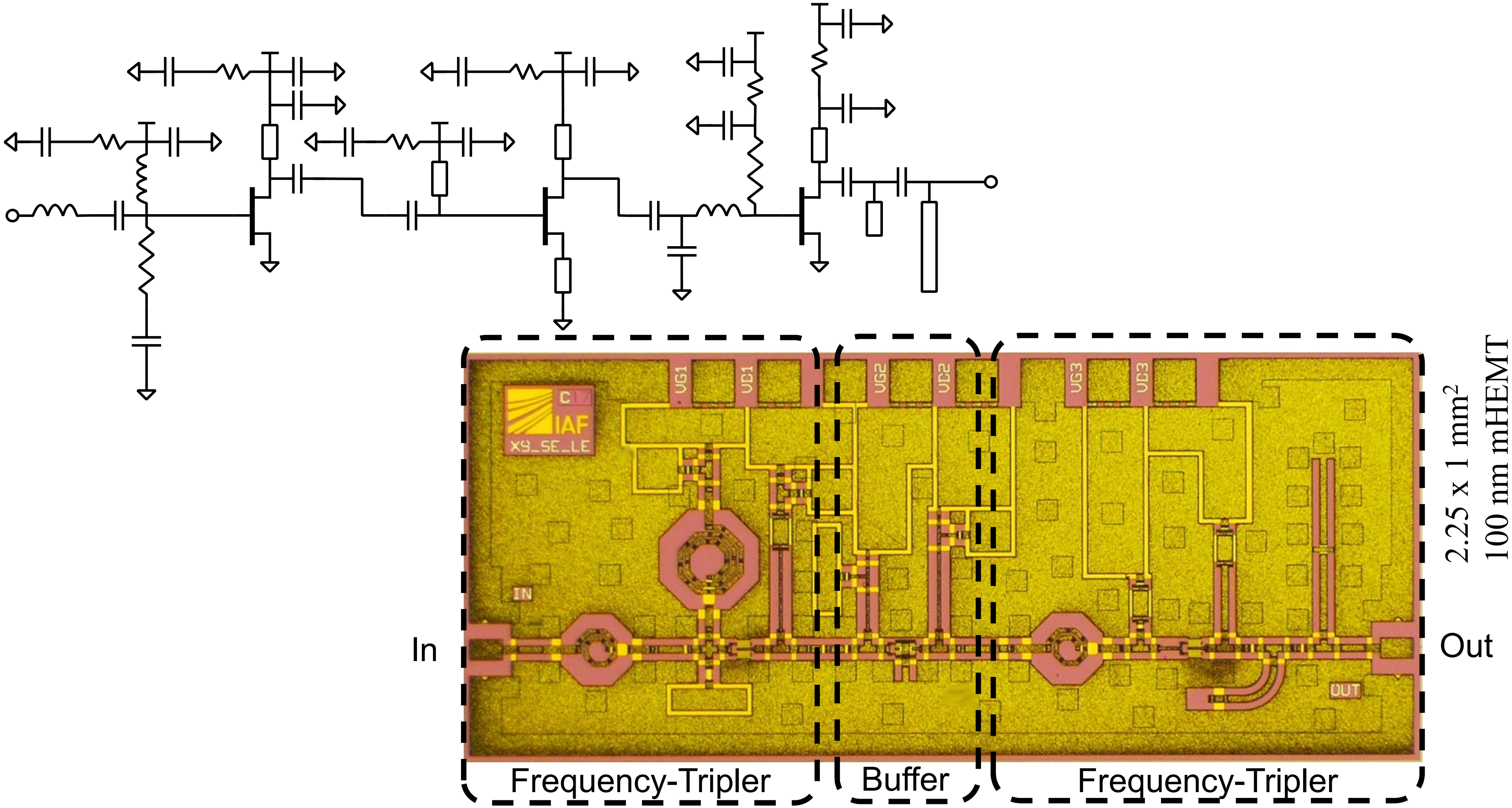
# W-Band Multiplier-by-Twelfe Module Performance

- Range: 78 – 100 GHz
- Bandwidth: 22 GHz (25%)
- Spectral purity: >12 dBc
- Output power: -1.5 dBm
- Conversion gain: 2.5 dB



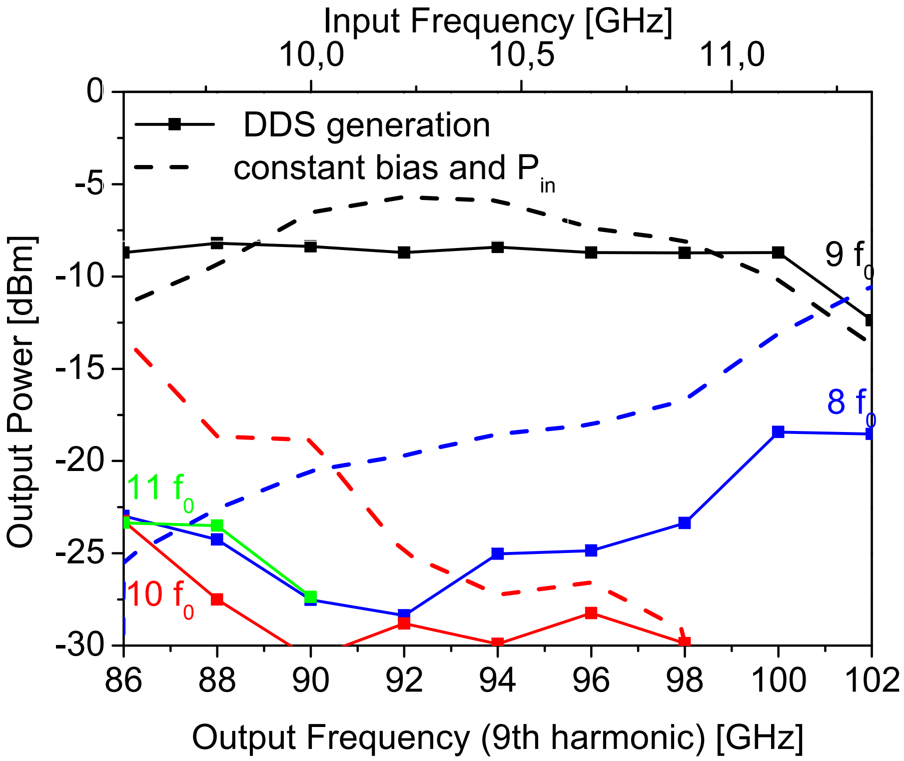
# (X to) W-Band Multiplier-by-Nine

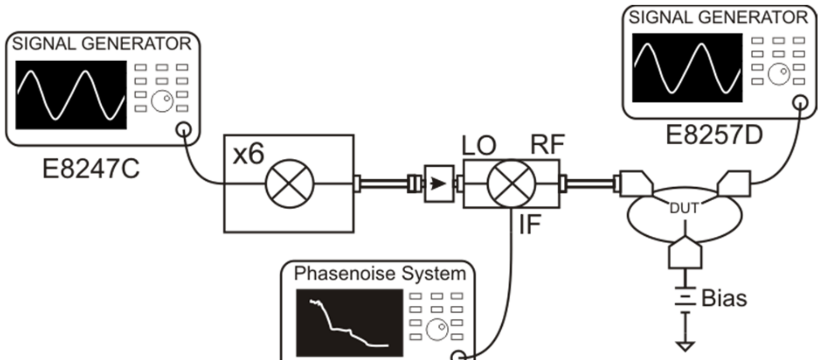


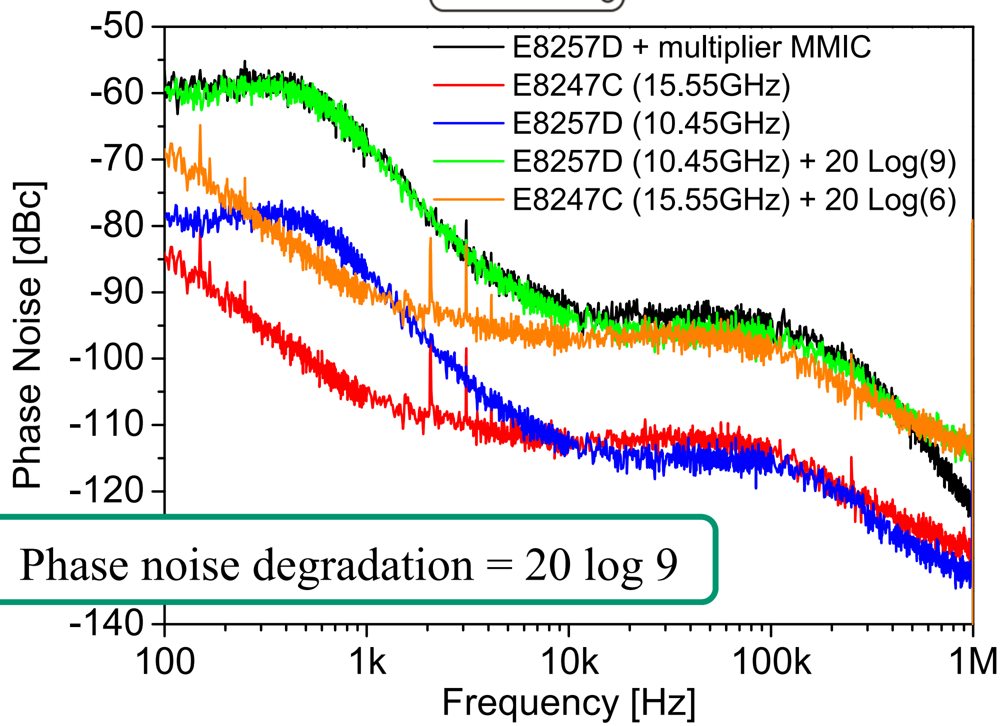

Lewark et. al. GeMIC 2011

# (X to) W-Band Multiplier-by-Nine

Optimized BW and spectral purity by DDS controlled bias and Pin

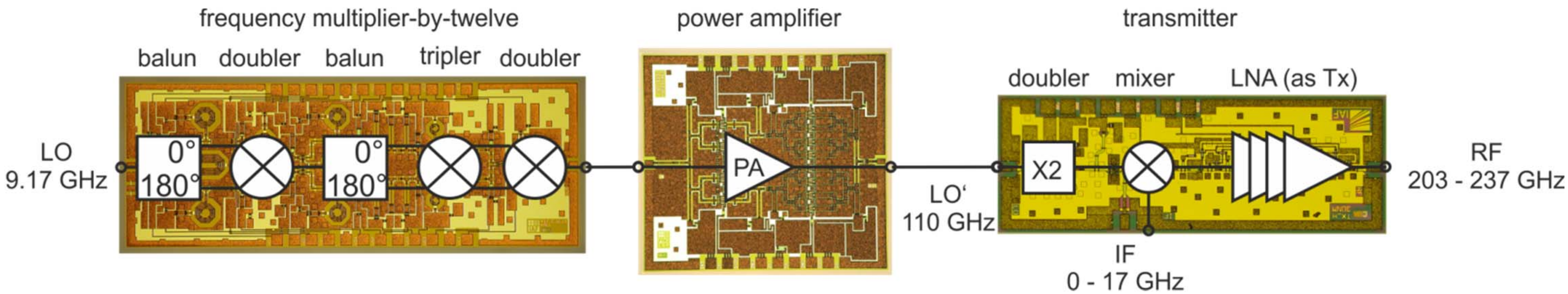


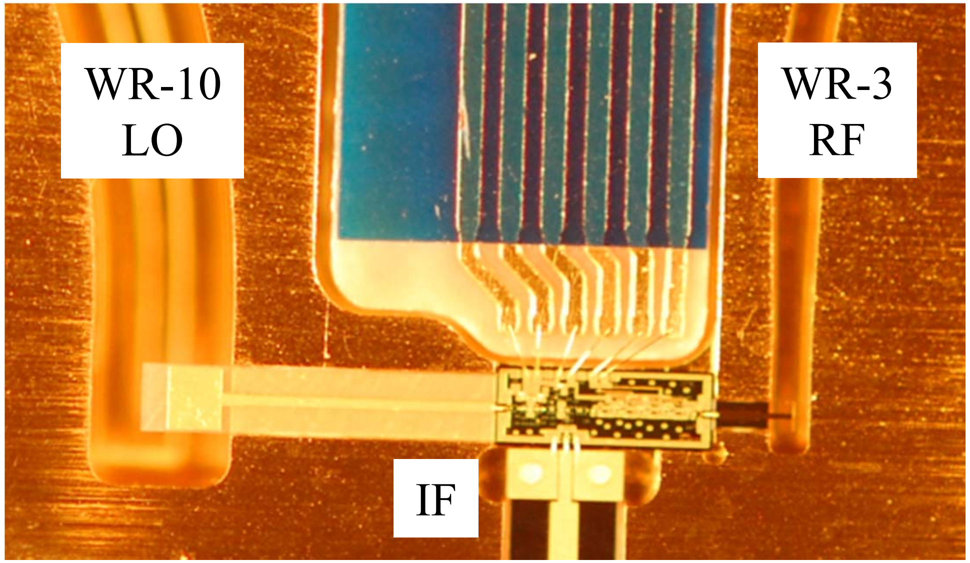




Phase noise degradation = 20 log 9

# Chip Set for 220 GHz Transmission

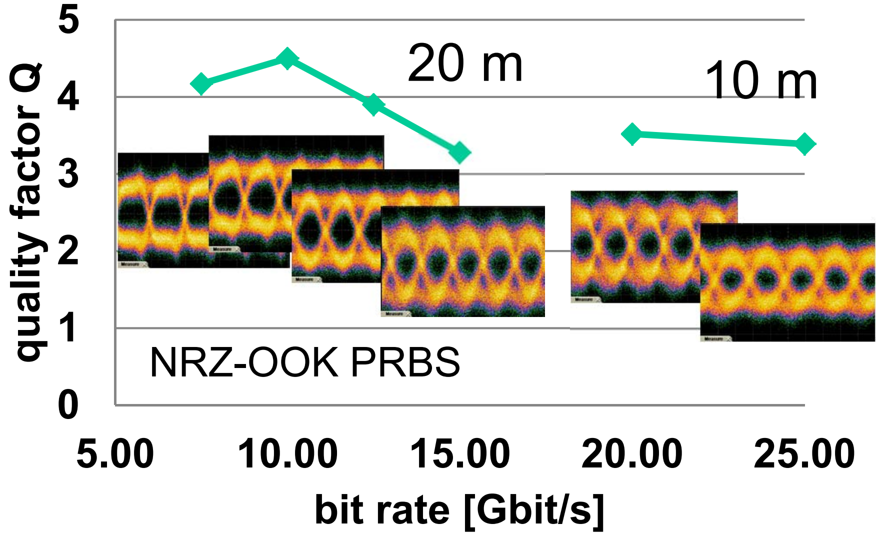


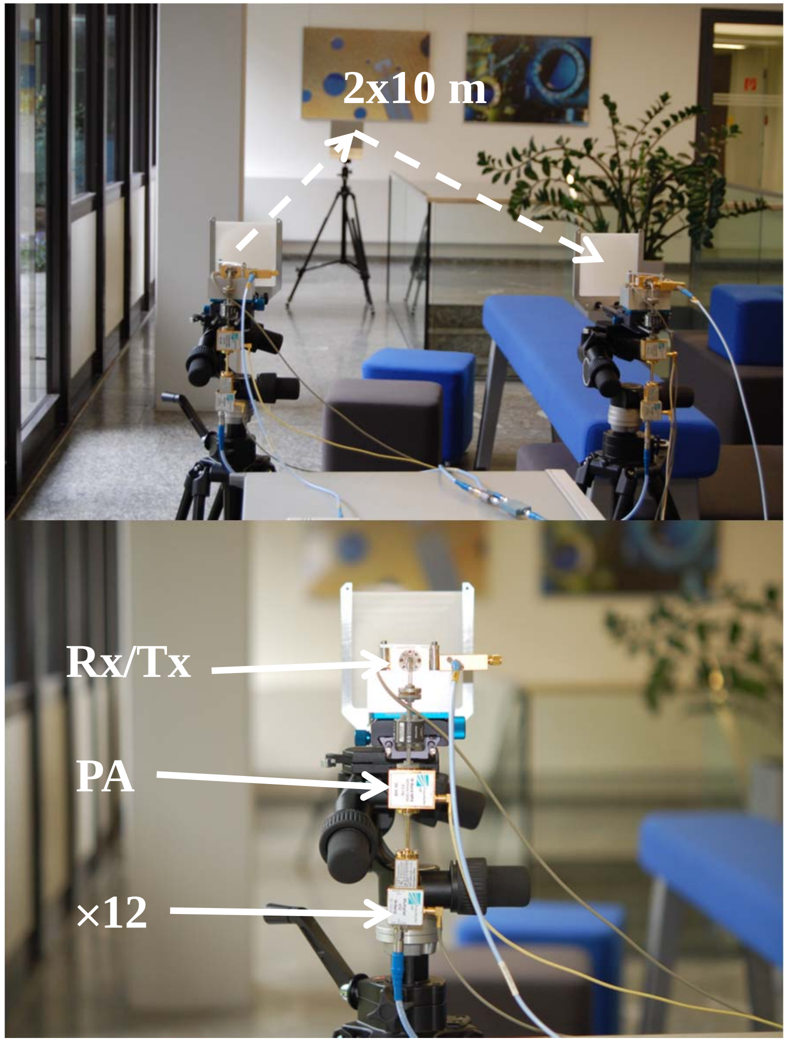

| | |
|---|---|
| $f_{RF,c}$ | 220 GHz |
| $B_{RF}$ | 34 GHz |
| $f_{LO}$ | 9.17 GHz |
| $f_{LO}$ | 110 GHz ($n$ = 12 ) |
| $B_{BB}$ | 17 GHz |
| $P_{tx}$ | ca. 0 dBm |
| $NF_{rx}$ | ca. 6.8 dB |
| $G_{rx/Gtx}$ | ca. 15 dB |



# 220 GHz Transmission Coherent LO

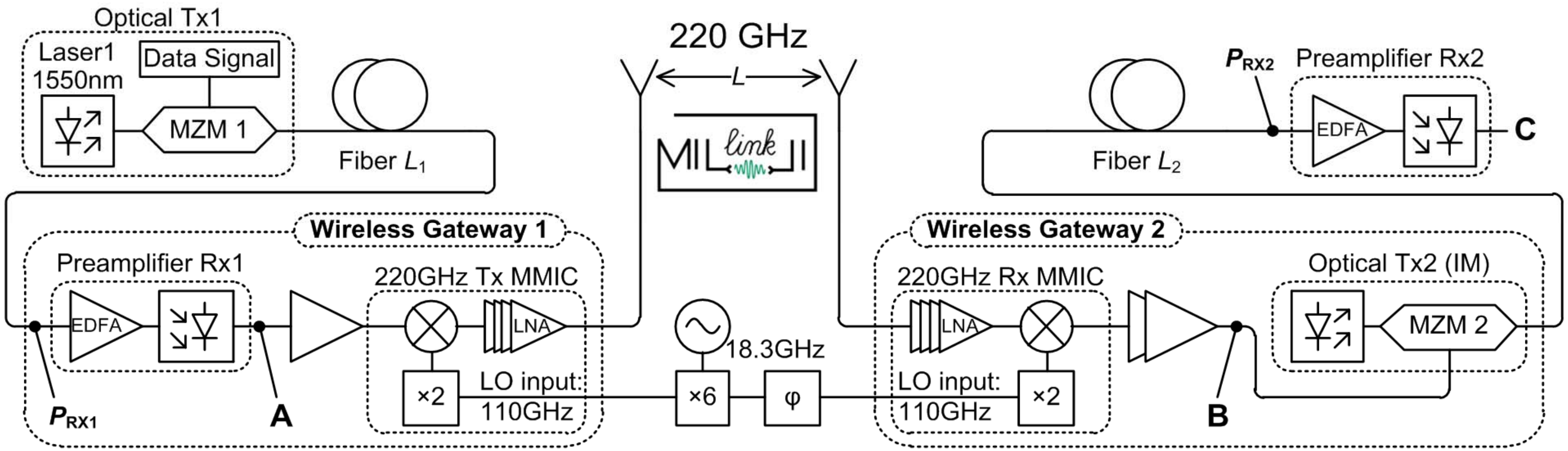
| Setup | Rate | Dist. | Quality |
|---|---|---|---|
| Coherent LO | 25 Gibt/s | 10 m | Q >3 |
| | 15 Gbit/s | 20 m | |
| | Full DVB-S | 20 m | n/a |
| | 30 Gbit/s | n/a | BER < $10^{-3}$ |
| | 16 Gbit/s | 2 m | $Q^2$ > 13.9 |



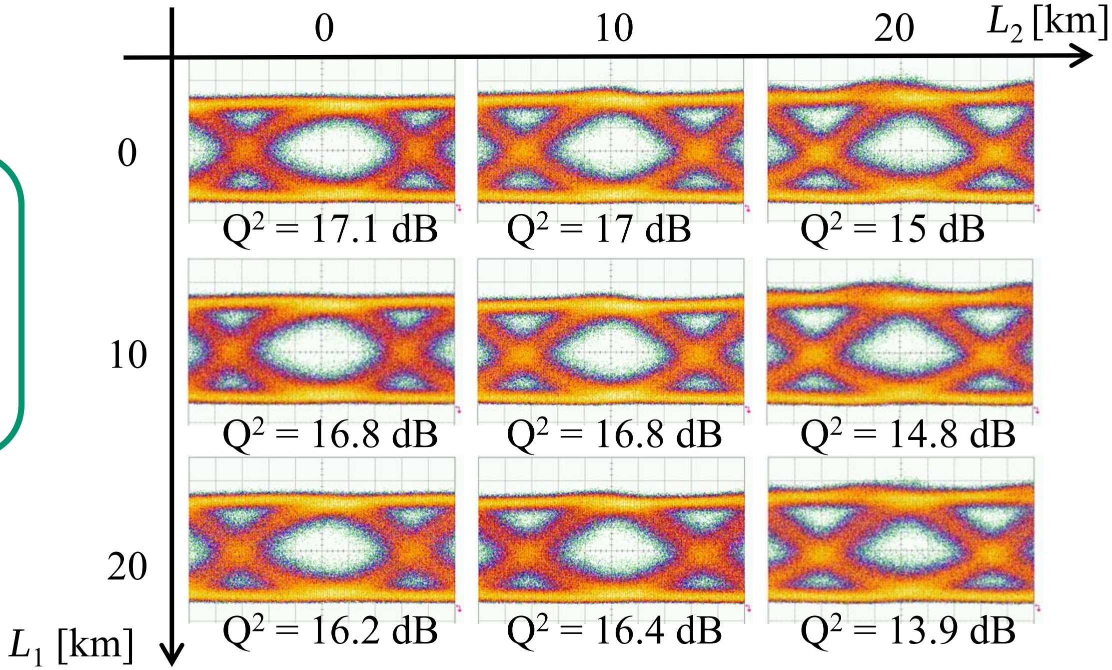




Antes et. al. EuMIC 2011

# Optical – 220 GHz Wireless – Optical Link

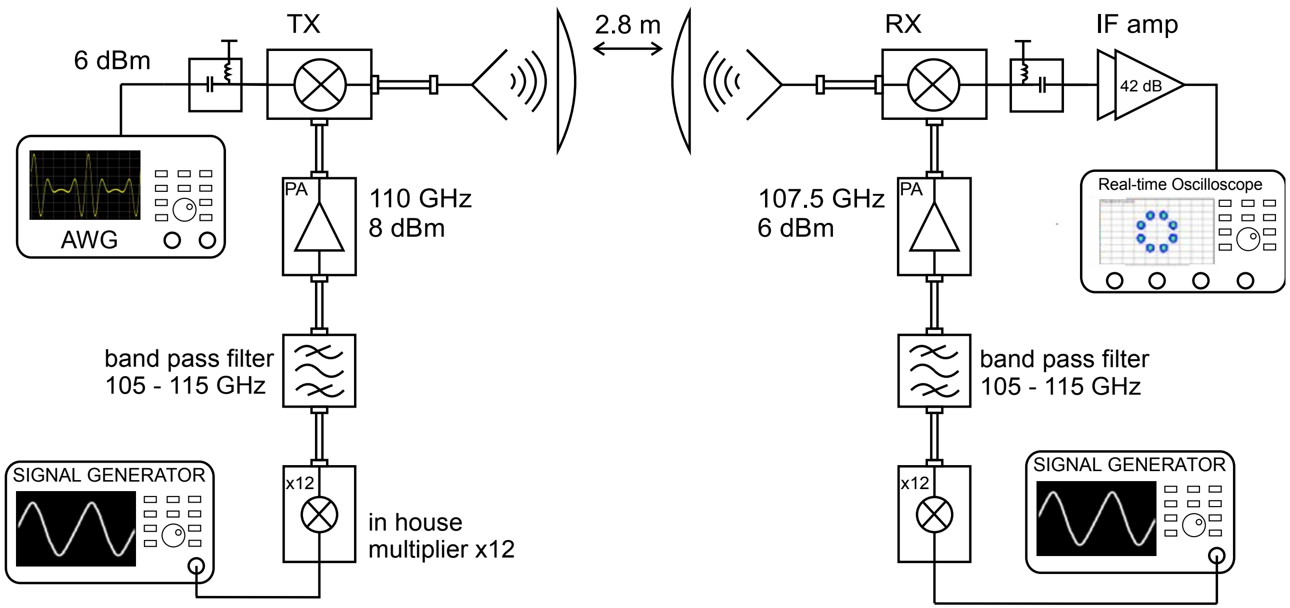


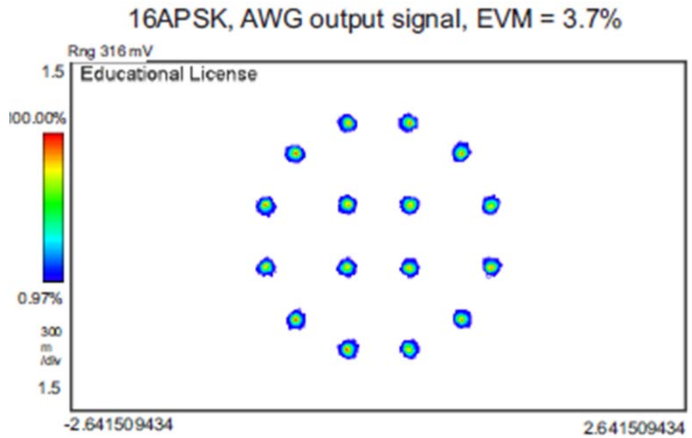

16 Gbit/s NRZ-OOK after 2x20 km fiber span ($P_{RX1} = P_{RX2} = -12$dBm)

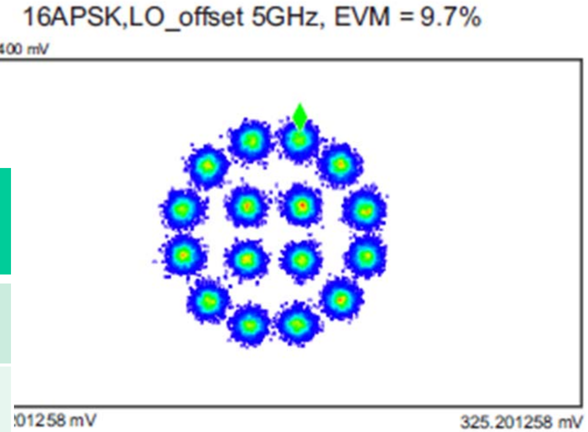



König et. al. OFC 2012

# 220 GHz Transmission Incoherent LO



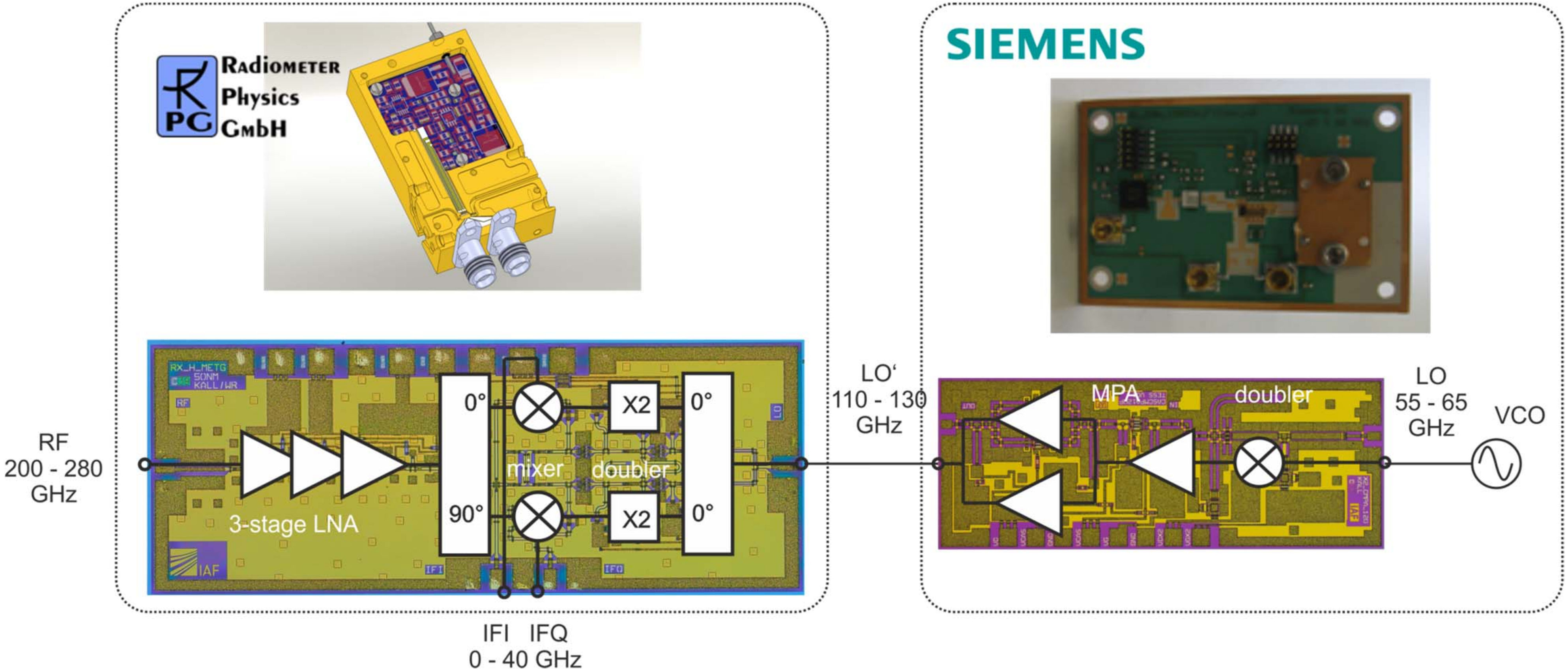




| | Symbol rate | Data rate | EVM | BER[*] |
|---|---|---|---|---|
| **QPSK** | 1 GBd | 2 Gbit/s | 12.4 % | $< 10^{-10}$ |
| | 2 GBd | 4 Gbit/s | 18.1 % | $10^{-8}$ |
| **8PSK** | 1 GBd | 3 Gbit/s | 10.7 % | $10^{-6}$ |
| **16APSK** | 1 GBd | 4 Gbit/s | 9.7 % | - |
| **16QAM** | 1 GBd | 4 Gbit/s | 10.5 % | $10^{-3}$ |

*Schmogrow IEEE Phot. Tech. Letters 2012

# Chip Set for 240 GHz Transmission

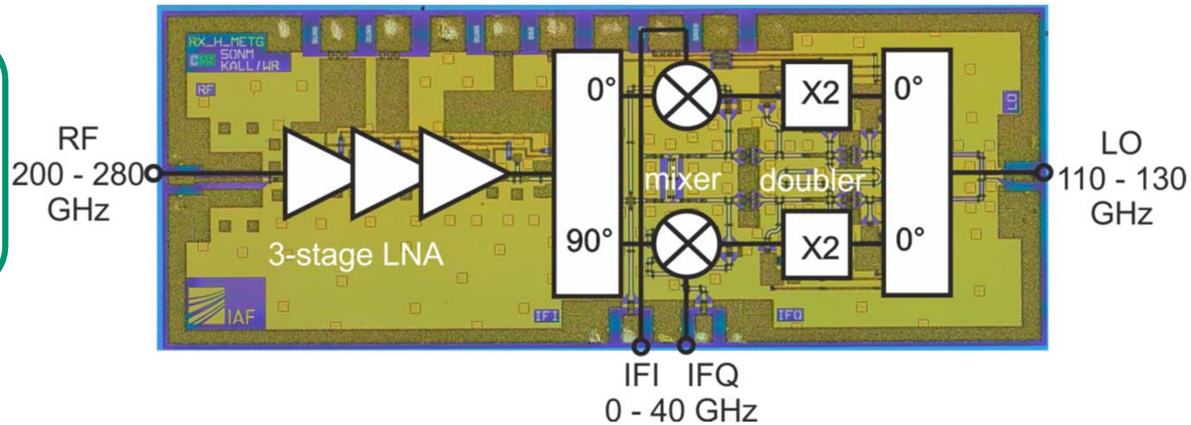


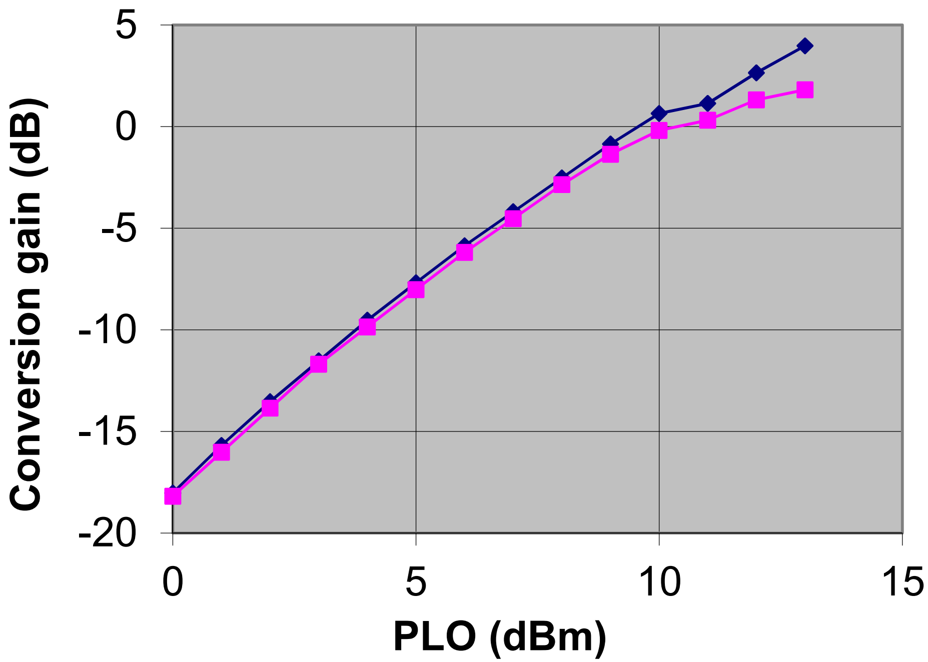

| | | | |
|---|---|---|---|
| $f_{RF,c}$ | 240 GHz | $B_{BB}$ | 40 GHz |
| $B_{RF}$ | 80 GHz | $P_{tx}$ | 0 dBm (excl. PA) |
| $f_{LO}$ | 55–65 GHz | $NF_{rx}$ | ca. 6.8 dB |
| $f_{LO}$ | 110-130 GHz ($n$ = 2 ) | $G_{rx/Gtx}$ | n/a |

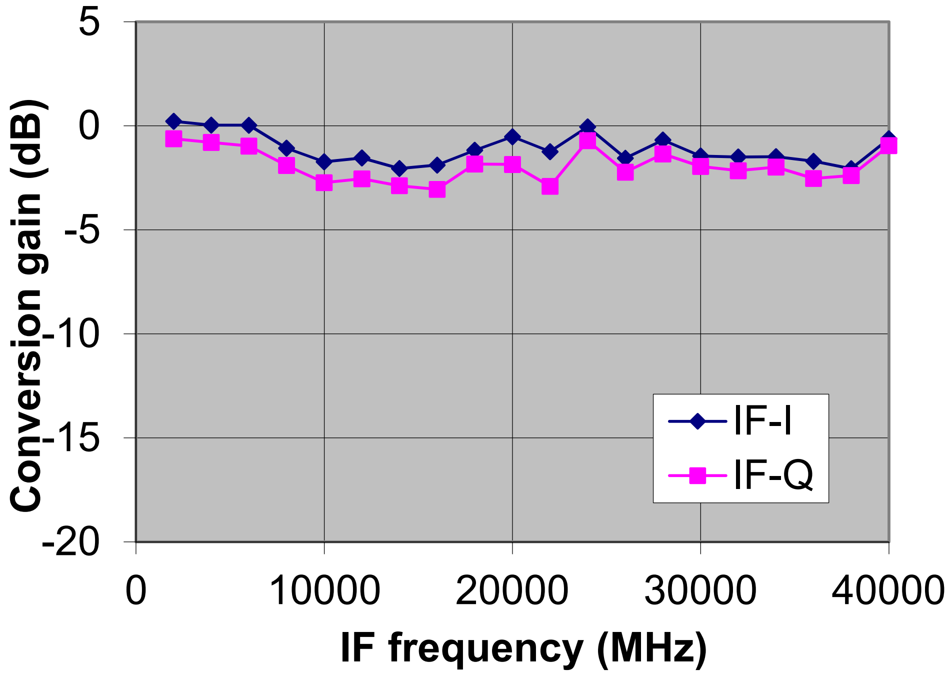
# 240 GHz Rx MMIC

LNA – fund. Mixer – LO doubler
IQ channels
Also as Tx

50 nm mHEMT, 2.5 x 1 $mm^2$

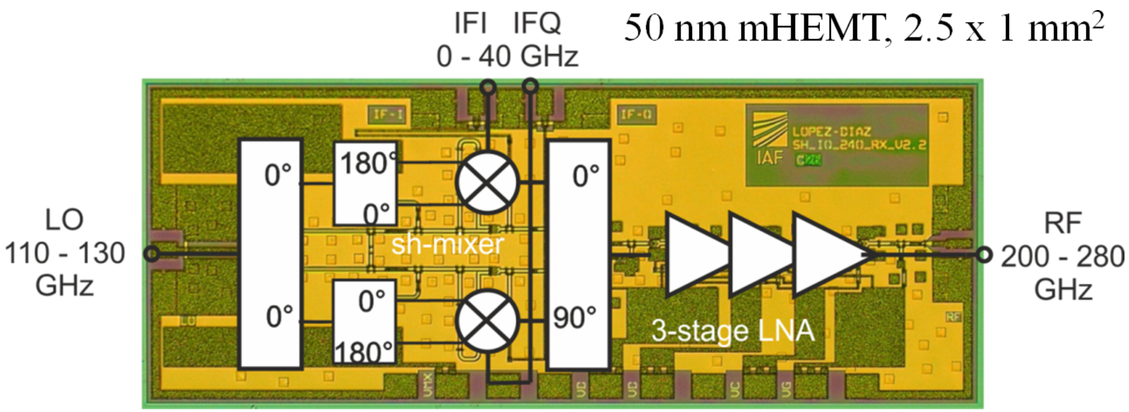


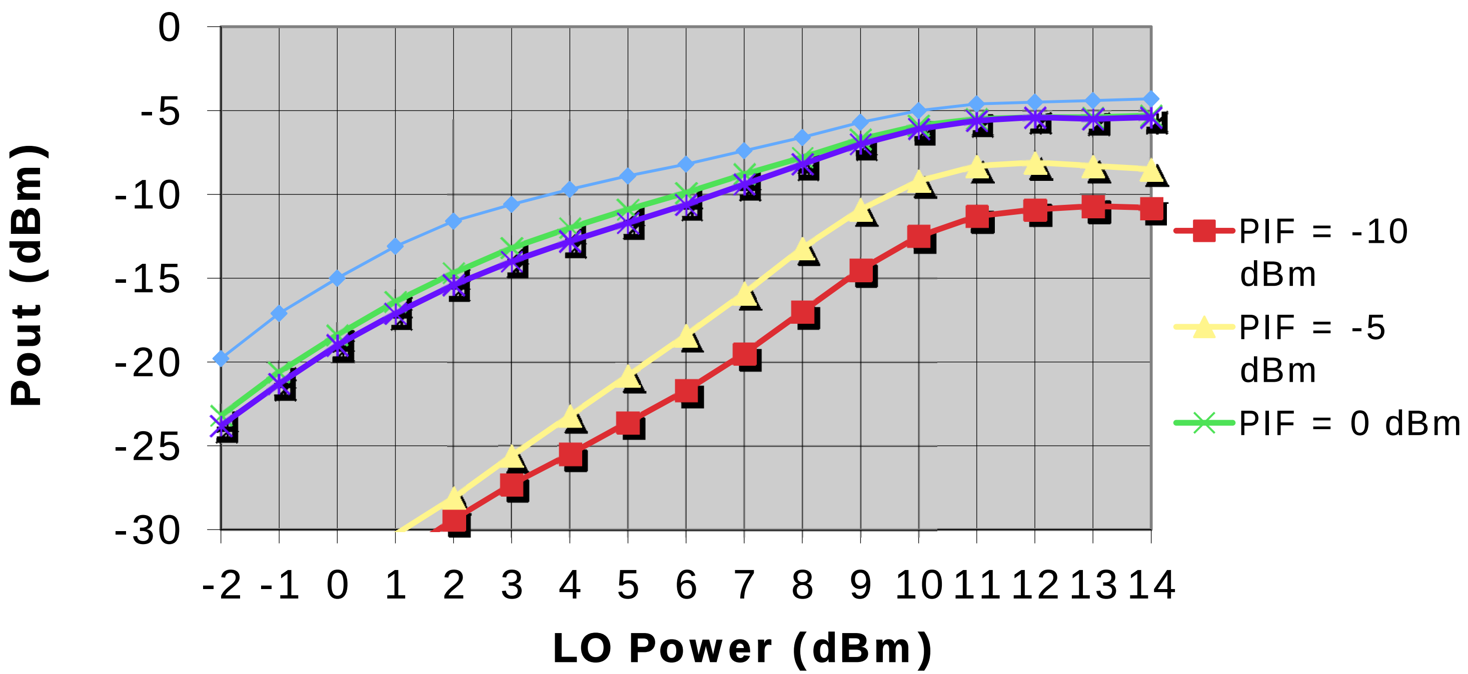



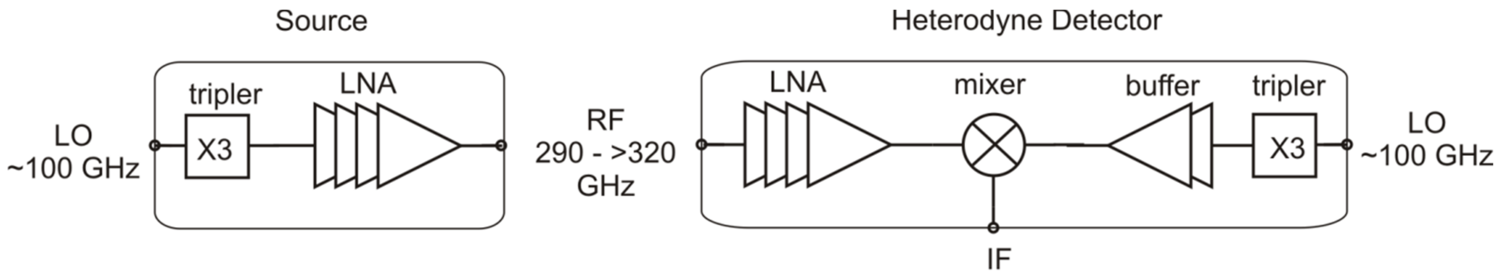
# 240 GHz Tx MMIC

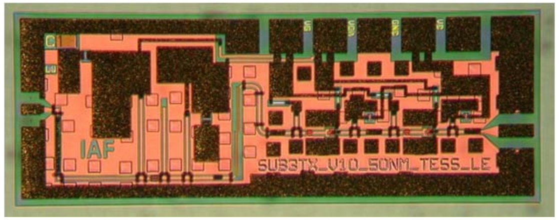
LNA (Tx) – subharm. Mixer
IQ channels
Also as Rx

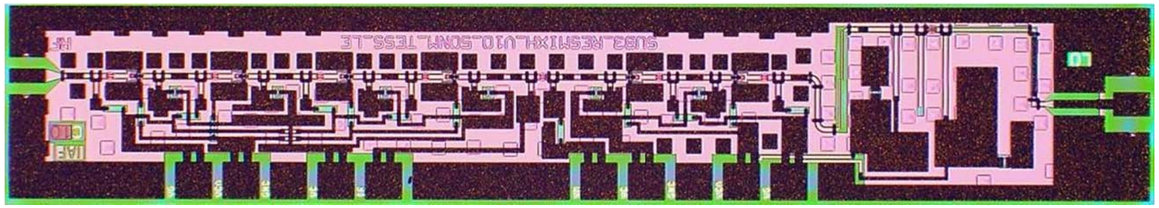


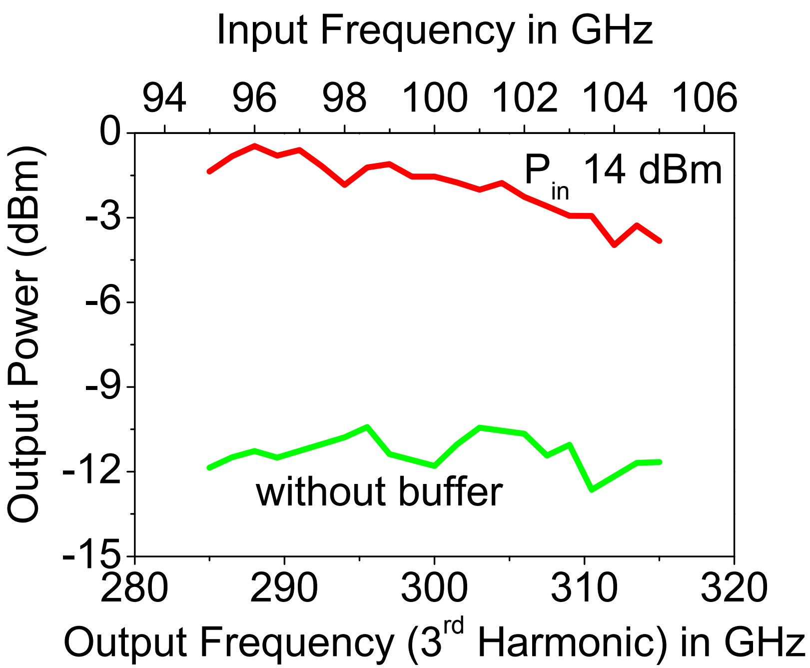



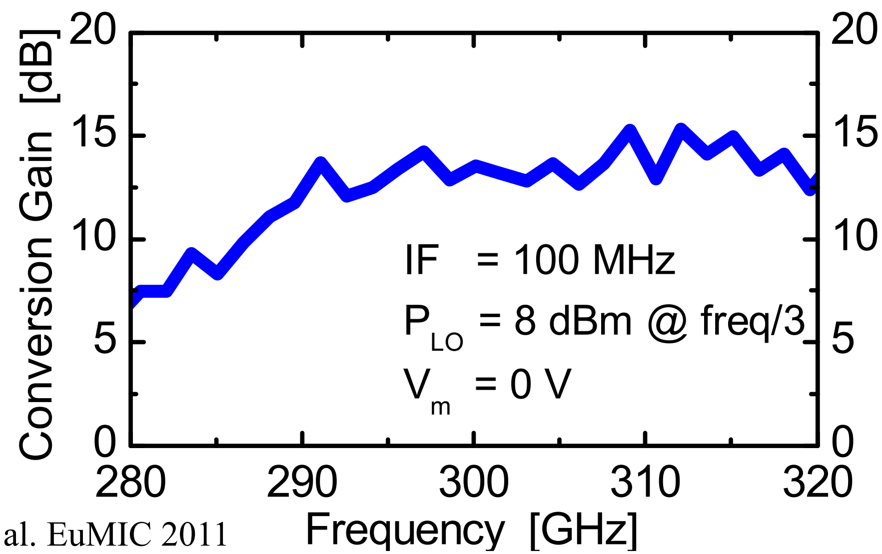
# 300 GHz Source and Receiver





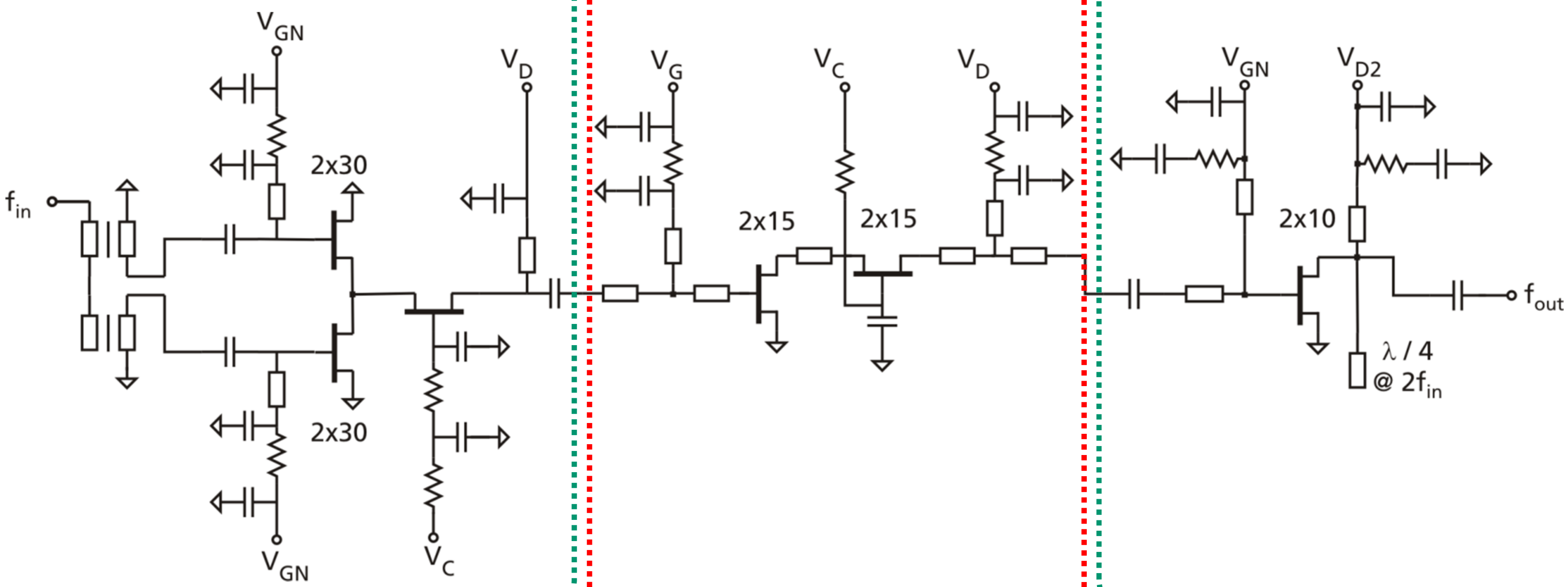

Lewark et. al. EuMIC 2011
Tessmann et. al. CSICS 2011

# 480 GHz Frequency Quadrupler

## Doubler
**balanced (Marchand) class-B cascode FETs**

## Amplifier
**Cascode FETs**

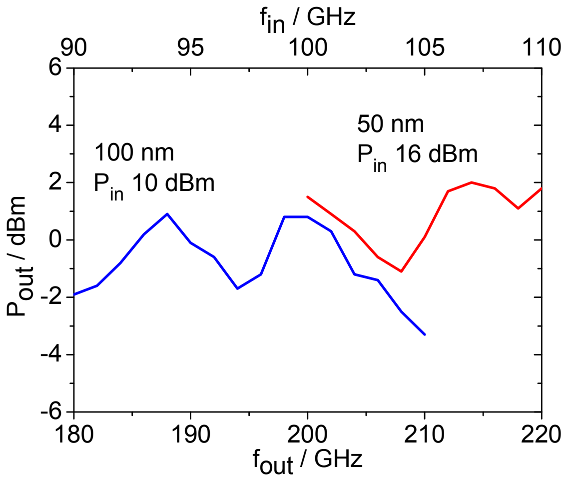
## Doubler
**single-ended class-B FET λ/4 fund. suppression**



# 480 GHz Frequency Quadrupler

## Doubler

**balanced (Marchand) class-B cascode FETs**




$P_{DC}$ 50 mW (w/ $P_{RF}$)

## Amplifier

**Cascode FETs**

**ca. 2 dBm Psat**

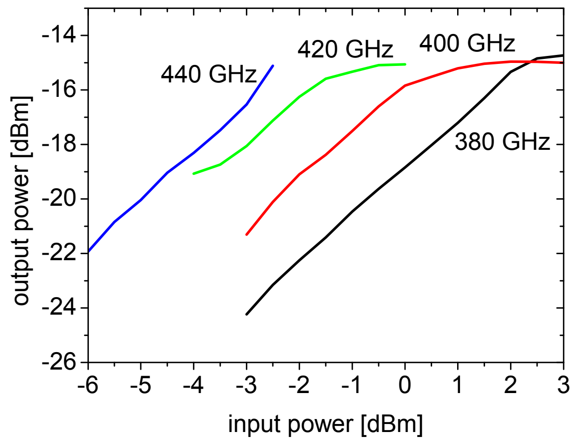
**input power backoff**

**reduced load/source pulling**

$P_{DC}$ 60 mW

## Doubler

**single-ended class-B FET**
**λ/4 fund. suppression**

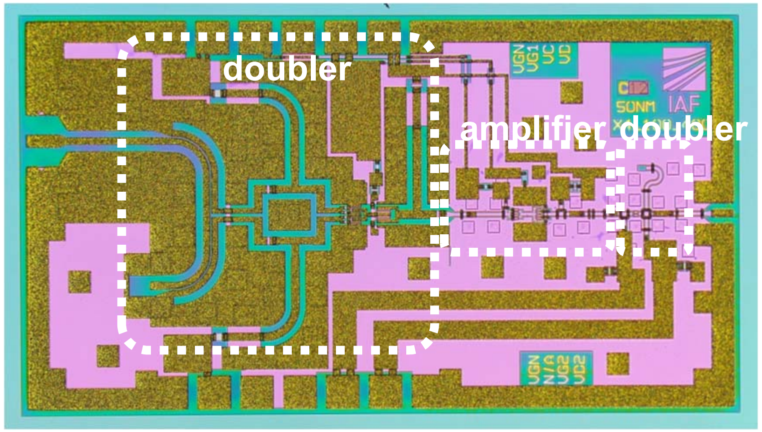



$P_{DC}$ 11 mW (w/ $P_{RF}$)

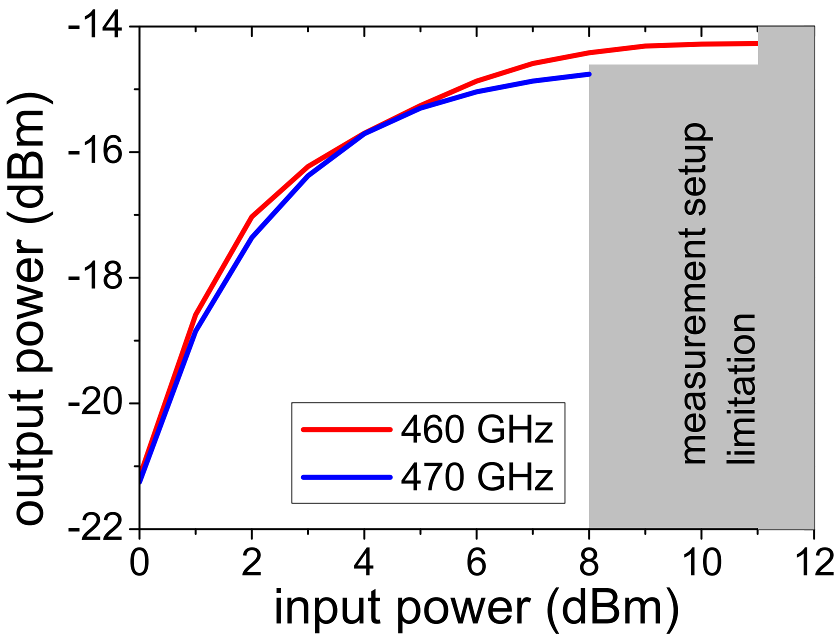
# 480 GHz Frequency Quadrupler

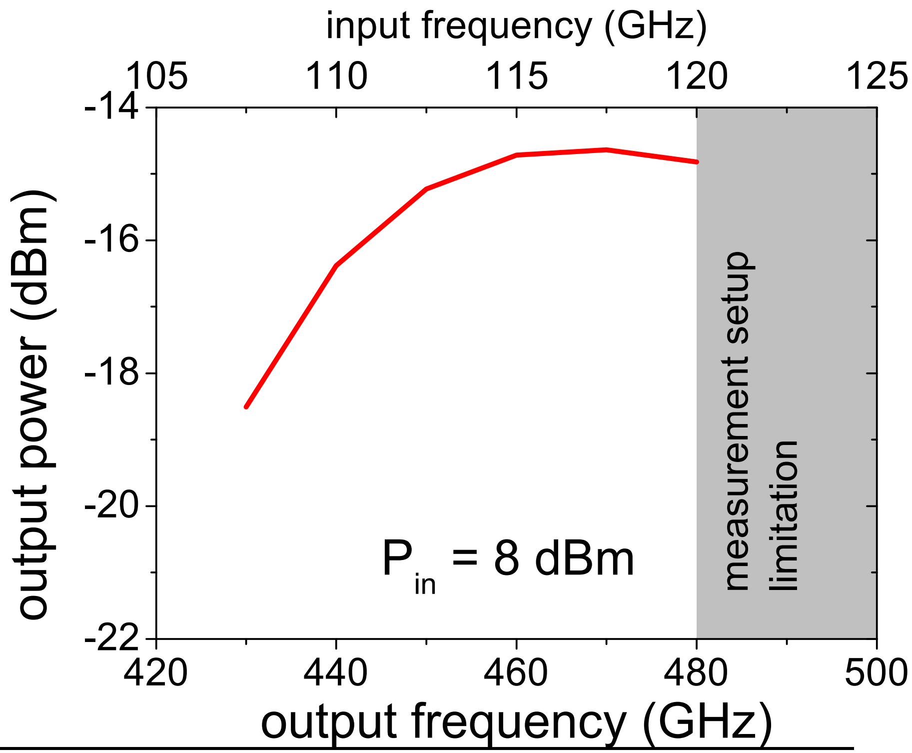
Output power:
 -14.3 dBm

Bandwidth:
 >45 GHz
 435...>480 GHz

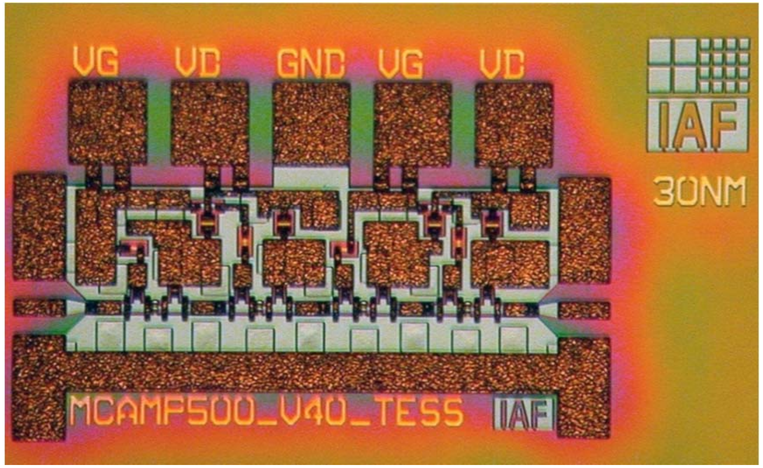



1.75 x 1 mm$^2$
35 nm mHEMT (fT/fmax 515/900)

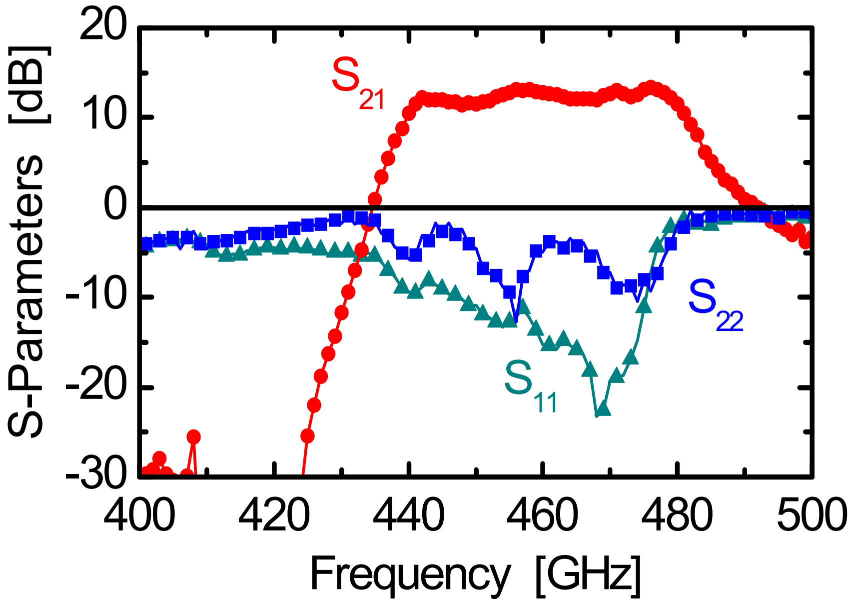


# Four-Stage 480 GHz Amplifier S-MMIC



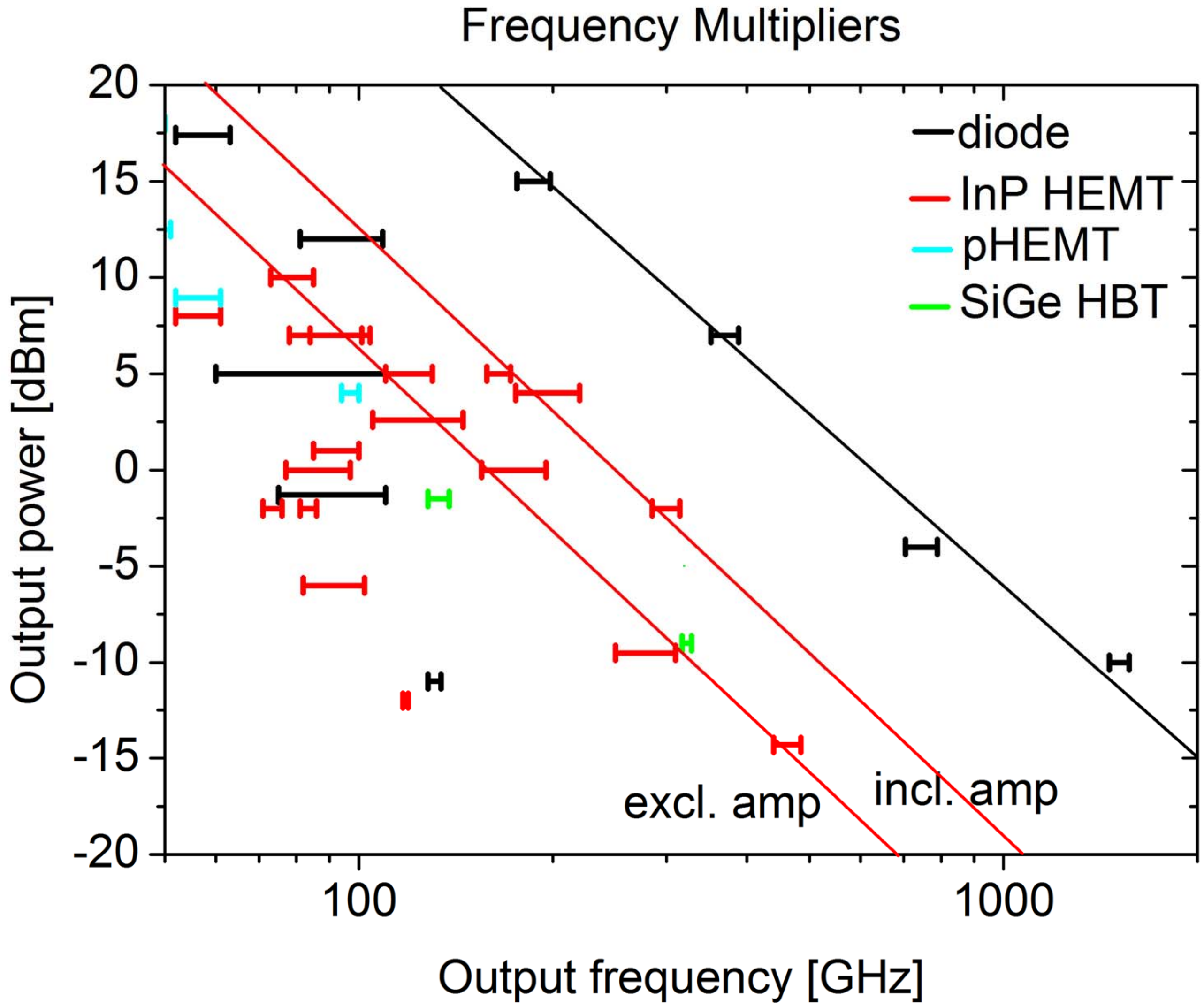

$0.61 \times 0.37$ mm$^2$
35 nm mHEMT




- reactively matched common source stages
- gate width: $2 \times 5$ µm

- 13.4 dB @ 476 GHz
- >10.5 dB @ 440...481 GHz
- 32 mW (Vd = 1.2 V, Id = 27 mA)
- simulated NF = 9.9 dB @ 480 GHz

# State-of-the-Art: Multipliers



# Chip Set Overview