Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: FEC Interleaving Proposal for the FSK PHY

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Re: FEC interleaving in the TG4k FSK PHY

Abstract: This contribution is prepared to identify recommendations to TG4k.

Purpose:

Introduction

- The draft states the *FEC scheme* is as captured in 16.3.2.6, thus adopting the FEC scheme of the *MR-OQPSK PHY* from the 802.15.4g amendment.
  - The FEC scheme uses convolutional encoding on both the PHR and payload.
  - The PHR is an independent code block from the PSDU.
  - The PHR and PSDU are independently terminated with tail bits.
- The draft states the *interleaving scheme* is as captured in 16.1.2.5, adopting the interleaving scheme of the *MR-FSK PHY* from the 802.15.4g amendment.
  - The code block adopted has a fixed size of 32 coded bits (4x4 coded symbols).
- Both FEC and interleaving are controlled via PIB attributes.

FEC and interleaving schemes adopted from different PHYs.

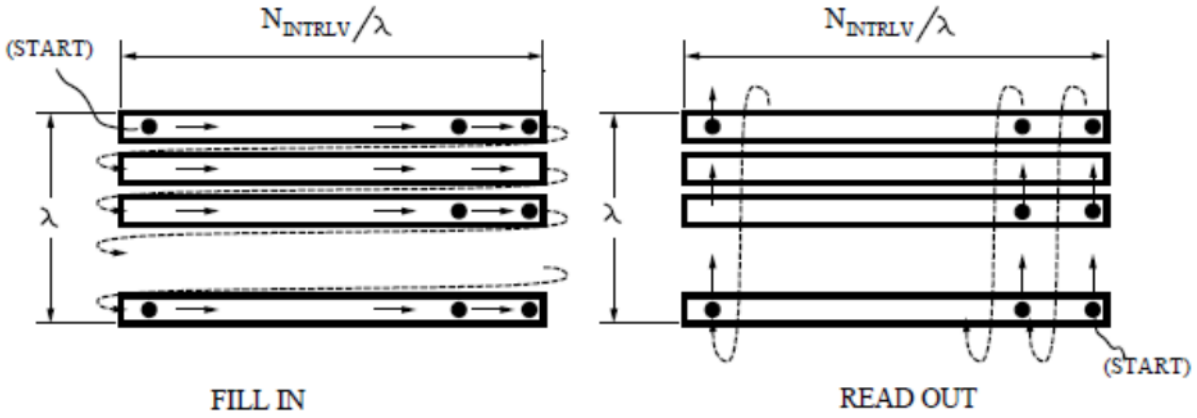
Issues

- The PHR is either 8 or 16 bits long prior to encoding, plus 6 tail bits, thus 28 or 44 bits long after FEC, yet the interleaving code block is fixed at 32 coded bits.
- As a result, the PHR does not fit evenly in a coded block and thus cannot be processed as an independent code block.
- PSDU bits can no longer be processed separately from the PHR bits, which is inconsistent with the rest of draft.
- Pad bit insertion is calculated in the FEC algorithm using assumptions about the interleaving block which are no longer true.

Modifications necessary to make the FEC and interleaving schemes compatible.

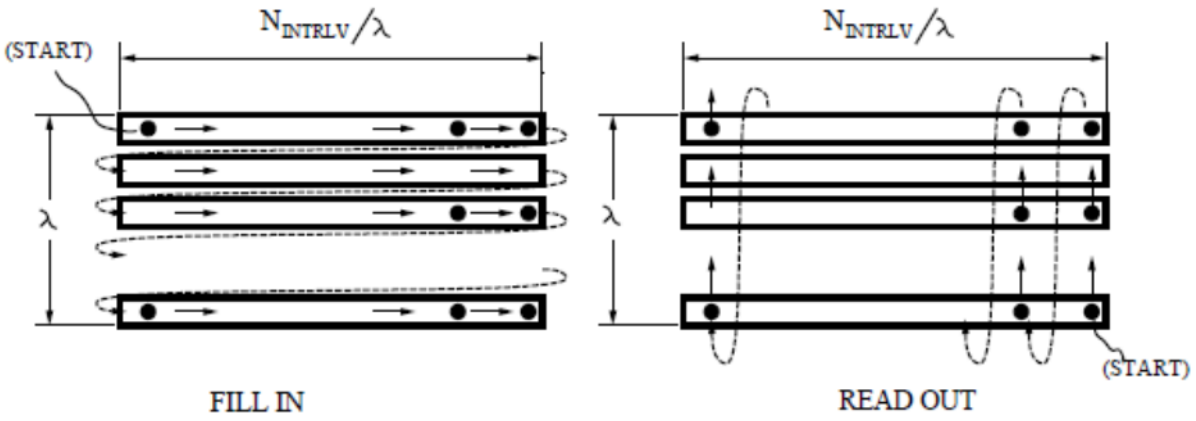
Interleaving Code Block Design

- Consider a write-in row/read-out column interleaving scheme shown here:



- The interleaver breaks a burst error of size S into m bursts of size S/m, where m is the degree of the interleaving.
- Constraint is S/m < t, where t is correcting capability of the convolutional code.
- The larger the degree of interleaving, the more likely the constraint can be met.
- In the MR-OQPSK PHY, for the same t, lambda and Nintrlv/lambda >= 6.

Interleaving Proposal



- Use separate interleaving code blocks for the PHR and PSDU.
- For PHR interleaving, use dual code blocks sized for the dual PHR length:
  - Nintrlv = Nintrlv(phr,short) = 4 x 7 = 28 coded bits when encoding the short header
  - Nintrlv = Nintrlv(phr,long) = 4 x 11 = 44 coded bits when encoding the long header.
- For PSDU interleaving, use Nintrlv = Nintrlv(psdu) = 6 x 12 = 72 coded bits
  - Note Nintrlv(psdu) = Nintrlv(phr,short) + Nintrlv(phr,long) thus RAM can be reused

Pad Bit Computation

- Use the following algorithm, where:
  - Nintrlv = Nintrlv(psdu)
  - LENGTH = PSDU length size in octets.

Prior to the convolutional encoding of the PSDU, the sequence of PSDU information bits $b = \{b_0, b_1, \ldots, b_{8 \times \text{LENGTH}-1}\}$, with its length (LENGTH) measured in octets, shall be extended by appending a termination sequence of six bits, all zero, and a sequence of additional bits (pad bits) as shown in Figure 139. The pad bits shall be set to zero and the number of pad bits, N_{PAD}, is computed from the number of blocks, N_B, the total number of uncoded bits, N_D, and the interleaver depth, N_{INTRLV}, as follows:

$$N_B = \text{ceiling}((8 \times \text{LENGTH} + 6)/(N_{\text{INTRLV}}/2)) \quad (8)$$

$$N_D = N_B \times (N_{\text{INTRLV}}/2) \quad (9)$$

$$N_{\text{PAD}} = N_D - (8 \times \text{LENGTH} + 6)$$

The function ceiling(.) is a function that returns the smallest integer value greater than or equal to its argument value.

PHR bits	000000	PSDU bits	000000	pad bits

Figure 139—PHR and PSDU extension prior to encoding

A Receiver Algorithm

- Following the receipt of SHR, run Stage1 and Stage2 serially or in parallel.
- Stage1:
  - Set Nintrlv = Nintrlv(phr,short) and deinterleave.
  - Demodulate the PHR Length bit assuming a short PHR.
  - If PHR Length == 0 (short header)
    - Declare Stage1 Success and proceed demodulating the rest of the PHR.
    - Go to Stage3
  - If PHR Length == 1 (long header), declare Stage1 Fail. Go to Stage2 if serial or Stage3.
- Stage2:
  - Set Nintrlv = Nintrlv(phr,long) and deinterleave.
  - Demodulate PHR Length bit assuming long PHR.
  - If PHR Length == 1 (long header)
    - Declare Stage2 Success and proceed demodulating the rest of the PHR.
    - Go to Stage3
  - If PHR Length == 0 (short header), declare Stage2 Fail. Go to Stage3.
- Stage3:
  - If XOR(Stage1 Success, Stage2 Success), go to Stage4.
  - Otherwise, if both succeeded, pick one with higher confidence metric above some threshold. Go to Stage4.
  - Else cease packet receipt.
- Stage4: set Nintrlv = Nintrlv(psdu), and de-interleave/demodulate PSDU.

Conclusions

- The current FEC and interleaving schemes in the FSK PHY are inconsistent.
- An interleaving proposals identified to address the inconsistencies. The interleaving scheme and PAD bit computation proposed, along with an example of a receiver algorithm.
- The proposal uses separate interleaving blocks for the PHR and PSDU, appropriately sized, consistent with the TG4k FSK PHY and FEC scheme selected.