**IEEE P802.15**

**Wireless Personal Area Networks**

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Contents

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1. Overview
	1. General
	2. Scope
	3. Purpose
2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

1. Definitions, acronyms, and abbreviations

For the purposes of this document, the following terms and definitions apply. The *IEEE Standards Dictionary: Glossary of Terms & Definitions* should be consulted for terms not defined in this clause.[[2]](#footnote-2)

1. General description
2. MAC protocol
3. MAC services
4. Security
5. General PHY requirements
6. PHY Services
7. O-QPSK PHY
8. Binary phase-shift keying (BPSK) PHY
9. Amplitude shift keying (ASK) PHY
10. Chirp spread spectrum (CSS) PHY
11. UWB PHY
12. GFSK PHY
13. SUN PHYs
14. LECIM PHYs
	1. DSSS PHY specification
		1. LECIM DSSS PPDU format

For convenience, the PPDU structure is presented so that the leftmost field as written in this standard shall be transmitted or received first. All multiple octet fields shall be transmitted or received least significant octet first, and each octet shall be transmitted or received least significant bit (LSB) first.

The PPDU shall be formatted as illustrated in Figure 1.



Figure PPDU Format

* + - 1. SHR

The SHR or Synchronization Header is a field which may be used for obtaining frequency, symbol, and frame synchronization. It consists of two sub-fields, the preamble and the start of frame delimiter (SFD). It is possible to recover a fixed length frame without the use of a SFD, or SHR.

* + - * 1. Preamble

The preamble is a sub-field which may be used to obtain symbol timing and frequency offset. A preamble length of 0, 2, 4 octets may be commissioned.

Preamble16 = [1 1 0 0 0 0 0 1 0 1 0 0 1 1 0]

Preamble32 = [ T.B.D. ]

* + - * 1. SFD

The SFD or start frame delimiter is a sub-field which may be used to indicate the beginning of the frame.

SFD = [ T.B.D. ]

* + - 1. PHR

The PHR or PHY Header is a field used to indicate the length of a variable length PHY payload. When the PHY payload is commissioned to a fixed size, the PHR is elided. For variable length PHY payloads of up to 128 octets, the PHR is a one octet and represents a payload of n+1 octets where n = 0..127. For variable length PHY payloads of 129-2048 octets, the PHR is two octets as illustrated in Figure 1.

* + 1. Modulation and spreading
			1. Data Rate

The data rate and bandwidths are band and/or region specific. A table of chip rates and bandwidths will be added here along with text describing the resulting data rates. For example:

|  |  |  |
| --- | --- | --- |
| **PHY****(MHz)** | **Frequency Band****(MHz)** | **Region/Availability** |
| **Modulation** | **Chip rate****(kchip/s)** |
| 400 | 400-470 | Korea | BPSK/? | 100(12.5 KHz channels bonded) |
| 470 | 470-510 | China | BPSK/O-QPSK |  |
| BPSK/O-QPSK |  |
| BPSK/O-QPSK |  |
| 780 | 779-787 | China | BPSK/O-QPSK |  |
| BPSK/O-QPSK |  |
| BPSK/O-QPSK |  |
| 868 | 863-870868.300868.950869.525 | EU/CEPT | BPSK/O-QPSK | 100 |
| 902 | 902-928 | Americas, Australia | BPSK/O-QPSK | 1000/? |
| **917** | **917-923.5** | **South Korea** | **BPSK/O-QPSK** |  |
| **BPSK/O-QPSK** |  |
| **BPSK/O-QPSK** |  |
| 920 | 920-928 | Japan | BPSK/O-QPSK | 200 |
| BPSK/O-QPSK | 600 |
| BPSK/O-QPSK | 1000 |
| 2450 | 2400-2483.5 | Worldwide | BPSK/O-QPSK | 1000, 2000? |

Channelization

902 902-928 Americas, Australia2400 2400-2483.5

The channel numbers, and spacing are as follows:

2402 + ((n-1) \* 1.99MHz)

Where n = 1..41

904 + ((n-1) \* 1.99MHz)

Where n = 1..15

The 1.99MHz spacing is used to minimize false lock and interference from spurious.

* + - 1. Reference modulator diagram

The functional block diagram in Figure 2 is provided as a reference for specifying the LECIM DSSS PHY modulation. All binary data contained in the SHR, PHR, and PSDU shall be encoded using the modulation shown in Figure 2.



Figure Reference modulator diagram

* + - 1. Convolutional FEC encoding

The convolutional encoder is the same as specified in the 802.11 standard.

The PSDU, and tail/pad parts, shall be coded with a convolutional encoder of coding rate R = 1/2. The convolutional encoder shall use the industry-standard generator polynomials, g0 = 1338 and g1 = 1718, of rate R = 1/2, as shown in Figure 3 below.



Figure 3 Convolutional encoder (k = 7)

* + - 1. Interleaver

The output of the convolutional coder is interleaved using a pruned bit reversal interleaving (PBRI) algorithm.

Below are examples of bit reverse interleavers for 3 fragment sizes (256, 384, 512). Fragment sizes that are not powers of two e.g. 384 employ pruning.

**256 symbols**

If the input sequence into the interleaver is represented by

[S0 S1 … S255]

Then the output sequence of the interleaver can be described as

[S0 S16 ..SN s255]

The value N for the Mth output is determined as the bit-reversal of the value M.

Representing the value M as a binary representation

M = [m7 m6 … m0] where mi are the binary digits, then

N = [m0 m1..m7]

where M is incremented sequentially from 0 to 255.

The sequence of N is thus,

     0   128    64   192    32   160    96   224    16   144    80   208    48   176   112   240     8   136    72   200    40   168   104   232    24   152    88   216    56   184   120

   248     4   132    68   196    36   164   100   228    20   148    84   212    52   180   116   244    12   140    76   204    44   172   108   236    28   156    92   220    60   188   124   252     2   130    66   194    34   162    98   226    18   146    82   210    50   178   114   242    10   138    74   202    42   170   106   234    26   154    90   218    58   186   122   250     6   134    70   198    38   166   102   230    22   150    86   214    54   182   118   246    14   142    78   206    46   174   110   238    30   158    94   222    62   190   126   254     1   129    65   193    33   161    97   225    17   145    81   209    49   177   113   241     9   137    73   201    41   169   105   233    25   153    89   217    57   185   121   249     5   133    69   197    37   165   101   229    21   149    85   213    53   181   117   245    13   141    77   205    45   173   109   237    29   157    93   221    61   189   125   253     3   131    67   195    35   163    99   227    19   147    83   211    51   179   115   243    11   139    75   203    43   171   107   235    27   155    91   219    59   187   123   251     7   135    71   199    39   167   103   231    23   151    87   215    55   183   119   247    15   143    79   207    47   175   111   239    31   159    95   223    63   191   127   255

**384 symbols**

If the input sequence into the interleaver is represented by

[S0 S1 … S383]

Then the output sequence of the interleaver can be described as

[S0 S16 ..SN s383]

Representing the value M as a binary representation

M’ = [m’8 m’6 … m’0] where mi are the binary digits, then

N = [m’0 m’1..m’8]

where M is incremented sequentially from 0 to 512

and M’ are the ordered set of M whose corresponding N is less than 384

[this is the pruning process]

The sequence of N is thus,

     0   256   128    64   320   192    32   288   160    96   352   224    16   272   144    80   336   208    48   304   176   112   368   240     8   264   136    72   328   200    40   296   168   104   360   232    24   280   152    88   344   216    56   312   184   120   376   248     4   260   132    68   324   196    36   292   164   100   356   228    20   276   148    84   340   212    52   308   180   116   372   244    12   268   140    76   332   204    44   300   172   108   364   236    28   284   156    92   348   220    60   316   188   124   380   252     2   258   130    66   322   194    34   290   162    98   354   226    18   274   146    82   338   210    50   306   178   114   370   242    10   266   138    74

   330   202    42   298   170   106   362   234    26   282   154    90   346   218    58   314   186   122   378   250     6   262   134    70   326   198    38   294   166   102   358   230    22   278   150    86   342   214    54   310   182   118   374   246    14   270   142    78   334   206    46   302   174   110   366   238    30   286   158    94   350   222    62   318   190   126   382   254     1   257   129    65   321   193    33   289   161    97   353   225    17   273   145    81   337   209    49   305   177   113   369   241     9   265   137    73   329   201    41   297   169   105   361   233    25   281   153    89   345   217    57   313   185   121   377   249     5   261   133    69   325   197    37   293   165   101   357   229    21   277   149    85   341   213    53   309   181   117   373   245    13   269   141    77   333   205    45   301   173   109   365   237    29   285   157    93   349   221    61   317   189   125   381   253     3   259   131    67   323   195    35   291   163    99   355   227    19   275   147    83   339   211    51   307   179   115   371   243    11   267   139    75   331   203    43   299   171   107   363   235    27   283   155    91   347   219    59   315   187   123   379   251     7   263   135    71   327   199    39   295   167   103   359   231    23   279   151    87   343   215    55   311   183   119   375   247    15   271   143    79   335   207    47   303   175   111   367   239    31   287   159    95   351   223    63   319   191   127   383   255

**512 symbols**

If the input sequence into the interleaver is represented by

[S0 S1 … S255]

Then the output sequence of the interleaver can be described as

[S0 S16 ..SN s255]

The value N for the Mth output is determined as the bit-reversal of the value M.

Representing the value M as a binary representation

M = [m8 m6 … m0] where mi are the binary digits, then

N = [m0 m1..m8]

where M is incremented sequentially from 0 to 511.

The sequence of N is thus,

 0   256   128   384    64   320   192   448    32   288   160   416    96   352   224   480    16   272   144   400    80   336   208   464    48   304   176   432   112   368   240   496     8   264   136   392    72   328   200   456    40   296   168   424   104   360   232   488    24   280   152   408    88   344   216   472    56   312   184   440   120   376   248   504     4   260   132   388    68   324   196   452    36   292   164   420   100   356   228   484    20   276   148   404    84   340   212   468    52   308   180   436   116   372   244   500    12   268   140   396    76   332   204   460    44   300   172   428   108   364   236   492    28   284   156   412    92   348   220   476    60   316   188   444   124   380   252   508     2   258   130   386    66   322   194   450    34   290   162   418    98   354   226   482    18   274   146   402    82   338   210   466    50   306   178   434   114   370   242   498    10   266   138   394    74   330   202   458    42   298   170   426   106   362   234   490    26   282   154   410    90   346   218   474    58   314   186   442   122   378   250   506     6   262   134   390    70  326   198   454    38   294   166   422   102   358   230   486    22   278   150   406    86   342   214   470    54   310   182   438   118   374   246   502    14   270   142   398    78   334   206   462    46   302   174   430   110   366   238   494    30   286   158   414    94   350   222   478    62   318   190   446   126   382   254   510     1   257   129   385    65   321   193   449    33   289   161   417    97   353   225   481    17   273   145   401    81   337   209    465    49   305   177   433   113   369   241   497     9   265   137   393    73   329   201   457    41   297   169   425   105   361   233   489    25   281   153   409    89   345   217   473    57   313   185   441   121   377   249   505     5   261   133   389    69   325   197   453    37   293   165   421   101   357   229   485    21   277   149   405    85   341   213   469    53   309   181   437   117   373   245   501    13   269   141   397    77   333   205   461    45   301   173   429   109   365   237   493    29  285   157   413    93   349   221   477    61   317   189   445   125   381   253   509     3   259   131   387    67   323   195   451    35   291   163   419    99   355   227   483    19   275   147   403    83   339   211   467    51   307   179   435   115   371   243   499    11   267   139   395    75   331   203   459    43   299   171   427   107   363   235   491    27   283   155   411    91   347   219   475    59   315   187   443   123   379   251   507     7   263   135   391    71   327   199   455    39   295   167   423   103   359   231   487    23   279   151   407    87   343   215   471    55   311   183   439   119   375   247   503    15   271   143   399    79   335   207   463    47   303   175   431   111   367   239   495    31   287   159   415    95   351   223   479    63   319   191   447   127   383   255   511

* + - 1. Differential encoding

As described in 802.15.4-2011 BPSK PHY section 11.2.3.

* + - 1. Bit-to-symbol and symbol-to-chip encoding

The bit-to-symbol mapper converts bits into binary symbols through the mapping:

$$x\left[n\right]= \left\{\begin{matrix}1, if b\left[n\right]=0\\-1, if b\left[n\right]=1\end{matrix}\right.$$

These binary symbols are then spread to chip-rate with spreading factor SF. This process is illustrated explicitly in Figure 3 below where SF = 8. The symbols are first up-sampled SF times and interpolated using a scaled boxcar filter, i.e. the symbol is repeated SF times at chip-rate. Note that this is a mathematical representation of the direct sequence spreading operation. This process can be implemented in an alternative manner that is mathematically equivalent. The up-sampled symbols are multiplied by a specified Gold Code to create the spread signal.



Figure Bit-to-chip diagram



Figure Boxcar filter

* + - * 1. Gold code generator

Gold Code sequences are a large family of easily parameterized PN sequences with good periodic cross-correlation and off-peak auto-correlation properties. A Gold Code sequence is derived from the binary addition (XOR) of two Maximum Length Sequences (m-sequences, or MLS) as illustrated in Figure 5. The m-sequences are generated using Fibonacci Linear Feedback Shift Registers (LFSR). Each LFSR is constructed from primitive (or prime) polynomials over Galois Field 2 (GF[2]). The resulting sequences thus constitute segments of a set of Gold sequences. The specific m-sequences listed below are the preferred pair as described in the 3rd Generation Partnership Project (3GPP) Technical Specification 25.213. The Gold Sequence can be parameterized by setting the Initialization Vector of LFSR2 to different values (LFSR1 is always initialized to 0x1).

* m = 25 (Length of LSFR)
* n = 2m-1 = 33,554,431 (Length of Gold Code)
* n+2 = 33,554,433 (Total Gold Sequences) = {a, b, a\*b, a\*Tb, a\*T2b, …}

LFSR (MLS) generator polynomials:

* p1(x) = x25 + x3 + 1
* p2(x) = x25 + x3 + x2 + x + 1



Figure 6 Gold code generator

* + - 1. BPSK/O-QPSK modulation
				1. BPSK modulation

Same as 802.15.4-2011 BPSK PHY section 11.2.5?

The chip sequences are modulated onto the carrier using BPSK with raised cosine pulse shaping (roll-off

factor = 1) where a chip value of one corresponds to a positive pulse and a chip value of zero corresponds to a negative pulse.

Chip rates/bands shown in table xyz.

Pulse shape

As described in 802.15.4-2011 BPSK PHY section 11.2.5.1.

Chip transmission order

During each symbol period, the least significant chip is transmitted first, and the most significant chip is transmitted last.

(further clarification on what is meant by least and most significant bit)

* + - * 1. O-QPSK modulation

The chip sequences representing each data symbol are modulated onto the carrier using O-QPSK with pulse shaping. For even-indexed symbol, the even-indexed chips are modulated onto the in-phase (I) carrier, and odd-indexed chips are modulated onto the quadrature-phase (Q) carrier. For odd-indexed symbol, even-indexed chips are modulated onto the quadrature-phase (Q) carrier, and odd-indexed chips are modulated onto the in-phase (I) carrier. To form the offset between I-phase and Q-phase chip modulation, the Q-phase chips shall be delayed by Tc with respect to the I-phase chips, as illustrated in Figure 6, where Tc is the inverse of the chip rate.



Figure 7 O-QPSK chip modulation

17.1.2.7.2.1 Pulse shape**4g 16.3.2.13 Modulation parameters for O-QPSK? (why multiple shapes?)**

Chip transmission order

Same as 802.15.4-2011 BPSK PHY section 10.2.7?

During each symbol period, the least significant chip, C0, is transmitted first, and the most significant chip, CSF-1, is transmitted last.

(further clarification on what is meant by least and most significant bit or reference Figure 6 CSF-1)

* 1. FSK PHY specification

# (informative)Bibliography

1. The Institute of Electrical and Electronics Engineers, Inc.

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