IEEE P802.15
Wireless Personal Area Networks

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Re:	Comment Resolution for TG4g Sponsor Ballot	
Abstract	This document presents examples of the processing to generate FSK packets.	
Purpose	Proposed resolution for Comment ID 36	
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Release	The contributor acknowledges and accepts that this contribution becomes the property of IEEE and may be made publicly available by P802.15.	

Proposed resolution to CID 36: Revised. Create Annex M as shown below.

Annex M
(informative)
Examples of encoding a frame for the MR-FSK PHY

This annex provides 14 examples of encoding a frame for the MR-FSK PHY as described in 16.1. In particular, generation of the PPDU bit sequence is described in detail. The first 6 examples use no coding, and the last 8 examples use convolutional coding. The examples are numbered from M.1 to M.14 and correspond to the scenarios in Table M.1. The frequency band used in these examples is the 915 MHz band, and these examples use Operating Mode #1 for the 2FSK examples.

In these examples, all binary sequences of length *n* are treated as bit strings:
$b_0\ b_1$ ..... b_{n-1}
The corresponding entries are processed b_0 first to b_{n-1} last.

In all these examples mode switch is not used, and the 4-octet FCS is used. In addition, the PIB attribute phyFSKPreambleLength is set to 4 so that 4 octets are used for all preambles.

Table M.1 – Scenarios for MR-FSK

Example Number	Modulation	Coding	Interleaving	Data Whitening	phyMRFSKSFD
M.1	2FSK	None	Off	Off	0
M.2	2FSK	None	Off	Off	1
M.3	2FSK	None	Off	On	0
M.4	4FSK	None	Off	Off	0
M.5	4FSK	None	Off	Off	1
M.6	4FSK	None	Off	On	0
M.7	2FSK	NRNSC	On	Off	0
M.8	2FSK	NRNSC	On	On	0
M.9	2FSK	RSC	Off	Off	0
M.10	2FSK	RSC	Off	On	0
M.11	2FSK	RSC	On	Off	0
M.12	2FSK	RSC	On	On	0
M.13	4FSK	NRNSC	On	Off	0
M.14	4FSK	NRNSC	On	On	0

In all examples the message encoded is a PSDU of 7 octets shown below. The message constitutes an acknowledgment frame with a 3-octet MHR and a 4-octet FCS, as defined in 5.2.1.9. The bit sequence of the example PSDU is: 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

The encoding illustration goes through the following stages:
a) Generating the bit sequence of the SHR
b) Generating the bit sequence of the PHR
c) Generating the bit sequence of the PSDU
d) Concatenating the PHR, PSDU, tail bits and pad bits
e) Encoding the bit sequence of the PSDU with a rate ½ convolutional encoder (if necessary)
f) Interleaving of the code-bit sequence (if necessary)
g) Performing data whitening of the bits after the header (if necessary)

h) Concatenation to form the PPDU
i) mapping pairs of bits to symbols for 4FSK (if necessary)

M.1 Example of 2FSK with no coding, no interleaving, no data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = FALSE
phyFSKFECScheme=0
phyFSKScramblePSDU=FALSE
phyMRFSKSFD = 0

M.1.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110

M.1.2 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening is not used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table M.2

Table M.2 – PHR for MR-FSK

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	0	0 0 0 0 0 0 0 0 1 1 1

M.1.3 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as
0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 0000 0000 0000 0111 0100 0000 0000 0000
0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

M.2 Example of 2FSK with no coding, no interleaving, no data whitening, and phyMRFSKSFD=1

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = FALSE
phyFSKFECScheme=0
phyFSKScramblePSDU=FALSE
phyMRFSKSFD = 1

M.2.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0111 1010 0000 1110

M.2.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.2 and is
0000 0000 0000 0111

M.2.3 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as
0101 0101 0101 0101 0101 0101 0101 0101 0111 1010 0000 1110 0000 0000 0000 0111 0100 0000 0000 0000
0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

M.3 Example of 2FSK with no coding, no interleaving, data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = FALSE
phyFSKFECScheme=0
phyFSKScramblePSDU=TRUE
phyMRFSKSFD = 0

M.3.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110

M.3.2 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening is used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table M.3

Table M.3– PHR for MR-FSK

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	1	0 0 0 0 0 0 0 0 1 1 1

M.3.3 Applying data whitening to the PSDU

The bit sequence of the example PSDU is
0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

Data whitening is applied as in 16.1.3. The bit sequence for the PSDU after data whitening is given as
0100 1111 0111 0000 1110 0101 0011 0010 0110 1010 0110 0010 0110 0000

M.3.4 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as

0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 0000 1000 0000 0111 0100 1111 0111 0000
1110 0101 0011 0010 0110 1010 0110 0010 0110 0000

M.4 Example of 4FSK with no coding, no interleaving, no data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:

phyFSKFECEnabled = FALSE
phyFSKFECScheme=0
phyFSKScramblePSDU=FALSE
phyMRFSKSFD = 0

M.4.1 Generation of the SHR

The preamble consists of phyFSKPreambleLength (which is 4 in these examples) multiples of the 16-bit sequence 0111 0111 0111 0111

4FSK symbols are mapped as in Table 122 by mapping each pair of bits to a single 4FSK symbol. In these examples for 4FSK the pairs of bits will be represented by a number from 0 to 3 with 0 representing "00", 1 representing "01", 2 representing "10", and 3 representing "11."

The preamble using this notation in symbols is
1313 1313 1313 1313 1313 1313 1313 1313

The SFD bit sequence is
1101 0111 0101 0101 0111 0101 1111 1101

which is represented in symbols as
3113 1111 1311 3331

The symbol sequence of the SHR is given as
1313 1313 1313 1313 1313 1313 1313 1313 3113 1111 1311 3331

M.4.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.2 and is
0000 0000 0000 0111

Mapping to symbols, the PHR is
0000 0013

M.4.3 Generation of the PSDU

The bit sequence of the PSDU is
0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

Mapping to symbols, this becomes
1000 0000 1112 1131 0221 3322 0220

M.4.4 Concatenating the SHR with the PHR and PSDU

The symbol sequence for the PPDU is given as
1313 1313 1313 1313 1313 1313 1313 1313 3113 1111 1311 3331 0000 0013 1000 0000 1112 1131 0221 3322 0220

M.5 Example of 4FSK with no coding, no interleaving, no data whitening, and phyMRFSKSFD=1

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = FALSE
phyFSKFECScheme=0
phyFSKScramblePSDU=FALSE
phyMRFSKSFD = 1

M.5.1 Generation of the SHR

The preamble consists of phyFSKPreambleLength (which is 4 in these examples) multiples of the 16-bit sequence
0111 0111 0111 0111

4FSK symbols are mapped as in Table 122 by mapping each pair of bits to a single 4FSK symbol. In these examples for 4FSK the pairs of bits will be represented by a number from 0 to 3 with 0 representing "00", 1 representing "01", 2 representing "10", and 3 representing "11."

The preamble using this notation in symbols is
1313 1313 1313 1313 1313 1313 1313 1313

The SFD bit sequence is
0111 1111 1101 1101 0101 0101 1111 1101

which is represented in symbols as
1333 3131 1111 3331

The symbol sequence of the SHR is given as
1313 1313 1313 1313 1313 1313 1313 1313 1333 3131 1111 3331

M.5.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.2 and is
0000 0000 0000 0111

Mapping to symbols, the PHR is
0000 0013

M.5.3 Generation of the PSDU

The bit sequence of the PSDU is
0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

Mapping to symbols, this becomes
1000 0000 1112 1131 0221 3322 0220

M.5.4 Concatenating the SHR with the PHR and PSDU

The symbol sequence for the PPDU is given as
1313 1313 1313 1313 1313 1313 1313 1313 1333 3131 1111 3331 0000 0013 1000 0000 1112 1131 0221 3322 0220

M.6 Example of 4FSK with no coding, no interleaving, data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = FALSE
phyFSKFECScheme=0
phyFSKScramblePSDU=TRUE
phyMRFSKSFD = 0

M.6.1 Generation of the SHR

The symbol sequence of the SHR is given as

1313 1313 1313 1313 1313 1313 1313 1313 3113 1111 1311 3331

M.6.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.3 and is
0000 1000 0000 0111

Mapping to symbols, the PHR is
0020 0013

M.6.3 Generation of the PSDU

The bit sequence of the PSDU is
0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

Data whitening is applied as in 16.1.3. The bit sequence for the PSDU after data whitening is given as
0100 1111 0111 0000 1110 0101 0011 0010 0110 1010 0110 0010 0110 0000

Mapping to symbols, this becomes
1033 1300 3211 0302 1222 1202 1200

M.6.4 Concatenating the SHR with the PHR and PSDU

The symbol sequence for the PPDU is given as
1313 1313 1313 1313 1313 1313 1313 1313 3113 1111 1311 3331 0020 0013 1033 1300 3211 0302 1222 1202 1200

All of the following examples employ convolutional coding.

M.7 Example of 2FSK with NRNSC coding, interleaving, no data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = TRUE
phyFSKFECScheme=0
phyFSKScramblePSDU=FALSE
phyMRFSKSFD = 0

M.7.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.7.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.2 and is
0000 0000 0000 0111

M.7.3 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as
0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011

M.7.4 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

1111 1111 1111 1111 1111 1111 1100 0110 1000 0100 0011 1111 1111 1111 1111 1111 1100 1011 0111 1001
1111 1011 1010 1000 0100 1110 1101 0011 0110 0101 0110 0001 0000 0010 1101 0000 1111 1111 0010 1110

M.7.5 Interleaving of the bit sequence

Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as
1011 1111 0111 1111 0011 1111 1111 1111 1111 1100 1111 1101 1111 1100 1111 0010 0011 0111 1010 1010
1011 1100 1011 0111 0101 1110 0001 0011 1010 0100 0101 1101 1011 0010 1111 0000 1011 0100 0011 1100

M.7.6 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1011 1111 0111 1111 0011 1111 1111 1111
1111 1100 1111 1101 1111 1100 1111 0010 0011 0111 1010 1010 1011 1100 1011 0111 0101 1110 0001 0011
1010 0100 0101 1101 1011 0010 1111 0000 1011 0100 0011 1100

M.8 Example of 2FSK with NRNSC coding, interleaving, data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = TRUE
phyFSKFECScheme=0
phyFSKScramblePSDU=TRUE
phyMRFSKSFD = 0

M.8.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.8.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.3 and is
0000 1000 0000 0111

M.8.3 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as
0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011

M.8.4 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as
1111 1111 0010 0000 1111 1111 1100 0110 1000 0100 0011 1111 1111 1111 1111 1111 1100 1011 0111 1001
1111 1011 1010 1000 0100 1110 1101 0011 0110 0101 0110 0001 0000 0010 1101 0000 1111 1111 0010 1110

M.8.5 Interleaving of the bit sequence

Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as
1011 0011 0111 0011 0011 1011 1111 0011 1111 1100 1111 1101 1111 1100 1111 0010 0011 0111 1010 1010
1011 1100 1011 0111 0101 1110 0001 0011 1010 0100 0101 1101 1011 0010 1111 0000 1011 0100 0011 1100

M.8.6 Applying data whitening to the PSDU

Data whitening is applied as in 16.1.3. Note that data whitening is not applied to the header, and the 16-bit header becomes 32 bits after the convolutional coding. The bit sequence for the PSDU after data whitening is given as
1011 0011 0111 0011 0011 1011 1111 0011 1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010
1111 0100 0001 1001 1110 0010 1000 0100 1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001

M.8.7 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1011 0011 0111 0011 0011 1011 1111 0011
1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010 1111 0100 0001 1001 1110 0010 1000 0100
1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001

M.9 Example of 2FSK with RSC coding, no interleaving, no data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = TRUE
phyFSKFECScheme=1
phyFSKFECInterleavingRSC=FALSE
phyFSKScramblePSDU=FALSE
phyMRFSKSFD = 0

M.9.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.9.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.2 and is
0000 0000 0000 0111

M.9.3 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as
0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011

M.9.4 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as
0000 0000 0000 0000 0000 0000 0011 0111 0001 0010 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100
0011 1001 0111 1011 0010 0110 0100 0001 1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101

M.9.5 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 0000 0000 0000 0000 0000 0000 0011 0111
0001 0010 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100 0011 1001 0111 1011 0010 0110 0100 0001
1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101

M.10 Example of 2FSK with RSC coding, no interleaving, data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = TRUE
phyFSKFECScheme=1
phyFSKFECInterleavingRSC=FALSE
phyFSKScramblePSDU=TRUE
phyMRFSKSFD = 0

M.10.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.10.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.3 and is
0000 1000 0000 0111

M.10.3 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as
0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011

M.10.4 Encoding of the bit sequence and data whitening

Convolutional coding is performed as described in 16.1.2.4 followed by data whitening as described in 16.1.3. The bit sequence after convolutional coding and data whitening is given as
0000 0000 1110 1000 0010 1000 0001 1111 0011 0101 0111 1010 1011 1001 0110 0101 0111 0000 0000 1100
0101 1001 1111 1101 1011 0010 1111 1110 1110 1101 1111 0001 0111 1101 0001 1110 1001 0000 1011 0000

M.10.5 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 0000 0000 1110 1000 0010 1000 0001 1111
0011 0101 0111 1010 1011 1001 0110 0101 0111 0000 0000 1100 0101 1001 1111 1101 1011 0010 1111 1110
1110 1101 1111 0001 0111 1101 0001 1110 1001 0000 1011 0000

M.11 Example of 2FSK with RSC coding, interleaving, no data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = TRUE
phyFSKFECScheme=1
phyFSKFECInterleavingRSC=TRUE
phyFSKScramblePSDU=FALSE
phyMRFSKSFD = 0

M.11.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.11.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.2 and is
0000 0000 0000 0111

M.11.3 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as
0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011

M.11.4 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as
0000 0000 0000 0000 0000 0000 0011 0111 0001 0010 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100

0011 1001 0111 1011 0010 0110 0100 0001 1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101

M.11.5 Interleaving of the bit sequence

Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as
1100 0000 0100 0000 1100 0000 0000 0000 1010 1010 0000 0000 1010 1001 0000 0000 1101 0011 1010 1110
1111 1101 0100 1000 0001 0110 0111 0001 0011 0010 1111 0100 0100 1010 0100 0001 1011 1000 1111 1110

M.11.6 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1100 0000 0100 0000 1100 0000 0000 0000
1010 1010 0000 0000 1010 1001 0000 0000 1101 0011 1010 1110 1111 1101 0100 1000 0001 0110 0111 0001
0011 0010 1111 0100 0100 1010 0100 0001 1011 1000 1111 1110

M.12 Example of 2FSK with RSC coding, interleaving, data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = TRUE
phyFSKFECScheme=1
phyFSKFECInterleavingRSC=TRUE
phyFSKScramblePSDU=TRUE
phyMRFSKSFD = 0

M.12.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.12.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.3 and is
0000 1000 0000 0111

M.12.3 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as
0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011

M.12.4 Encoding of the bit sequence and data whitening

Convolutional coding is performed as described in 16.1.2.4 followed by data whitening as described in 16.1.3. The bit sequence after convolutional coding and data whitening is given as
1100 0000 1110 1000 0110 1000 0000 1100 1010 0101 1101 1010 1011 0000 0110 1111 1001 0000 1001 1100
0001 1111 1110 0110 1010 1010 0100 1100 1010 0000 1110 1001 1001 1001 1001 1111 0001 0010 1001 1011

M.12.5 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1100 0000 1110 1000 0110 1000 0000 1100
1010 0101 1101 1010 1011 0000 0110 1111 1001 0000 1001 1100 0001 1111 1110 0110 1010 1010 0100 1100
1010 0000 1110 1001 1001 1001 1001 1111 0001 0010 1001 1011

M.13 Example of 4FSK with NRNSC coding, interleaving, no data whitening, and

phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = TRUE
phyFSKFECScheme=0
phyFSKScramblePSDU=FALSE
phyMRFSKSFD = 0

M.13.1 Generation of the SHR

The preamble consists of phyFSKPreambleLength (which is 4 in these examples) multiples of the 16-bit sequence
0111 0111 0111 0111

4FSK symbols are mapped as in Table 122 by mapping each pair of bits to a single 4FSK symbol. In these examples for 4FSK the pairs of bits will be represented by a number from 0 to 3 with 0 representing "00", 1 representing "01", 2 representing "10", and 3 representing "11."

The preamble using this notation in symbols is
1313 1313 1313 1313 1313 1313 1313 1313

The SFD bit sequence is
0111 1101 1111 1111 0111 0101 1111 1101

which is represented in symbols as
1331 3333 1311 3331

The symbol sequence of the SHR is given as
1313 1313 1313 1313 1313 1313 1313 1313 1331 3333 1311 3331

M.13.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.2 and is
0000 0000 0000 0111

M.13.3 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as
0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011

M.13.4 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as
1111 1111 1111 1111 1111 1111 1100 0110 1000 0100 0011 1111 1111 1111 1111 1111 1100 1011 0111 1001
1111 1011 1010 1000 0100 1110 1101 0011 0110 0101 0110 0001 0000 0010 1101 0000 1111 1111 0010 1110

M.13.5 Interleaving of the bit sequence

Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as
1011 1111 0111 1111 0011 1111 1111 1111 1111 1100 1111 1101 1111 1100 1111 0010 0011 0111 1010 1010
1011 1100 1011 0111 0101 1110 0001 0011 1010 0100 0101 1101 1011 0010 1111 0000 1011 0100 0011 1100

Mapped to symbols this becomes
2333 1333 0333 3333 3330 3331 3330 3302 0313 2222 2330 2313 1132 0103 2210 1131 2302 3300 2310 0330

M.13.6 Concatenating the SHR with the PHR and PSDU

The symbol sequence for the PPDU is given as
1313 1313 1313 1313 1313 1313 1313 1313 1331 3333 1311 3331 2333 1333 0333 3333 3330 3331 3330 3302 0313 2222 2330 2313 1132 0103 2210 1131 2302 3300 2310 0330

M.14 Example of 4FSK with NRNSC coding, interleaving, data whitening, and phyMRFSKSFD=0

For this example, selected PIB attributes are set as follows:
phyFSKFECEnabled = TRUE
phyFSKFECScheme=0
phyFSKScramblePSDU=TRUE
phyMRFSKSFD = 0

M.14.1 Generation of the SHR

The preamble consists of phyFSKPreambleLength (which is 4 in these examples) multiples of the 16-bit sequence 0111 0111 0111 0111

4FSK symbols are mapped as in Table 122 by mapping each pair of bits to a single 4FSK symbol. In these examples for 4FSK the pairs of bits will be represented by a number from 0 to 3 with 0 representing "00", 1 representing "01", 2 representing "10", and 3 representing "11."

The preamble using this notation in symbols is
1313 1313 1313 1313 1313 1313 1313 1313

The SFD bit sequence is
0111 1101 1111 1111 0111 0101 1111 1101

which is represented in symbols as
1331 3333 1311 3331

The symbol sequence of the SHR is given as
1313 1313 1313 1313 1313 1313 1313 1313 1331 3333 1311 3331

M.14.2 Generation of the PHR

The bit sequence of the PHR is generated as in Table M.3 and is
0000 1000 0000 0111

M.14.3 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as
0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011

M.14.4 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as
1111 1111 0010 0000 1111 1111 1100 0110 1000 0100 0011 1111 1111 1111 1111 1111 1100 1011 0111 1001 1111 1011 1010 1000 0100 1110 1101 0011 0110 0101 0110 0001 0000 0010 1101 0000 1111 1111 0010 1110

M.14.5 Interleaving of the bit sequence

Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as
1011 0011 0111 0011 0011 1011 1111 0011 1111 1100 1111 1101 1111 1100 1111 0010 0011 0111 1010 1010

1011 1100 1011 0111 0101 1110 0001 0011 1010 0100 0101 1101 1011 0010 1111 0000 1011 0100 0011 1100

M.14.6 Applying data whitening to the PSDU

Data whitening is applied as in 16.1.3. Note that data whitening is not applied to the header, and the 16-bit header becomes 32 bits after the convolutional coding. The bit sequence for the PSDU after data whitening is given as
1011 0011 0111 0011 0011 1011 1111 0011 1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010
1111 0100 0001 1001 1110 0010 1000 0100 1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001

Mapped to symbols this becomes
2303 1303 0323 3303 3303 2031 1033 2131 1310 0302 3310 0121 3202 2010 2130 1000 1201 0210 0110 1221

M.14.7 Concatenating the SHR with the PHR and PSDU

The symbol sequence for the PPDU is given as
1313 1313 1313 1313 1313 1313 1313 1313 1331 3333 1311 3331 2303 1303 0323 3303 3303 2031 1033 2131
1310 0302 3310 0121 3202 2010 2130 1000 1201 0210 0110 1221