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3**IEEE P802.15**
Wireless Personal Area Networks

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Re:	Comment Resolution for TG4g Sponsor Ballot
Abstract	This document presents examples of the processing to generate MR-FSK packets.
Purpose	Proposed resolution for Comment ID 36 (CID 261 in initial sponsor ballot)
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Release	The contributor acknowledges and accepts that this contribution becomes the property of IEEE and may be made publicly available by P802.15.

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Proposed resolution to CID 36 (CID 261 of the initial sponsor ballot): Revised. Create Annex M as shown below.

Annex M

(informative)

Examples of encoding a packet for the MR-FSK PHY

M.1 Introduction

The purpose of this annex is to show examples of encoding a packet for the MR-FSK PHY, as described in 16.1, for a variety of use-case scenarios. The use-case scenarios are given in Table 1.

Table 1: Scenarios for MR-FSK

Scenario name	Modulation	Data Whitening	FEC	Interleaving	Mode-switch	Sub-clause
Baseline	Filtered 2FSK	Disabled	Disabled	Disabled	Disabled	M.2
Whitened	Filtered 2FSK	Enabled	Disabled	Disabled	Disabled	M.3
NRNSC	Filtered 2FSK	Disabled	Enabled, NRNSC	Enabled	Disabled	M.4
Whitened and NRNSC	Filtered 2FSK	Enabled	Enabled, NRNSC	Enabled	Disabled	M.5
RSC	Filtered 2FSK	Disabled	Enabled, RSC	Disabled	Disabled	M.6
RSC and interleaved	Filtered 2FSK	Disabled	Enabled, RSC	Enabled	Disabled	M.7
Whitened and RSC	Filtered 2FSK	Enabled	Enabled, RSC	Disabled	Disabled	M.8
Whitened and RSC and interleaved	Filtered 2FSK	Enabled	Enabled, RSC	Enabled	Disabled	M.9
4FSK	Filtered 4FSK	Disabled	Disabled	Disabled	Disabled	M.10
4FSK, whitened and RSC and interleaved	Filtered 4FSK	Enabled	Enabled, RSC	Enabled	Disabled	M.11
Mode switch	Filtered 2FSK -> Filtered 4FSK	Disabled	Disabled	Disabled	Enabled	M.12

In all examples the message encoded is a PSDU of 7 octets shown below. The message constitutes an acknowledgment frame with a 3-octet MHR and a 4-octet FCS, as defined in 5.2.1.9. The bit sequence of the example PSDU is: 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

The encoding illustration goes through the following stages:

- a) Generating the bit sequence of the SHR
- b) Generating the bit sequence of the PHR
- c) Concatenating the PHR, PSDU, and when FEC is enabled, tail bits and pad bits
- d) Encoding of the concatenated bit sequence with the specified FEC code when FEC is enabled
- e) Interleaving of the code-bit sequence when interleaving is enabled (requires FEC also enabled)
- f) Data whitening of the PSDU when data whitening is enabled
- g) Concatenation to form the PPDU

1 h) In the case of the mode switch example, concatenation of the mode switch PPDU and the PPDU of the new mode.
 2
 3 For each scenario, the settings of the PIB attributes are also shown.

4 M.2 Baseline Scenario

5 M.2.1 Settings

6
 7 For this example, selected PIB attributes are set as follows:

8 phyFSKPreambleLength=4
 9 phyMRFSKSFD = 0
 10 phyFSKFECEnabled = FALSE
 11 phyFSKFECScheme=N/A
 12 phyFSKScramblePSDU=FALSE
 13

14 M.2.2 Generation of the SHR

15 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
 16 0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110
 17

18 M.2.3 Generation of the PHR

19 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type
 20 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening
 21 is not used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the
 22 PSDU length of the packet. The complete PHR field is shown in Table 2
 23
 24
 25

Table 2: PHR for Baseline Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R ₁ -R ₀	FCS	DW	L ₁₀ -L ₀
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	0	00000000111

28 M.2.4 Concatenating the SHR with the PHR and PSDU

29
 30 The bit sequence for the PPDU is given as:

31
 32 0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 0000 0000 0000 0111 0100 0000 0000 0000
 33 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000
 34

35 M.3 Whitened Scenario

36 M.3.1 Settings

37
 38 For this example, selected PIB attributes are set as follows:

39 phyFSKPreambleLength=4
 40 phyMRFSKSFD = 0

1 phyFSKFECEnabled = FALSE
 2 phyFSKFECScheme=N/A
 3 phyFSKScramblePSDU=TRUE
 4

5 M.3.2 Generation of the SHR

6 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
 7 0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110
 8

9 M.3.3 Generation of the PHR

10 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type
 11 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening
 12 is used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the PSDU
 13 length of the packet. The complete PHR field is shown in Table 3
 14
 15

Table 3: PHR for Whitened Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R ₁ -R ₀	FCS	DW	L ₁₀ -L ₀
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	1	00000000111

16
 17 **M.3.4 Bit sequence after data whitening of the PSDU and concatenation with PHR**
 18 Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence of the PHR and PSDU after data
 19 whitening is given as:
 20

21 0000 1000 0000 0111 0100 1111 0111 0000 1110 0101 0011 0010 0110 1010 0110 0010 0110 0000
 22

23 M.3.5 Concatenating the SHR with the PHR and PSDU

24
 25 The bit sequence for the PPDU is given as:
 26

27 0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 0000 1000 0000 0111 0100 1111 0111 0000
 28 1110 0101 0011 0010 0110 1010 0110 0010 0110 0000
 29

30 M.4 NRNSC Scenario

31
 32 <This example is per what is captured in document 717 rev1, with adjustments on text formatting for consistency
 33 with the second example included here. Make adjustments per the draft changes from d5 to d6, e.g. remove line
 34 containing the attribute phyFSKFECInterleaving .->
 35

36 M.5 Whitened and NRNSC Scenario

37 M.5.1 Settings

38 For this example, selected PIB attributes are set as follows:
 39 phyFSKPreLength=4
 40 phyMRFSKSFD = 0

1 phyFSKFECEnabled = TRUE
 2 phyFSKFECScheme=0
 3 phyFSKScramblePSDU=TRUE
 4

5 M.5.2 Generation of the SHR

6 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
 7 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110
 8

9 M.5.3 Generation of the PHR

10 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type
 11 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening
 12 is used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the PSDU
 13 length of the packet. The complete PHR field is shown in Table 4
 14
 15

Table 4: PHR for Whitened and NRNSC Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R ₁ -R ₀	FCS	DW	L ₁₀ -L ₀
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	1	00000000111

16
 17

18 M.5.4 Concatenating the PHR, PSDU, tail bits, and pad bits

19 Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation
 20 the bit sequence is given as
 21

22 0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011
 23

24 M.5.5 Encoding of the bit sequence

25 Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as
 26

27 1111 1111 0010 0000 1111 1111 1100 0110 1000 0100 0011 1111 1111 1111 1111 1111 1100 1011 0111 1001
 28 1111 1011 1010 1000 0100 1110 1101 0011 0110 0101 0110 0001 0000 0010 1101 0000 1111 1111 0010 1110
 29
 30

31 M.5.6 Interleaving of the bit sequence

32 Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as
 33

34 1011 0011 0111 0011 0011 1011 1111 0011 1111 1100 1111 1101 1111 1100 1111 0010 0011 0111 1010 1010
 35 1011 1100 1011 0111 0101 1110 0001 0011 1010 0100 0101 1101 1011 0010 1111 0000 1011 0100 0011 1100
 36

37 M.5.7 Bit sequence after data whitening of the PSDU

38 Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as
 39

40 1011 0011 0111 0011 0011 1011 1111 0011 1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010
 41 1111 0100 0001 1001 1110 0010 1000 0100 1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001
 42
 43

44 M.5.8 Concatenating the SHR with the PHR and PSDU

45 The bit sequence for the PPDU is given as
 46

1 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1011 0011 0111 0011 0011 1011 1111 0011
 2 1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010 1111 0100 0001 1001 1110 0010 1000 0100
 3 1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001
 4

5 M.6 RSC Scenario

7 M.6.1 Settings

8 For this example, selected PIB attributes are set as follows:
 9 phyFSKPreambleLength=4
 10 phyMRFSKSFD = 0
 11 phyFSKFECEnabled = TRUE
 12 phyFSKFECScheme=1
 13 phyFSKScramblePSDU=FALSE
 14 phyFSKFECInterleavingRSC = FALSE

15 M.6.2 Generation of the SHR

16 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
 17 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

18 M.6.3 Generation of the PHR

19 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type
 20 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening
 21 is not used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the
 22 PSDU length of the packet. The complete PHR field is shown in Table 5
 23
 24
 25

Table 5: PHR for RSC Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R ₁ -R ₀	FCS	DW	L ₁₀ -L ₀
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	0	00000000111

26 M.6.4 Concatenating the PHR, PSDU, tail bits, and pad bits

27 Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation
 28 the bit sequence is given as
 29

30 0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 1100 1011

31 M.6.5 Encoding of the bit sequence

32 Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as
 33

34 0000 0000 0000 0000 0000 0000 0011 0111 0001 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100
 35 0011 1001 0111 1011 0010 0110 0100 0001 1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101

36 M.6.6 Concatenating the SHR with the PHR and PSDU

37 The bit sequence for the PPDU is given as:
 38

1
 2 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 0000 0000 0000 0000 0000 0011 0111
 3 0001 0010 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100 0011 1001 0111 1011 0010 0110 0100 0001
 4 1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101
 5

6 M.7 RSC and Interleaved Scenario

7 M.7.1 Settings

8 For this example, selected PIB attributes are set as follows:
 9 phyFSKpreambleLength=4
 10 phyMRFSKSFD = 0
 11 phyFSKFECEnabled = TRUE
 12 phyFSKFECscheme=1
 13 phyFSKScramblePSDU=FALSE
 14 phyFSKFECInterleavingRSC = TRUE
 15

16 M.7.2 Generation of the SHR

17 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
 18 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

19 M.7.3 Generation of the PHR

20 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type
 21 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening
 22 is not used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the
 23 PSDU length of the packet. The complete PHR field is shown in Table 6
 24
 25
 26

Table 6: PHR for RSC and Interleaved Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R ₁ -R ₀	FCS	DW	L ₁₀ -L ₀
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	0	00000000111

27 M.7.4 Concatenating the PHR, PSDU, tail bits, and pad bits

28 Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation
 29 the bit sequence is given as
 30

31 0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 1100 1011

32 M.7.5 Encoding of the bit sequence

33 Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as
 34

35 0000 0000 0000 0000 0000 0000 0011 0111 0001 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100
 36 0011 1001 0111 1011 0010 0110 0100 0001 1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101

37 M.7.6 Interleaving of the bit sequence

38 Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as

1
 2 1100 0000 0100 0000 1100 0000 0000 0000 1010 1010 0000 0000 1010 1001 0000 0000 1101 0011 1010 1110
 3 1111 1101 0100 1000 0001 0110 0111 0001 0011 0010 1111 0100 0100 1010 0100 0001 1011 1000 1111 1110

4 **M.7.7 Concatenating the SHR with the PHR and PSDU**

5
 6 The bit sequence for the PPDU is given as:

7
 8
 9 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1100 0000 0100 0000 1100 0000 0000 0000
 10 1010 1010 0000 0000 1010 1001 0000 0000 1101 0011 1010 1110 1111 1101 0100 1000 0001 0110 0111 0001
 11 0011 0010 1111 0100 0100 1010 0100 0001 1011 1000 1111 1110

12 **M.8 Whitened and RSC Scenario**

13 **M.8.1 Settings**

14
 15 For these examples, selected PIB attributes are set as follows:
 16 phyFSKPreableLength=4
 17 phyMRFSKSFD = 0
 18 phyFSKFECEnabled = TRUE
 19 phyFSKFECScheme=1
 20 phyFSKScramblePSDU=TRUE
 21 phyFSKFECInterleavingRSC = FALSE

22 **M.8.2 Generation of the SHR**

23 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
 24 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

25 **M.8.3 Generation of the PHR**

26 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type
 27 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening
 28 is used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the PSDU
 29 length of the packet. The complete PHR field is shown in Table 7

30
 31
 32 **Table 7: PHR for Whitened and RSC Scenario**

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R ₁ -R ₀	FCS	DW	L ₁₀ -L ₀
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	1	00000000111

33

34 **M.8.4 Concatenating the PHR, PSDU, tail bits, and pad bits**

35 Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation
 36 the bit sequence is given as

37
 38 0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0100 1011

1 M.8.5 Encoding of the bit sequence

2 Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

3
4 0000 0000 1110 1000 0010 1000 0001 1111 0011 1010 0000 1010 0000 1010 0000 1010 0011 0011 1001 0100
5 0001 0001 0101 0011 0000 1110 0110 1001 1101 0101 1110 1100 1010 1110 1100 1010 0011 0000 1110 0101

6 M.8.6 Bit sequence after data whitening of the PSDU

7
8 Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as

9
10 0000 0000 1110 1000 0010 1000 0001 1111 0011 0101 0111 1010 1011 1001 0110 0101 0111 0000 0000 1100
11 0101 1001 1111 1101 1011 0010 1111 1110 1101 1111 0001 0111 1101 0001 1110 1001 0000 1011 0000

12 M.8.7 Concatenating the SHR with the PHR and PSDU

13 The bit sequence for the PPDU is given as:

14
15 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 0000 0000 1110 1000 0010 1000 0001 1111
16 0011 0101 0111 1010 1011 1001 0110 0101 0111 0000 0000 1100 0101 1001 1111 1101 1011 0010 1111 1110
17 1110 1101 1111 0001 0111 1101 0001 1110 1001 0000 1011 0000

19 M.9 Whitened and RSC and Interleaved Scenario

20 M.9.1 Settings

21 For these examples, selected PIB attributes are set as follows:

22 phyFSKPreambleLength=4
23 phyMRFSKSFD = 0
24 phyFSKFECEnabled = TRUE
25 phyFSKFECScheme=1
26 phyFSKScramblePSDU=TRUE
27 phyFSKFECInterleavingRSC = TRUE

28 M.9.2 Generation of the SHR

29 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as

30 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

31 M.9.3 Generation of the PHR

32 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type
33 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening
34 is used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the PSDU
35 length of the packet. The complete PHR field is shown in Table 8

36
37
38 **Table 8: PHR for Whitened and RSC and Interleaved Scenario**

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R ₁ -R ₀	FCS	DW	L ₁₀ -L ₀
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	1	000000001111

1

2 M.9.4 Concatenating the PHR, PSDU, tail bits, and pad bits

3 Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation
4 the bit sequence is given as

5
6 0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0100 1011
7

8 M.9.5 Encoding of the bit sequence

9 Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

10
11 0000 0000 1110 1000 0010 1000 0001 1111 0011 1010 0000 1010 0000 1010 0000 1010 0011 0011 1001 0100
12 0001 0001 0101 0011 0000 1110 0110 1001 1101 0101 1110 1100 1010 1110 1100 1010 0011 0000 1110 0101

13 M.9.6 Interleaving of the bit sequence

14 Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as

15
16 1100 0000 1110 1000 0110 1000 0000 1100 1010 1010 1010 1010 0000 0011 0000 0000 1101 0011 0000 0100
17 0101 0111 0100 1000 0001 0110 1101 1011 1001 1000 1111 0100 0100 1010 0100 1011 1011 0010 1100 1110

18 M.9.7 Bit sequence after data whitening of the PSDU

19
20 Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as

21
22 1100 0000 1110 1000 0110 1000 0000 1100 1010 0101 1101 1010 1011 0000 0110 1111 1001 0000 1001 1100
23 0001 1111 1110 0110 1010 1010 0100 1100 1010 0000 1110 1001 1001 1001 1001 1111 0001 0010 1001 1011

24 M.9.8 Concatenating the SHR with the PHR and PSDU

25 The bit sequence for the PPDU is given as:

26
27 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1100 0000 1110 1000 0110 1000 0000 1100
28 1010 0101 1101 1010 1011 0000 0110 1111 1001 0000 1001 1100 0001 1111 1110 0110 1010 1010 0100 1100
29 1010 0000 1110 1001 1001 1001 1001 1111 0001 0010 1001 1011
30

31 M.10 4FSK Scenario**32 M.10.1 Settings**

33
34 For this example, selected PIB attributes are set as follows:

35 phyFSKPreambleLength=4
36 phyMRFSKSFD = 0
37 phyFSKFECEnabled = FALSE
38 phyFSKFECScheme=N/A
39 phyFSKScramblePSDU=FALSE
40

41 M.10.2 Generation of the SHR

1 The bit sequence of the SHR, consisting of eight preamble octets and four SFD octets, is given as

2
3 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 0111 0101 0101
4 0111 0101 1111 1101
5

6 **M.10.3 Generation of the PHR**

7 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type
8 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening
9 is not used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the
10 PSDU length of the packet. The complete PHR field is shown in Table 9

11
12 **Table 9: PHR for 4FSK Scenario**

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R ₁ -R ₀	FCS	DW	L ₁₀ -L ₀
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	0	00000000111

13 **M.10.4 Concatenating the SHR with the PHR and PSDU**

14
15 The bit sequence for the PPDU is given as:

16
17
18 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 0111 0101 0101
19 0111 0101 1111 1101 0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010
20 0010 1000
21

22 **M.11 4FSK, whitened and RSC and interleaved Scenario**

23 **M.11.1 Settings**

24
25 For this example, selected PIB attributes are set as follows:

26 phyFSKPreambleLength=4
27 phyMRFSKSFD = 0
28 phyFSKFECEnabled = TRUE
29 phyFSKFECScheme=1
30 phyFSKScramblePSDU=TRUE
31 phyFSKFECInterleavingRSC = TRUE
32
33

34 **M.11.2 Generation of the SHR**

35 The bit sequence of the SHR, consisting of eight preamble octets and four SFD octets, is given as

36
37 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 1111 1111
38 0111 0101 1111 1101
39

40 **M.11.3 Generation of the PHR**

41 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type
42 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening
43 is used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the PSDU
44 length of the packet. The complete PHR field is shown in Table 10.

Table 10: PHR for 4FSK, Whitened and RSC and Interleaved Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R ₁ -R ₀	FCS	DW	L ₁₀ -L ₀
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	1	00000000111

M.11.4 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as

```
0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0100 1011
```

M.11.5 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

```
0000 0000 1110 1000 0010 1000 0001 1111 0011 1010 0000 1010 0000 1010 0000 1010 0011 0011 1001 0100
0001 0001 0101 0011 0000 1110 0110 1001 1101 0101 1110 1100 1010 1110 1100 1010 0011 0000 1110 0101
```

M.11.6 Interleaving of the bit sequence

Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as

```
1100 0000 1110 1000 0110 1000 0000 1100 1010 1010 1010 1010 0000 0011 0000 0000 1101 0011 0000 0100
0101 0111 0100 1000 0001 0110 1101 1011 1001 1000 1111 0100 0100 1010 0100 1011 1011 0010 1100 1110
```

M.11.7 Bit sequence after data whitening of the PSDU

Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as

```
1100 0000 1110 1000 0110 1000 0000 1100 1010 0101 1101 1010 1011 0000 0110 1111 1001 0000 1001 1100
0001 1111 1110 0110 1010 1010 0100 1100 1010 0000 1110 1001 1001 1001 1001 1111 0001 0010 1001 1011
```

M.11.8 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as:

```
0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 1111 1111
0111 0101 1111 1101 1100 0000 1110 1000 0110 1000 0000 1100 1010 0101 1101 1010 1011 0000 0110 1111
1001 0000 1001 1100 0001 1111 1110 0110 1010 1010 0100 1100 1010 0000 1110 1001 1001 1001 1001 1111
0001 0010 1001 1011
```

M.12 Mode Switch Scenario

M.12.1 Settings

For this example, selected PIB attributes are set as follows:

```
phyFSKpreambleLength=4
```

1 phyMRFSKSFD = 0
 2 phyFSKFECEnabled = FALSE
 3 phyFSKFECScheme=N/A
 4 phyFSKScramblePSDU=FALSE
 5

6 In the example, mode switch is used, to switch from filtered 2FSK to filtered 4FSK. Two packets are sent in
 7 sequence, the first one is the mode switch packet, sent in the 2-FSK mode, and the second one is the packet
 8 encapsulating the message captured in M.1, sent in the 4-FSK mode.
 9

10 The ModeSwitchParameterEntry (see Figure 106) is assumed to be 0, and the elements of the corresponding
 11 ModeSwitchDescriptor (see Tables 124 and 71b) are assumed to be as follows:

- 12 - the SettlingDelay is 0
- 13 - the SecondaryFSKPreLength is 4
- 14 - the SecondaryFSKSFD is TRUE.

15
 16 The NewMode (see Figure 107) is set as follows:

- 17 - Page is 0 (channel page seven)
- 18 - ModulationScheme is 0 (filtered FSK)
- 19 - Mode = 3 (Operating mode #4 using filtered 4-FSK)

20 21 M.12.2 Generation of the Mode Switch Packet

22 23 M.12.2.1 Generation of the SHR

24 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
 25 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110
 26

27 M.12.2.2 Generation of the PHR

28 The complete PHR field is shown in Table 11.
 29
 30

Table 11: PHR for Mode Switch Scenario

Bit string index	0	1-2	3	4-10	11-14	15
Bit mapping	MS	M ₁ -M ₀	FEC	See Figure 107	B ₃ -B ₀	PC
Field name	Mode Switch	Mode Switch Param Entry	New Mode FEC	New Mode	Checksum	Parity Check
Value	1	0 0	0	0000 011	1100	1

31 32 M.12.2.3 Concatenating the SHR with the PHR to form the Mode Switch Packet

33 The bit sequence for the mode switch PPDU is given as:
 34 0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 1000 0000 0111 1001
 35
 36

37 M.12.3 Generation of the Packet in the New Mode

38 This packet is the same as in M.10
 39

40 M.12.4 Concatenating the Two Packets

41 The final bit sequence consists of the concatenation of the following two bit sequences:
 42
 43

- 44 1) the first sequence, sent with 2FSK modulation, as follows:

1
2
3
4
5
6
7
8
9

0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 1000 0000 0111 1001

2) the second sequence, sent with 4FSK modulation, as follows:

0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 0111 0101 0101
0111 0101 1111 1101 0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010
0010 1000