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**IEEE P802.15**  
**Wireless Personal Area Networks**

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Re:	Comment Resolution for TG4g Sponsor Ballot
Abstract	This document presents examples of the processing to generate MR-FSK packets.
Purpose	Proposed resolution for Comment ID 36 (CID 261 in initial sponsor ballot)
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Release	The contributor acknowledges and accepts that this contribution becomes the property of IEEE and may be made publicly available by P802.15.

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Proposed resolution to CID 36 (CID 261 of the initial sponsor ballot): Revised. Create Annex M as shown below.

## Annex M

(informative)

### Examples of encoding a packet for the MR-FSK PHY

#### M.1 Introduction

The purpose of this annex is to show examples of encoding a packet for the MR-FSK PHY, as described in 16.1, for a variety of use-case scenarios. The use-case scenarios are given in Table 1.

**Table 1: Scenarios for MR-FSK**

Scenario name	Modulation	Data Whitening	FEC	Interleaving	Mode-switch	Sub-clause
Baseline	Filtered 2FSK	Disabled	Disabled	Disabled	Disabled	M.2
Whitened	Filtered 2FSK	Enabled	Disabled	Disabled	Disabled	M.3
NRNSC	Filtered 2FSK	Disabled	Enabled, NRNSC	Enabled	Disabled	M.4
Whitened and NRNSC	Filtered 2FSK	Enabled	Enabled, NRNSC	Enabled	Disabled	M.5
RSC	Filtered 2FSK	Disabled	Enabled, RSC	Disabled	Disabled	M.6
RSC and interleaved	Filtered 2FSK	Disabled	Enabled, RSC	Enabled	Disabled	M.7
Whitened and RSC	Filtered 2FSK	Enabled	Enabled, RSC	Disabled	Disabled	M.8
Whitened and RSC and interleaved	Filtered 2FSK	Enabled	Enabled, RSC	Enabled	Disabled	M.9
4FSK	Filtered 4FSK	Disabled	Disabled	Disabled	Disabled	M.10
Mode switch	Filtered 2FSK -> Filtered 4FSK	Disabled	Disabled	Disabled	Enabled	M.11

In all examples the message encoded is a PSDU of 7 octets shown below. The message constitutes an acknowledgment frame with a 3-octet MHR and a 4-octet FCS, as defined in 5.2.1.9. The bit sequence of the example PSDU is: 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

The encoding illustration goes through the following stages:

- a) Generating the bit sequence of the SHR
- b) Generating the bit sequence of the PHR
- c) Concatenating the PHR, PSDU, and when FEC is enabled, tail bits and pad bits
- d) Encoding of the concatenated bit sequence with the specified FEC code when FEC is enabled
- e) Interleaving of the code-bit sequence when interleaving is enabled (requires FEC also enabled)
- f) Data whitening of the PSDU when data whitening is enabled
- g) Concatenation to form the PPDU
- h) In the case of the mode switch example, concatenation of the mode switch PPDU and the PPDU of the new mode.

For each scenario, the settings of the PIB attributes are also shown.

## 1 M.2 Baseline Scenario

### 2 M.2.1 Settings

3  
4 For this example, selected PIB attributes are set as follows:  
5 phyFSKPreambleLength=4  
6 phyMRFSKSFDF = 0  
7 phyFSKFECEnabled = FALSE  
8 phyFSKFECScheme=N/A  
9 phyFSKScramblePSDU=FALSE

10

### 11 M.2.2 Generation of the SHR

12 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as  
13 0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110

14

### 15 M.2.3 Generation of the PHR

16 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type  
17 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening  
18 is not used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the  
19 PSDU length of the packet. The complete PHR field is shown in Table 2

20

21

22

**Table 2: PHR for Baseline Scenario**

<b>Bit string index</b>	0	1-2	3	4	5-15
<b>Bit mapping</b>	MS	R <sub>1</sub> -R <sub>0</sub>	FCS	DW	L <sub>10</sub> -L <sub>0</sub>
<b>Field name</b>	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
<b>Value</b>	0	00	0	0	00000000111

23

24

### 25 M.2.4 Concatenating the SHR with the PHR and PSDU

26

27 The bit sequence for the PPDU is given as:

28

29 0101 0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 0000 0000 0000 0111 0100 0000 0000 0000  
30 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

31

## 32 M.3 Whitened Scenario

### 33 M.3.1 Settings

34

35 For this example, selected PIB attributes are set as follows:  
36 phyFSKPreambleLength=4  
37 phyMRFSKSFDF = 0  
38 phyFSKFECEnabled = FALSE  
39 phyFSKFECScheme=N/A  
40 phyFSKScramblePSDU=TRUE

41

### 1 M.3.2 Generation of the SHR

2 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as  
 3 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110  
 4

### 5 M.3.3 Generation of the PHR

6 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type  
 7 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening  
 8 is used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the PSDU  
 9 length of the packet. The complete PHR field is shown in Table 3

10  
 11 **Table 3: PHR for Whitened Scenario**

<b>Bit string index</b>	0	1-2	3	4	5-15
<b>Bit mapping</b>	MS	R <sub>1</sub> -R <sub>0</sub>	FCS	DW	L <sub>10</sub> -L <sub>0</sub>
<b>Field name</b>	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
<b>Value</b>	0	00	0	1	00000000111

### 12 M.3.4 Bit sequence after data whitening of the PSDU and concatenation with PHR

13 Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence of the PHR and PSDU after data  
 14 whitening is given as:

15  
 16  
 17 0000 1000 0000 0111 0100 1111 0111 0000 1110 0101 0011 0010 0110 1010 0110 0010 0110 0000  
 18

### 19 M.3.5 Concatenating the SHR with the PHR and PSDU

20  
 21 The bit sequence for the PPDU is given as:

22  
 23 0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 0000 1000 0000 0111 0100 1111 0111 0000  
 24 1110 0101 0011 0010 0110 1010 0110 0010 0110 0000  
 25

## 26 M.4 NRNSC Scenario

27  
 28 <This example is per what is captured in document 717 rev1, with adjustments on text formatting for consistency  
 29 with the second example included here. Make adjustments per the draft changes from d5 to d6, e.g. remove line  
 30 containing the attribute phyFSKFECInterleaving .>  
 31

## 32 M.5 Whitened and NRNSC Scenario

### 33 M.5.1 Settings

34 For this example, selected PIB attributes are set as follows:  
 35 phyFSKPreambleLength=4  
 36 phyMRFSKSFD = 0  
 37 phyFSKFECEnabled = TRUE  
 38 phyFSKFECScheme=0  
 39 phyFSKScramblePSDU=TRUE  
 40

### 1 M.5.2 Generation of the SHR

2 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as  
 3 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110  
 4

### 5 M.5.3 Generation of the PHR

6 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type  
 7 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening  
 8 is used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the PSDU  
 9 length of the packet. The complete PHR field is shown in Table 4  
 10  
 11

Table 4: PHR for Whitenes and NRNSC Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R <sub>1</sub> -R <sub>0</sub>	FCS	DW	L <sub>10</sub> -L <sub>0</sub>
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	1	0 0 0 0 0 0 0 0 1 1 1

### 14 M.5.4 Concatenating the PHR, PSDU, tail bits, and pad bits

15 Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation  
 16 the bit sequence is given as  
 17

18 0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011  
 19

### 20 M.5.5 Encoding of the bit sequence

21 Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as  
 22

23 1111 1111 0010 0000 1111 1111 1100 0110 1000 0100 0011 1111 1111 1111 1111 1111 1100 1011 0111 1001  
 24 1111 1011 1010 1000 0100 1110 1101 0011 0110 0101 0110 0001 0000 0010 1101 0000 1111 1111 0010 1110  
 25  
 26

### 27 M.5.6 Interleaving of the bit sequence

28 Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as  
 29

30 1011 0011 0111 0011 0011 1011 1111 0011 1111 1100 1111 1101 1111 1100 1111 0010 0011 0111 1010 1010  
 31 1011 1100 1011 0111 0101 1110 0001 0011 1010 0100 0101 1101 1011 0010 1111 0000 1011 0100 0011 1100  
 32

### 33 M.5.7 Bit sequence after data whitening of the PSDU

34 Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as  
 35

36 1011 0011 0111 0011 0011 1011 1111 0011 1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010  
 37 1111 0100 0001 1001 1110 0010 1000 0100 1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001  
 38  
 39

### 40 M.5.8 Concatenating the SHR with the PHR and PSDU

41 The bit sequence for the PPDU is given as  
 42

43 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1011 0011 0111 0011 0011 1011 1111 0011  
 44 1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010 1111 0100 0001 1001 1110 0010 1000 0100  
 45 1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001  
 46

## 1 M.6 RSC Scenario

### 3 M.6.1 Settings

4 For this example, selected PIB attributes are set as follows:

5 phyFSKPreambleLength=4  
 6 phyMRFSKSFD = 0  
 7 phyFSKFECEnabled = TRUE  
 8 phyFSKFECScheme=1  
 9 phyFSKScramblePSDU=FALSE  
 10 phyFSKFECInterleavingRSC = FALSE

### 11 M.6.2 Generation of the SHR

12 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as  
 13 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

### 14 M.6.3 Generation of the PHR

15 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type  
 16 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening  
 17 is not used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the  
 18 PSDU length of the packet. The complete PHR field is shown in Table 5  
 19  
 20  
 21

**Table 5: PHR for RSC Scenario**

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R <sub>1</sub> -R <sub>0</sub>	FCS	DW	L <sub>10</sub> -L <sub>0</sub>
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	0	00000000111

### 22 M.6.4 Concatenating the PHR, PSDU, tail bits, and pad bits

23 Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation  
 24 the bit sequence is given as  
 25

26 0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 1100 1011

### 27 M.6.5 Encoding of the bit sequence

28 Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as  
 29

30 0000 0000 0000 0000 0000 0000 0011 0111 0001 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100  
 31 0011 1001 0111 1011 0010 0110 0100 0001 1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101

### 32 M.6.6 Concatenating the SHR with the PHR and PSDU

33 The bit sequence for the PPDU is given as:  
 34  
 35

36 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 0000 0000 0000 0000 0000 0000 0011 0111  
 37 0001 0010 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100 0011 1001 0111 1011 0010 0110 0100 0001  
 38 1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101  
 39

## 1 M.7 RSC and Interleaved Scenario

### 2 M.7.1 Settings

3 For this example, selected PIB attributes are set as follows:

4 phyFSKPreambleLength=4  
 5 phyMRFSKSFDF = 0  
 6 phyFSKFECEnabled = TRUE  
 7 phyFSKFECScheme=1  
 8 phyFSKScramblePSDU=FALSE  
 9 phyFSKFECInterleavingRSC = TRUE  
 10

### 11 M.7.2 Generation of the SHR

12 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as  
 13 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

### 14 M.7.3 Generation of the PHR

15 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type  
 16 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening  
 17 is not used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the  
 18 PSDU length of the packet. The complete PHR field is shown in Table 6  
 19  
 20  
 21

**Table 6: PHR for RSC and Interleaved Scenario**

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R <sub>1</sub> -R <sub>0</sub>	FCS	DW	L <sub>10</sub> -L <sub>0</sub>
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	0	000000001111

### 22 M.7.4 Concatenating the PHR, PSDU, tail bits, and pad bits

23 Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation  
 24 the bit sequence is given as  
 25

26 0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 1100 1011

### 27 M.7.5 Encoding of the bit sequence

28 Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as  
 29

30 0000 0000 0000 0000 0000 0000 0011 0111 0001 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100  
 31 0011 1001 0111 1011 0010 0110 0100 0001 1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101

### 32 M.7.6 Interleaving of the bit sequence

33 Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as  
 34

35 1100 0000 0100 0000 1100 0000 0000 0000 1010 1010 0000 0000 1010 1001 0000 0000 1101 0011 1010 1110  
 36 1111 1101 0100 1000 0001 0110 0111 0001 0011 0010 1111 0100 0100 1010 0100 0001 1011 1000 1111 1110



## 1 M.7.7 Concatenating the SHR with the PHR and PSDU

2  
3 The bit sequence for the PPDU is given as:

4  
5  
6 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1100 0000 0100 0000 1100 0000 0000 0000  
7 1010 1010 0000 0000 1010 1001 0000 0000 1101 0011 1010 1110 1111 1101 0100 1000 0001 0110 0111 0001  
8 0011 0010 1111 0100 0100 1010 0100 0001 1011 1000 1111 1110

## 9 M.8 Whitened and RSC Scenario

### 10 M.8.1 Settings

11 For these examples, selected PIB attributes are set as follows:

12 phyFSKPreambleLength=4  
13 phyMRFSKSFD = 0  
14 phyFSKFECEnabled = TRUE  
15 phyFSKFECScheme=1  
16 phyFSKScramblePSDU=TRUE  
17 phyFSKFECInterleavingRSC = FALSE

### 19 M.8.2 Generation of the SHR

20 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as

21 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

### 22 M.8.3 Generation of the PHR

23 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type  
24 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening  
25 is used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the PSDU  
26 length of the packet. The complete PHR field is shown in Table 7

27  
28  
29 **Table 7: PHR for Whitened and RSC Scenario**

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R <sub>1</sub> -R <sub>0</sub>	FCS	DW	L <sub>10</sub> -L <sub>0</sub>
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	1	00000000111

### 31 M.8.4 Concatenating the PHR, PSDU, tail bits, and pad bits

32 Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation  
33 the bit sequence is given as

34  
35 0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0100 1011

### 36 M.8.5 Encoding of the bit sequence

37 Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

1  
 2 0000 0000 1110 1000 0010 1000 0001 1111 0011 1010 0000 1010 0000 1010 0000 1010 0011 0011 1001 0100  
 3 0001 0001 0101 0011 0000 1110 0110 1001 1101 0101 1110 1100 1010 1110 1100 1010 0011 0000 1110 0101

#### 4 **M.8.6 Bit sequence after data whitening of the PSDU**

5  
 6 Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as

7  
 8 0000 0000 1110 1000 0010 1000 0001 1111 0011 0101 0111 1010 1011 1001 0110 0101 0111 0000 0000 1100  
 9 0101 1001 1111 1101 1011 0010 1111 1110 1101 1111 0001 0111 1101 0001 1110 1001 0000 1011 0000

#### 10 **M.8.7 Concatenating the SHR with the PHR and PSDU**

11 The bit sequence for the PPDU is given as:

12  
 13 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 0000 0000 1110 1000 0010 1000 0001 1111  
 14 0011 0101 0111 1010 1011 1001 0110 0101 0111 0000 0000 1100 0101 1001 1111 1101 1011 0010 1111 1110  
 15 1110 1101 1111 0001 0111 1101 0001 1110 1001 0000 1011 0000

#### 17 **M.9 Whitened and RSC and Interleaved Scenario**

##### 18 **M.9.1 Settings**

19 For these examples, selected PIB attributes are set as follows:

20 phyFSKPreambleLength=4  
 21 phyMRFSKSFDF = 0  
 22 phyFSKFECEnabled = TRUE  
 23 phyFSKFECScheme=1  
 24 phyFSKScramblePSDU=TRUE  
 25 phyFSKFECInterleavingRSC = TRUE

##### 26 **M.9.2 Generation of the SHR**

27 The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as

28 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

##### 29 **M.9.3 Generation of the PHR**

30 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type  
 31 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening  
 32 is used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the PSDU  
 33 length of the packet. The complete PHR field is shown in Table 8

34  
 35  
 36

**Table 8: PHR for Whitened and RSC and Interleaved Scenario**

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R <sub>1</sub> -R <sub>0</sub>	FCS	DW	L <sub>10</sub> -L <sub>0</sub>
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	00	0	1	0000000111

37

### 1 **M.9.4 Concatenating the PHR, PSDU, tail bits, and pad bits**

2 Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation  
3 the bit sequence is given as

4  
5 0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0100 1011  
6

### 7 **M.9.5 Encoding of the bit sequence**

8 Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

9  
10 0000 0000 1110 1000 0010 1000 0001 1111 0011 1010 0000 1010 0000 1010 0000 1010 0011 0011 1001 0100  
11 0001 0001 0101 0011 0000 1110 0110 1001 1101 0101 1110 1100 1010 1110 1100 1010 0011 0000 1110 0101

### 12 **M.9.6 Interleaving of the bit sequence**

13 Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as

14  
15 1100 0000 1110 1000 0110 1000 0000 1100 1010 1010 1010 1010 0000 0011 0000 0000 1101 0011 0000 0100  
16 0101 0111 0100 1000 0001 0110 1101 1011 1001 1000 1111 0100 0100 1010 0100 1011 1011 0010 1100 1110

### 17 **M.9.7 Bit sequence after data whitening of the PSDU**

18  
19 Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as

20  
21 1100 0000 1110 1000 0110 1000 0000 1100 1010 0101 1101 1010 1011 0000 0110 1111 1001 0000 1001 1100  
22 0001 1111 1110 0110 1010 1010 0100 1100 1010 0000 1110 1001 1001 1001 1001 1111 0001 0010 1001 1011

### 23 **M.9.8 Concatenating the SHR with the PHR and PSDU**

24 The bit sequence for the PPDU is given as:

25  
26 0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1100 0000 1110 1000 0110 1000 0000 1100  
27 1010 0101 1101 1010 1011 0000 0110 1111 1001 0000 1001 1100 0001 1111 1110 0110 1010 1010 0100 1100  
28 1010 0000 1110 1001 1001 1001 1001 1111 0001 0010 1001 1011  
29

## 30 **M.10 4FSK Scenario**

### 31 **M.10.1 Settings**

32  
33 For this example, selected PIB attributes are set as follows:

34 phyFSKPreambleLength=4  
35 phyMRFSKSFD = 0  
36 phyFSKFECEnabled = FALSE  
37 phyFSKFECScheme=N/A  
38 phyFSKScramblePSDU=FALSE  
39

### 40 **M.10.2 Generation of the SHR**

41 The bit sequence of the SHR, consisting of eight preamble octets and four SFD octets, is given as

1 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 0111 0101 0101  
 2 0111 0101 1111 1101  
 3

### 4 M.10.3 Generation of the PHR

5 The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type  
 6 (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening  
 7 is not used), and the Frame Length field entries are set to the binary representation of “7,” corresponding to the  
 8 PSDU length of the packet. The complete PHR field is shown in Table 9  
 9

10 **Table 9: PHR for 4FSK Scenario**

<b>Bit string index</b>	0	1-2	3	4	5-15
<b>Bit mapping</b>	MS	R <sub>1</sub> -R <sub>0</sub>	FCS	DW	L <sub>10</sub> -L <sub>0</sub>
<b>Field name</b>	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
<b>Value</b>	0	00	0	0	00000000111

### 11 M.10.4 Concatenating the SHR with the PHR and PSDU

12 The bit sequence for the PPDU is given as:  
 13

14 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 0111 0101 0101  
 15 0111 0101 1111 1101 0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010  
 16 0010 1000  
 17  
 18

## 19 M.11 Mode Switch Scenario

### 20 M.11.1 Settings

21 For this example, selected PIB attributes are set as follows:  
 22

23 phyFSKPreambleLength=4  
 24 phyMRFSKSFD = 0  
 25 phyFSKFECEnabled = FALSE  
 26 phyFSKFECScheme=N/A  
 27 phyFSKFECScramblePSDU=FALSE  
 28  
 29

30 In the example, mode switch is used, to switch from filtered 2FSK to filtered 4FSK. Two packets are sent in  
 31 sequence, the first one is the mode switch packet, sent in the 2-FSK mode, and the second one is the packet  
 32 encapsulating the message captured in M.1, sent in the 4-FSK mode.  
 33

34 The ModeSwitchParameterEntry (see Figure 106) is assumed to be 0, and the elements of the corresponding  
 35 ModeSwitchDescriptor (see Tables 124 and 71b) are assumed to be as follows:

- 36 - the SettlingDelay is 0
- 37 - the SecondaryFSKPreambleLength is 4
- 38 - the SecondaryFSKSFD is TRUE.

39 The NewMode (see Figure 107) is set as follows:

- 40 - Page is 0 (channel page seven)
- 41 - ModulationScheme is 0 (filtered FSK)
- 42 - Mode = 3 (Operating mode #4 using filtered 4-FSK)

### 43 M.11.2 Generation of the Mode Switch Packet

1  
2  
3  
4  
5  
6  
7  
8  
9

### M.11.2.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as  
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

### M.11.2.2 Generation of the PHR

The complete PHR field is shown in Table 10

**Table 10: PHR for Mode Switch Scenario**

Bit string index	0	1-2	3	4-10	11-14	15
Bit mapping	MS	$M_1-M_0$	FEC	See Figure 107	$B_3-B_0$	PC
Field name	Mode Switch	Mode Switch Param Entry	New Mode FEC	New Mode	Checksum	Parity Check
Value	1	0 0	0	0000 011	1100	1

10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26

### M.11.2.3 Concatenating the SHR with the PHR to form the Mode Switch Packet

The bit sequence for the mode switch PPDU is given as:

0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 1000 0000 0111 1001

### M.11.3 Generation of the Packet in the New Mode

This packet is the same as in M.10

### M.11.4 Concatenating the Two Packets

The bit sequence is given as:

0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 1000 0000 0111 1001 0111 0111 0111 0111  
0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 0111 0101 0101 0111 0101 1111 1101  
0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000