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Re:	Comment Resolution for TG4g Sponsor Ballot
Abstract	This document presents examples of the processing to generate MR-FSK packets.
Purpose	Proposed resolution for Comment ID 36 (CID 261 in initial sponsor ballot)
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Release	The contributor acknowledges and accepts that this contribution becomes the property of IEEE and may be made publicly available by P802.15.

List of Tables

Proposed resolution to CID 36 (CID 261 of the initial sponsor ballot): Revised. Create Annex M as shown below.

Annex M

(informative)

Examples of encoding a packet for the MR-FSK PHY

M.1 Introduction

The purpose of this annex is to show examples of encoding a packet for the MR-FSK PHY, as described in 16.1, for a variety of use-case scenarios. The use-case scenarios are given in Table 1.

Table 1: Scenarios for MR-FSK

Scenario name	Modulation	Data Whitening	FEC	Interleaving	Mode-switch	Sub-clause
Baseline	Filtered 2FSK	Disabled	Disabled	Disabled	Disabled	M.2
Whitened	Filtered 2FSK	Enabled	Disabled	Disabled	Disabled	M.3
NRNSC	Filtered 2FSK	Disabled	Enabled, NRNSC	Enabled	Disabled	M.4
Whitened and NRNSC	Filtered 2FSK	Enabled	Enabled, NRNSC	Enabled	Disabled	M.5
RSC	Filtered 2FSK	Disabled	Enabled, RSC	Disabled	Disabled	M.6
RSC and interleaved	Filtered 2FSK	Disabled	Enabled, RSC	Enabled	Disabled	M.7
Whitened and RSC	Filtered 2FSK	Enabled	Enabled, RSC	Disabled	Disabled	M.8
Whitened and RSC and interleaved	Filtered 2FSK	Enabled	Enabled, RSC	Enabled	Disabled	M.9
4FSK	Filtered 4FSK	Disabled	Disabled	Disabled	Disabled	M.10
Mode switch	Filtered 2FSK -> Filtered 4FSK	Disabled	Disabled	Disabled	Enabled	M.11

In all examples the message encoded is a PSDU of 7 octets shown below. The message constitutes an acknowledgment frame with a 3-octet MHR and a 4-octet FCS, as defined in 5.2.1.9. The bit sequence of the example PSDU is: 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

The encoding illustration goes through the following stages:

a) Generating the bit sequence of the SHR
b) Generating the bit sequence of the PHR
c) Concatenating the PHR, PSDU, and when FEC is enabled, tail bits and pad bits
d) Encoding of the concatenated bit sequence with the specified FEC code when FEC is enabled
e) Interleaving of the code-bit sequence when interleaving is enabled (requires FEC also enabled)
f) Data whitening of the PSDU when data whitening is enabled
g) Concatenation to form the PPDU
h) In the case of the mode switch example, concatenation of the mode switch PPDU and the PPDU of the new mode.

For each scenario, the settings of the PIB attributes are also shown.

M.2 Baseline Scenario

M.2.1 Settings

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = FALSE
phyFSKFECScheme=N/A
phyFSKScramblePSDU=FALSE

M.2.2 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110

M.2.3 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening is not used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table 2

Table 2: PHR for Baseline Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	0	0 0 0 0 0 0 0 0 0 1 1 1

M.2.4 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as:

0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 0000 0000 0000 0111 0100 0000 0000 0000
0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

M.3 Whitened Scenario

M.3.1 Settings

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = FALSE
phyFSKFECScheme=N/A
phyFSKScramblePSDU=TRUE

M.3.2 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110

M.3.3 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening is used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table 3

Table 3: PHR for Whitened Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	1	0 0 0 0 0 0 0 0 0 1 1 1

M.3.4 Bit sequence after data whitening of the PSDU and concatenation with PHR

Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence of the PHR and PSDU after data whitening is given as:

0000 1000 0000 0111 0100 1111 0111 0000 1110 0101 0011 0010 0110 1010 0110 0010 0110 0000

M.3.5 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as:

0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 0000 1000 0000 0111 0100 1111 0111 0000
1110 0101 0011 0010 0110 1010 0110 0010 0110 0000

M.4 NRNSC Scenario

<This example is per what is captured in document 717 rev1, with adjustments on text formatting for consistency with the second example included here. Make adjustments per the draft changes from d5 to d6, e.g. remove line containing the attribute phyFSKFECInterleaving .>

M.5 Whitened and NRNSC Scenario

M.5.1 Settings

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = TRUE
phyFSKFECScheme=0
phyFSKScramblePSDU=TRUE

M.5.2 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.5.3 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening is used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table 4

Table 4: PHR for Whitened and NRNSC Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	1	0 0 0 0 0 0 0 0 1 1 1

M.5.4 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as

0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011

M.5.5 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

1111 1111 0010 0000 1111 1111 1100 0110 1000 0100 0011 1111 1111 1111 1111 1111 1100 1011 0111 1001
1111 1011 1010 1000 0100 1110 1101 0011 0110 0101 0110 0001 0000 0010 1101 0000 1111 1111 0010 1110

M.5.6 Interleaving of the bit sequence

Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as

1011 0011 0111 0011 0011 1011 1111 0011 1111 1100 1111 1101 1111 1100 1111 0010 0011 0111 1010 1010
1011 1100 1011 0111 0101 1110 0001 0011 1010 0100 0101 1101 1011 0010 1111 0000 1011 0100 0011 1100

M.5.7 Bit sequence after data whitening of the PSDU

Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as

1011 0011 0111 0011 0011 1011 1111 0011 1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010
1111 0100 0001 1001 1110 0010 1000 0100 1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001

M.5.8 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as

0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1011 0011 0111 0011 0011 1011 1111 0011
1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010 1111 0100 0001 1001 1110 0010 1000 0100
1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001

M.6 RSC Scenario

M.6.1 Settings

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = TRUE
phyFSKFECScheme=1
phyFSKScramblePSDU=FALSE
phyFSKFECInterleavingRSC = FALSE

M.6.2 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.6.3 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening is not used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table 5

Table 5: PHR for RSC Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	0	0 0 0 0 0 0 0 0 1 1 1

M.6.4 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as

0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 1100 1011

M.6.5 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

0000 0000 0000 0000 0000 0000 0011 0111 0001 0010 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100
0011 1001 0111 1011 0010 0110 0100 0001 1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101

M.6.6 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as:

0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 0000 0000 0000 0000 0000 0000 0011 0111
0001 0010 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100 0011 1001 0111 1011 0010 0110 0100 0001
1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101

M.7 RSC and Interleaved Scenario

M.7.1 Settings

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = TRUE
phyFSKFECScheme=1
phyFSKScramblePSDU=FALSE
phyFSKFECInterleavingRSC = TRUE

M.7.2 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.7.3 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening is not used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table 6

Table 6: PHR for RSC and Interleaved Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	0	0 0 0 0 0 0 0 0 1 1 1

M.7.4 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as

0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 1100 1011

M.7.5 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

0000 0000 0000 0000 0000 0000 0011 0111 0001 0010 0010 0010 0010 0010 0010 0010 0001 1011 1011 1100
0011 1001 0111 1011 0010 0110 0100 0001 1111 1101 1100 0100 1000 0110 1110 0010 1111 0000 1110 0101

M.7.6 Interleaving of the bit sequence

Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as

1100 0000 0100 0000 1100 0000 0000 0000 1010 1010 0000 0000 1010 1001 0000 0000 1101 0011 1010 1110
1111 1101 0100 1000 0001 0110 0111 0001 0011 0010 1111 0100 0100 1010 0100 0001 1011 1000 1111 1110

M.7.7 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as:

0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1100 0000 0100 0000 1100 0000 0000 0000
1010 1010 0000 0000 1010 1001 0000 0000 1101 0011 1010 1110 1111 1101 0100 1000 0001 0110 0111 0001
0011 0010 1111 0100 0100 1010 0100 0001 1011 1000 1111 1110

M.8 Whitened and RSC Scenario

M.8.1 Settings

For these examples, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = TRUE
phyFSKFECScheme=1
phyFSKScramblePSDU=TRUE
phyFSKFECInterleavingRSC = FALSE

M.8.2 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.8.3 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening is used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table 7

Table 7: PHR for Whitened and RSC Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	1	0 0 0 0 0 0 0 0 1 1 1

M.8.4 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as

0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0100 1011

M.8.5 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

0000 0000 1110 1000 0010 1000 0001 1111 0011 1010 0000 1010 0000 1010 0000 1010 0011 0011 1001 0100
0001 0001 0101 0011 0000 1110 0110 1001 1101 0101 1110 1100 1010 1110 1100 1010 0011 0000 1110 0101

M.8.6 Bit sequence after data whitening of the PSDU

Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as

0000 0000 1110 1000 0010 1000 0001 1111 0011 0101 0111 1010 1011 1001 0110 0101 0111 0000 0000 1100
0101 1001 1111 1101 1011 0010 1111 1110 1110 1101 1111 0001 0111 1101 0001 1110 1001 0000 1011 0000

M.8.7 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as:

0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 0000 0000 1110 1000 0010 1000 0001 1111
0011 0101 0111 1010 1011 1001 0110 0101 0111 0000 0000 1100 0101 1001 1111 1101 1011 0010 1111 1110
1110 1101 1111 0001 0111 1101 0001 1110 1001 0000 1011 0000

M.9 Whitened and RSC and Interleaved Scenario

M.9.1 Settings

For these examples, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = TRUE
phyFSKFECScheme=1
phyFSKScramblePSDU=TRUE
phyFSKFECInterleavingRSC = TRUE

M.9.2 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.9.3 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening is used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table 8

Table 8: PHR for Whitened and RSC and Interleaved Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	1	0 0 0 0 0 0 0 0 1 1 1

M.9.4 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as

0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0100 1011

M.9.5 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

0000 0000 1110 1000 0010 1000 0001 1111 0011 1010 0000 1010 0000 1010 0000 1010 0011 0011 1001 0100
0001 0001 0101 0011 0000 1110 0110 1001 1101 0101 1110 1100 1010 1110 1100 1010 0011 0000 1110 0101

M.9.6 Interleaving of the bit sequence

Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as

1100 0000 1110 1000 0110 1000 0000 1100 1010 1010 1010 1010 0000 0011 0000 0000 1101 0011 0000 0100
0101 0111 0100 1000 0001 0110 1101 1011 1001 1000 1111 0100 0100 1010 0100 1011 1011 0010 1100 1110

M.9.7 Bit sequence after data whitening of the PSDU

Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as

1100 0000 1110 1000 0110 1000 0000 1100 1010 0101 1101 1010 1011 0000 0110 1111 1001 0000 1001 1100
0001 1111 1110 0110 1010 1010 0100 1100 1010 0000 1110 1001 1001 1001 1001 1111 0001 0010 1001 1011

M.9.8 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as:

0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1100 0000 1110 1000 0110 1000 0000 1100
1010 0101 1101 1010 1011 0000 0110 1111 1001 0000 1001 1100 0001 1111 1110 0110 1010 1010 0100 1100
1010 0000 1110 1001 1001 1001 1001 1111 0001 0010 1001 1011

M.10 4FSK Scenario

M.10.1 Settings

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = FALSE
phyFSKFECScheme=N/A
phyFSKScramblePSDU=FALSE

M.10.2 Generation of the SHR

The bit sequence of the SHR, consisting of eight preamble octets and four SFD octets, is given as

0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 0111 0101 0101 0111 0101 1111 1101

M.10.3 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (0) (data whitening is not used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table 9

Table 9: PHR for 4FSK Scenario

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	0	0 0 0 0 0 0 0 0 1 1 1

M.10.4 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as:

0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 0111 0101 0101 0111 0101 1111 1101 0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

M.11 Mode Switch Scenario

M.11.1 Settings

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = FALSE
phyFSKFECScheme=N/A
phyFSKScramblePSDU=FALSE

In the example, mode switch is used, to switch from filtered 2FSK to filtered 4FSK. Two packets are sent in sequence, the first one is the mode switch packet, sent in the 2-FSK mode, and the second one is the packet encapsulating the message captured in M.1, sent in the 4-FSK mode.

The ModeSwitchParameterEntry (see Figure 106) is assumed to be 0, and the elements of the corresponding ModeSwitchDescriptor (see Tables 124 and 71b) are assumed to be as follows:

- the SettlingDelay is 0
- the SecondaryFSKPreambleLength is 4
- the SecondaryFSKSFD is TRUE.

The NewMode (see Figure 107) is set as follows:

- Page is 0 (channel page seven)
- ModulationScheme is 0 (filtered FSK)
- Mode = 3 (Operating mode #4 using filtered 4-FSK)

M.11.2 Generation of the Mode Switch Packet

M.11.2.1 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.11.2.2 Generation of the PHR

The complete PHR field is shown in Table 10

Table 10: PHR for Mode Switch Scenario

Bit string index	0	1-2	3	4-10	11-14	15
Bit mapping	MS	M_1-M_0	FEC	See Figure 107	B_3-B_0	PC
Field name	Mode Switch	Mode Switch Param Entry	New Mode FEC	New Mode	Checksum	Parity Check
Value	1	0 0	0	0000 011	1100	1

M.11.2.3 Concatenating the SHR with the PHR to form the Mode Switch Packet

The bit sequence for the mode switch PPDU is given as:
0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 1000 0000 0111 1001

M.11.3 Generation of the Packet in the New Mode

This packet is the same as in M.10

M.11.4 Concatenating the Two Packets

The bit sequence is given as:

0101 0101 0101 0101 0101 0101 0101 0101 1001 0000 0100 1110 1000 0000 0111 1001 0111 0111 0111 0111
0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 0111 1101 0111 0101 0101 0111 0101 1111 1101
0000 0000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000