IEEE P802.15
Wireless Personal Area Networks

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Re:	Comment Resolution for TG4g Sponsor Ballot
Abstract	This document presents examples of the processing to generate FSK packets.
Purpose	Proposed resolution for Comment ID 36 (CID 261 in initial sponsor ballot)
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Release	The contributor acknowledges and accepts that this contribution becomes the property of IEEE and may be made publicly available by P802.15.

Proposed resolution to CID 36 (CID 261 of the initial sponsor ballot): Revised. Create Annex M as shown below.

Annex M
(informative)
Examples of encoding a packet for the MR-FSK PHY

M.1 Introduction
The purpose of this annex is to show examples of encoding a packet for the MR-FSK PHY, as described in 16.1. In particular, generation of the PPDU bit sequence is described in detail.

The encoding illustration goes through the following stages:
a) Generating the bit sequence of the SHR
b) Generating the bit sequence of the PHR
c) Generating the bit sequence of the PSDU
d) Concatenating the PHR, PSDU, tail bits and pad bits
e) Encoding the bit sequence of the PSDU with a rate ½ convolutional encoder
f) Interleaving of the code-bit sequence
g) Concatenation to form the PPDU

In this example, all binary sequences of length *n* are treated as bit strings:
$b_0\ b_1$ ..... b_{n-1}
The corresponding entries are processed b_0 first to b_{n-1} last.

M.2 Example with NRNSC FEC enabled, no data whitening

<This example is per what is captured in document 717 rev1, with adjustments on text formatting for consistency with the second example included here. Make adjustments per the draft changes from d5 to d6, e.g. remove line containing the attribute phyFSKFECInterleaving .>

M.3 Example with NRNSC FEC enabled and data whitening enabled

M.3.1 Settings
The frequency band used in these examples is the 915 MHz band, and this example uses Operating Mode #1.

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = TRUE
phyFSKFECScheme=0
phyFSKScramblePSDU=TRUE

In the example mode switch is not used, and the 4-octet FCS is used.

M.3.2 Generation of the SHR

The bit sequence of the SHR, consisting of four preamble octets and two SFD octets, is given as
0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110

M.3.3 Generation of the PHR

The Mode Switch (MS) field is set to (0) (no mode switch), the Reserved field entries are set to (0,0), the FCS Type (FCS) field is set to (0) corresponding to a 4-octet FCS, the Data Whitening (DW) field is set to (1) (data whitening is used), and the Frame Length field entries are set to the binary representation of "7," corresponding to the PSDU length of the packet. The complete PHR field is shown in Table M.1

Table M.1 – PHR for MR-FSK

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length
Value	0	0 0	0	1	0 0 0 0 0 0 0 0 0 1 1 1

M.3.4 The message

The example payload of 7 octets is shown below. It constitutes an acknowledgment frame with a 3-octet MHR and a 4-octet FCS, as defined in 5.2.1.9.
The bit sequence of the example PSDU is
0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000

M.3.5 Concatenating the PHR, PSDU, tail bits, and pad bits

Concatenation of the PHR, PSDU, tail bits, and pad bits is performed as described in 16.1.2.4. After concatenation the bit sequence is given as

0000 1000 0000 0111 0100 0000 0000 0000 0101 0110 0101 1101 0010 1001 1111 1010 0010 1000 0000 1011

M.3.6 Encoding of the bit sequence

Convolutional coding is performed as described in 16.1.2.4. The bit sequence after convolutional coding is given as

1111 1111 0010 0000 1111 1111 1100 0110 1000 0100 0011 1111 1111 1111 1111 1111 1100 10110111 1001
1111 1011 1010 1000 0100 1110 1101 0011 0110 0101 0110 0001 0000 0010 1101 0000 1111 1111 0010 1110

M.3.7 Interleaving of the bit sequence

Interleaving is performed as described in 16.1.2.5. The bit sequence after interleaving is given as

1011 0011 0111 0011 0011 1011 1111 0011 1111 1100 1111 1101 1111 1100 1111 0010 0011 0111 1010 1010
1011 1100 1011 0111 0101 1110 0001 0011 1010 0100 0101 1101 1011 0010 1111 0000 1011 0100 0011 1100

M.3.8 Bit sequence after data whitening of the PSDU

Data whitening of the PSDU is performed as described in 16.1.3. The bit sequence after data whitening is given as

1011 0011 0111 0011 0011 1011 1111 0011 1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010
1111 0100 0001 1001 1110 0010 1000 0100 1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001

M.3.9 Concatenating the SHR with the PHR and PSDU

The bit sequence for the PPDU is given as

0101 0101 0101 0101 0101 0101 0101 0101 0110 1111 0100 1110 1011 0011 0111 0011 0011 1011 1111 0011
1111 0011 1000 1101 0100 1111 1001 1101 0111 0100 0011 0010 1111 0100 0001 1001 1110 0010 1000 0100
1001 1100 0100 0000 0110 0001 0010 0100 0001 0100 0110 1001

M.4 Examples with RSC FEC enabled and data whitening enabled

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = TRUE
phyFSKFECScheme=1
phyFSKScramblePSDU=TRUE

In these examples mode switch is not used, and the 4-octet FCS is used.

M.4.1 Interleaving enabled

For this example, phyFSKFECInterleavingRSC = TRUE

The bit sequence for the PPDU is given as:

< Note to the editors: for the remaining examples in this document, please format the PPDU as per the format shown in example M.3.9 >

Columns 1 through 15
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
Columns 16 through 30
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
Columns 31 through 45
0 1 0 1 1 0 1 1 1 1 0 1 0 0 1
Columns 46 through 60
1 1 0 1 1 0 0 0 0 0 0 1 1 1 0
Columns 61 through 75
1 0 0 0 0 1 1 0 1 0 0 0 0 0 0
Columns 76 through 90
0 1 1 0 0 1 0 1 0 0 1 0 1 1 1
Columns 91 through 105
0 1 1 0 1 0 1 0 1 1 0 0 0 0 0
Columns 106 through 120
1 1 0 1 1 1 1 1 0 0 1 0 0 0 0
Columns 121 through 135
1 0 0 1 1 1 0 0 0 0 0 1 1 1 1
Columns 136 through 150
1 1 1 1 0 0 1 1 0 1 0 1 0 1 0
Columns 151 through 165
1 0 0 1 0 0 1 1 0 0 1 0 1 0 0
Columns 166 through 180
0 0 0 1 1 1 0 1 0 0 1 1 0 0 1

Columns 181 through 195
1 0 0 1 1 0 0 1 1 1 1 1 0 0 0
Columns 196 through 208
1 0 0 1 0 1 0 0 1 1 0 1 1

M.4.2 Interleaving disabled

For this example, phyFSKFECInterleavingRSC = FALSE

The bit sequence for the PPDU is given as:

Columns 1 through 15
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
Columns 16 through 30
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
Columns 31 through 45
0 1 0 1 1 0 1 1 1 1 0 1 0 0 1
Columns 46 through 60
1 1 0 0 0 0 0 0 0 0 0 1 1 1 0
Columns 61 through 75
1 0 0 0 0 0 1 0 1 0 0 0 0 0 0
Columns 76 through 90
1 1 1 1 1 0 0 1 1 0 1 0 1 0 1
Columns 91 through 105
1 1 1 0 1 0 1 0 1 1 1 0 0 1 0
Columns 106 through 120
1 1 0 0 1 0 1 0 1 1 1 0 0 0 0
Columns 121 through 135
0 0 0 0 1 1 0 0 0 1 0 1 1 0 0
Columns 136 through 150
1 1 1 1 1 1 1 0 1 1 0 1 1 0 0
Columns 151 through 165
1 0 1 1 1 1 1 1 1 0 1 1 1 0 1
Columns 166 through 180
1 0 1 1 1 1 1 0 0 0 1 0 1 1 1
Columns 181 through 195
1 1 0 1 0 0 0 1 1 1 1 0 1 0 0
Columns 196 through 208
1 0 0 0 0 1 0 1 1 0 0 0 0

M.5 Examples with RSC FEC enabled and data whitening disabled

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = TRUE
phyFSKFECScheme=1
phyFSKScramblePSDU=FALSE

In these examples mode switch is not used, and the 4-octet FCS is used.

M.5.1 Interleaving disabled

For this example, phyFSKFECInterleavingRSC = FALSE

The bit sequence for the PPDU is given as:

```
Columns 1 through 15
   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0
Columns 16 through 30
   1   0   1   0   1   0   1   0   1   0   1   0   1   0   1
Columns 31 through 45
   0   1   0   1   1   0   1   1   1   1   0   1   0   0   1
Columns 46 through 60
   1   1   0   0   0   0   0   0   0   0   0   0   0   0   0
Columns 61 through 75
   0   0   0   0   0   0   0   0   0   0   0   0   0   0   1
Columns 76 through 90
   1   0   1   1   1   0   0   0   1   0   0   1   0   0   0
Columns 91 through 105
   1   0   0   0   1   0   0   0   1   0   0   0   1   0   0
Columns 106 through 120
   0   1   0   0   0   1   0   0   0   0   1   1   0   1   1
Columns 121 through 135
   1   0   1   1   1   1   0   0   0   0   1   1   1   0   0
Columns 136 through 150
   1   0   1   1   1   1   0   1   1   0   0   1   0   0   1
Columns 151 through 165
   1   0   0   1   0   0   0   0   0   1   1   1   1   1   1
Columns 166 through 180
   1   0   1   1   1   0   0   0   1   0   0   1   0   0   0
Columns 181 through 195
   0   1   1   0   1   1   1   0   0   0   1   0   1   1   1
Columns 196 through 208
   1   0   0   0   0   1   1   1   0   0   1   0   1
```

M.5.2 Interleaving enabled

For this example, phyFSKFECInterleavingRSC = TRUE

```
Columns 1 through 17
   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0
Columns 18 through 34
   1   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0   1
Columns 35 through 51
   1   0   1   1   1   1   0   1   0   0   1   1   1   0   1   1   0
Columns 52 through 68
   0   0   0   0   0   0   1   0   0   0   0   0   0   1   1   0   0
Columns 69 through 85
   0   0   0   0   0   0   0   0   0   0   0   0   0   1   0   1   0   1
Columns 86 through 102
   0   1   0   0   0   0   0   0   0   0   0   0   1   0   1   0   1   0
Columns 103 through 119
   0   1   0   0   0   0   0   0   0   0   1   1   0   1   0   0   1
```

Columns 120 through 136
1 1 0 1 0 1 1 1 0 1 1 1 1 1 1 0 1
Columns 137 through 153
0 1 0 0 1 0 0 0 0 0 0 1 0 1 1 0 0
Columns 154 through 170
1 1 1 0 0 0 1 0 0 1 1 0 0 1 0 1 1
Columns 171 through 187
1 1 0 1 0 0 0 1 0 0 1 0 1 0 0 1 0
Columns 188 through 204
0 0 0 0 1 1 0 1 1 1 0 0 0 1 1 1 1
Columns 205 through 208
1 1 1 0

M.6 Example with FEC disabled and data whitening disabled

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = FALSE
phyFSKFECScheme=N/A
phyFSKScramblePSDU=FALSE

In the example mode switch is not used, and the 4-octet FCS is used.

The bit sequence for the PPDU is given as:

Columns 1 through 17
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
Columns 18 through 34
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0
Columns 35 through 51
0 1 0 0 0 0 0 1 0 0 1 1 1 0 0 0 0
Columns 52 through 68
0 0 0 0 0 0 0 0 0 0 1 1 1 0 1 0 0
Columns 69 through 85
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0
Columns 86 through 102
1 1 0 0 1 0 1 1 1 0 1 0 0 1 0 1 0
Columns 103 through 119
0 1 1 1 1 1 1 0 1 0 0 0 1 0 1 0 0
Column 120
0

M.7 Example with FEC disabled and data whitening enabled

For this example, selected PIB attributes are set as follows:
phyFSKPreambleLength=4
phyMRFSKSFD = 0
phyFSKFECEnabled = FALSE
phyFSKFECScheme=N/A

phyFSKScramblePSDU=TRUE

In the example mode switch is not used, and the 4-octet FCS is used.

The bit sequence for the PPDU is given as:

```
Columns 1 through 17
   0    1    0    1    0    1    0    1    0    1    0    1    0    1    0    1    0
Columns 18 through 34
   1    0    1    0    1    0    1    0    1    0    1    0    1    0    1    1    0
Columns 35 through 51
   0    1    0    0    0    0    0    1    0    0    1    1    1    0    0    0    0
Columns 52 through 68
   0    1    0    0    0    0    0    0    0    0    1    1    1    0    1    0    0
Columns 69 through 85
   0    0    0    0    0    0    0    0    0    0    0    0    0    1    0    1    1
Columns 86 through 102
   0    0    1    0    0    1    0    1    1    0    1    1    0    0    1    1    0
Columns 103 through 119
   1    0    1    0    0    1    0    1    0    1    0    1    1    0    1    0    1
Column 120
   1
```