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Abstract: Graphene is emerging as an attractive electronic material for ultra-high speed electronics due to its exceptionally high carrier mobility and saturation velocity. However, the conventional dielectric integration and device fabrication processes cannot be readily applied to graphene transistors because they can often introduce substantial defects into the monolayer of carbon lattices and severely degrade the device performance. Here I will discuss the opportunities, challenges and recent progresses in exploring graphene for high speed transistors.

Purpose: Overview of the potential of graphene for terahertz electronics.

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Approaching Terahertz Transistors with Graphene

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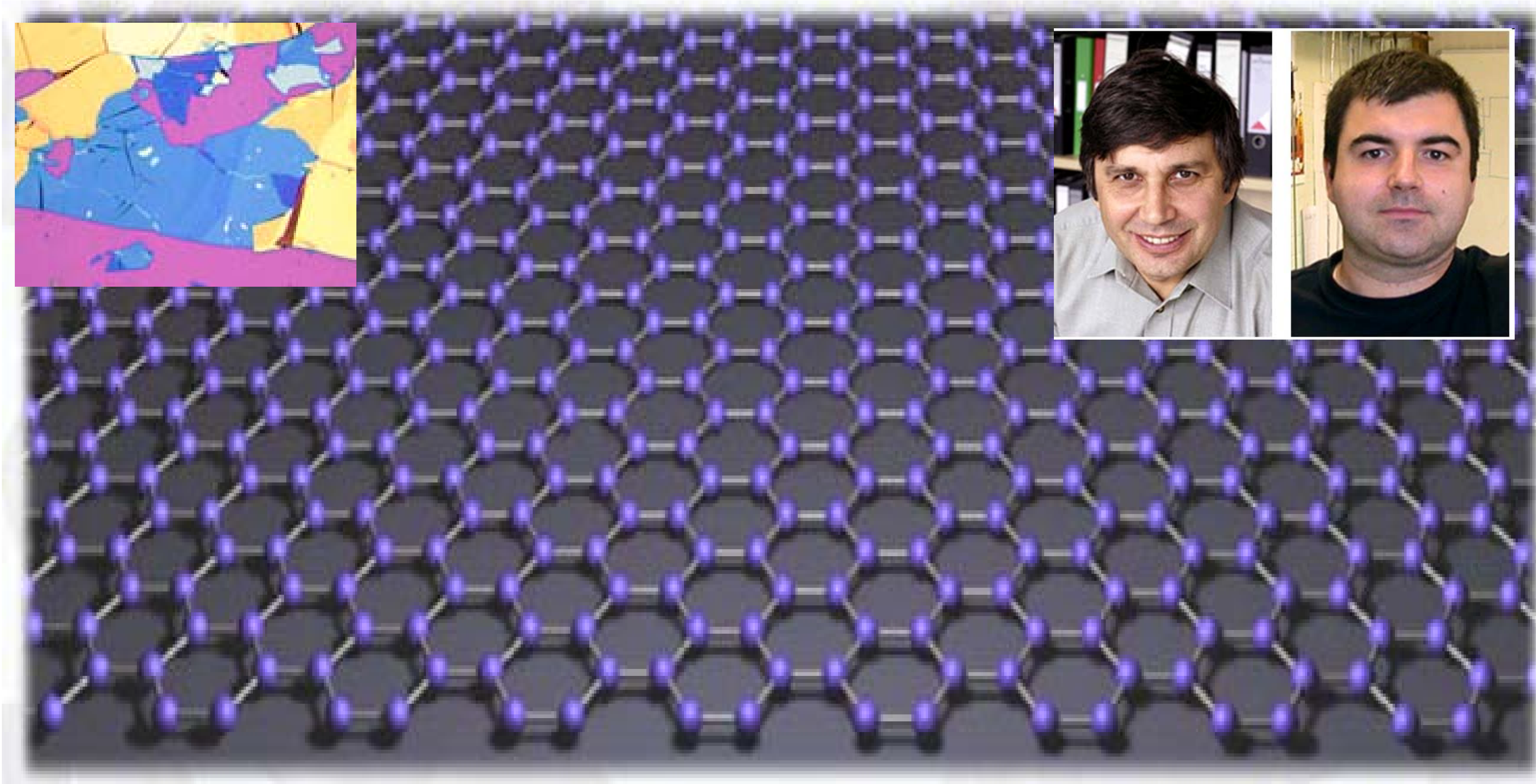
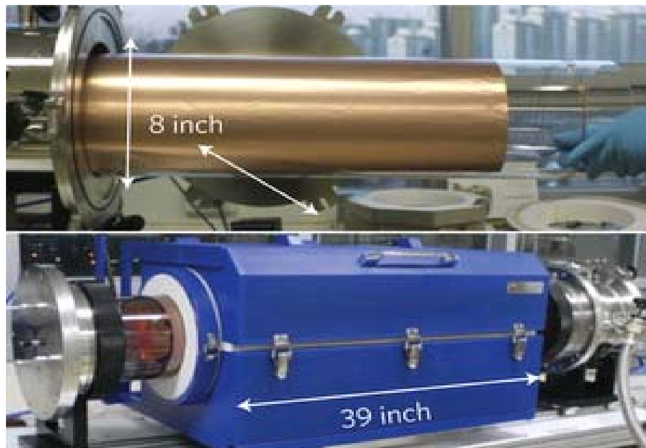
Graphene

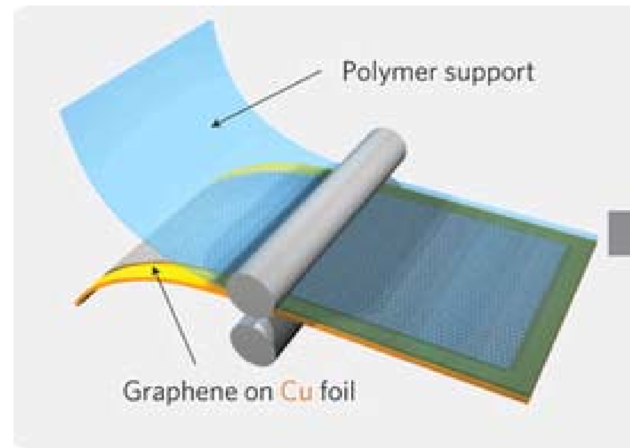
a Two-Dimensional Atomic Thin Film



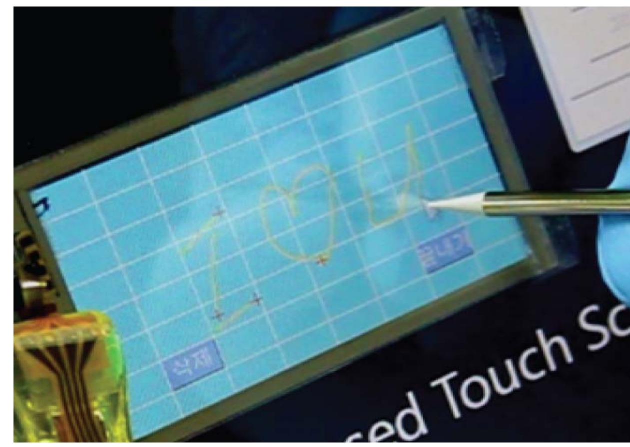
Two dimensional thin film structure may allow for scalable fabrication of electronic circuits.

Large Area Graphene





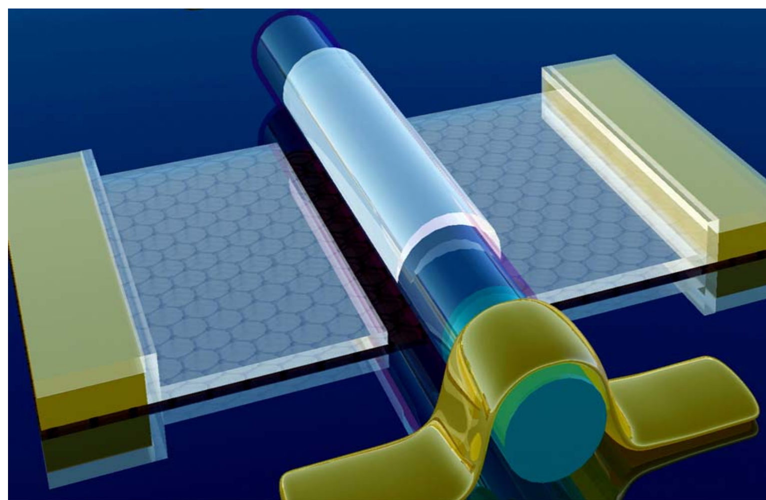
Nature Nanotech. 5, 574 (2010)



With just a few years of development, we have seen tremendous development with >30" single layer graphene now possible using CVD.

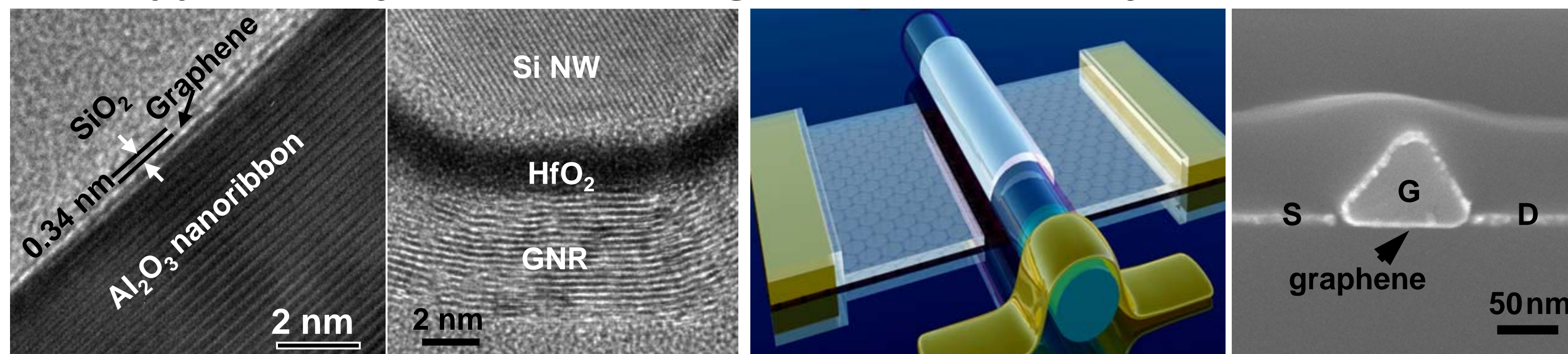
Graphene for High Speed Electronics

- Single atomic thickness
- Highest carrier mobility up to 200,000 -1,000,000 $cm^2 V^{-1}s^{-1}$
- Highest saturation velocity (~5.5×10^7 cm/s)
- High thermal conductivity (~5,000 $Wm^{-1}K^{-1}$)
- Exceptional mechanical strength and flexibility
- Optically transparency
- Chemically inertness



Challenges to High performance Graphene Transistors

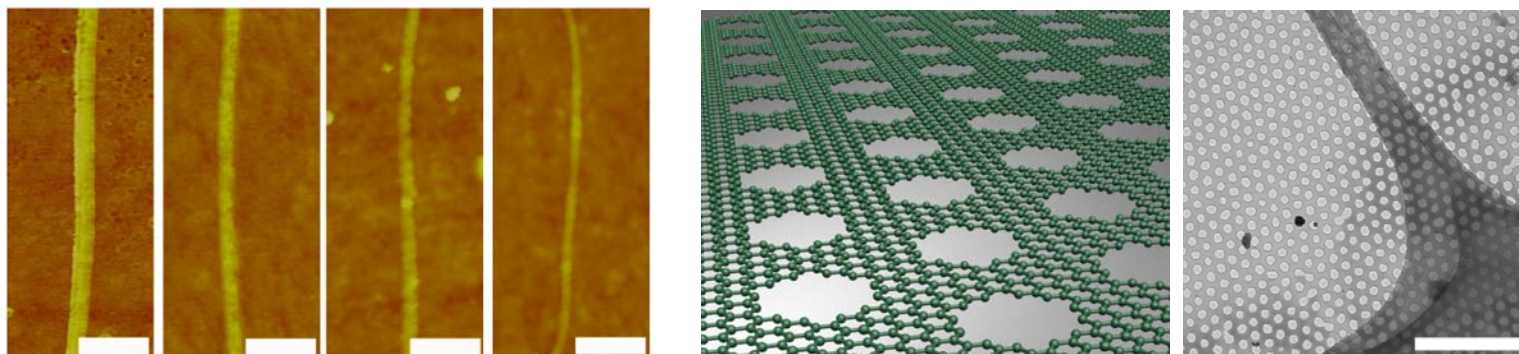
1. New approaches for material integration and device fabrication



Dielectric integration: *PNAS, 107, 6711: Adv. Mater. 22, 2941; Nano Lett. 10 , 1917; 11 , 2555.*

Device fabrication: *Nature, 467, 305; Nano Lett. 10 , 3952* ， NanoLett. 10.1021/nl201922c

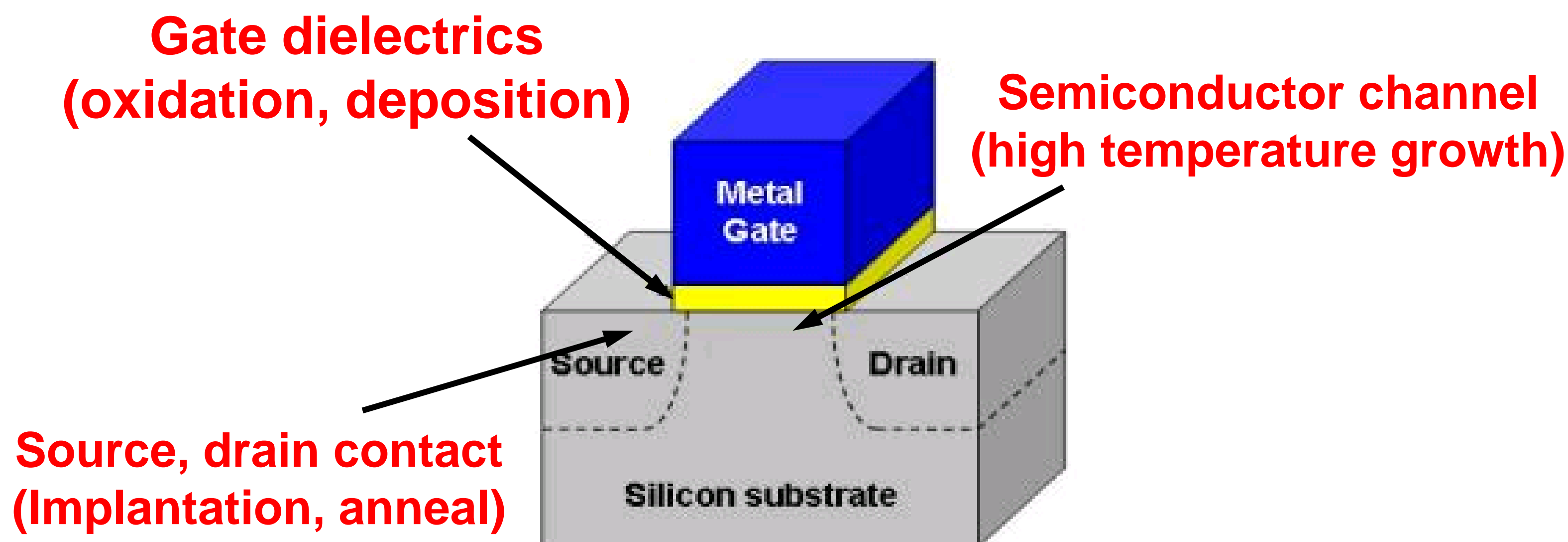
2. Induce a band-gap: graphene nanostructures



Nanoribbon: *Nano Lett., 9, 2083 (2009); 10 , 4590; 11, 1082 (2011) Nature Nano 5, 655, (2010).*

Nanomesh: *Nature Nano 5, 190, (2010); Chem Phys. Lett. 498,334 (2010).*

Challenges to High performance Graphene Transistors



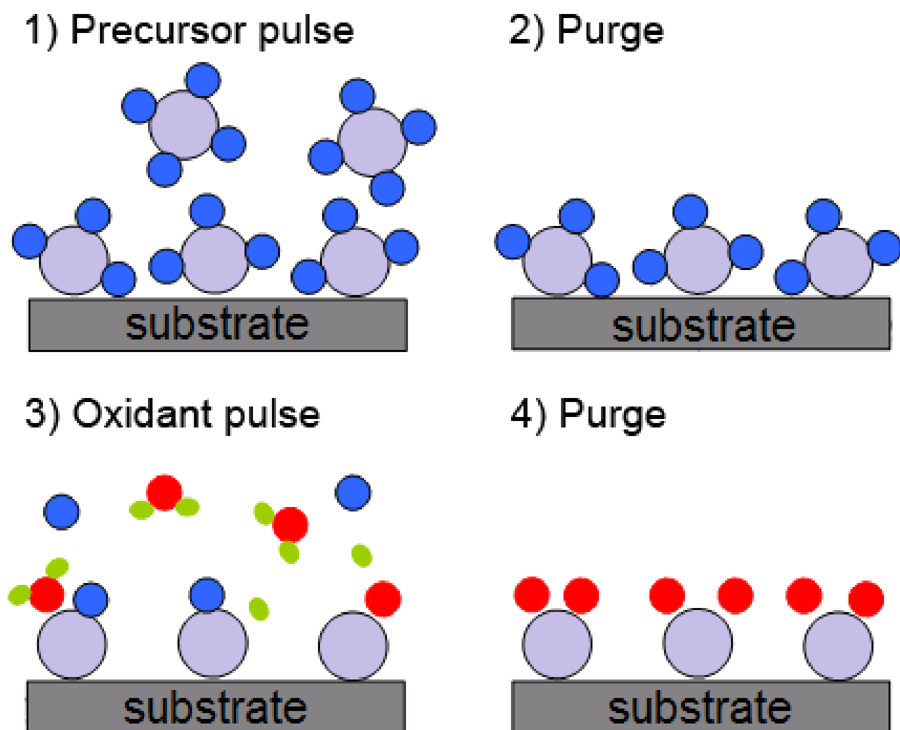
❖ To form a transistor requires effective integration with other material components including gate dielectrics and source drain contacts.

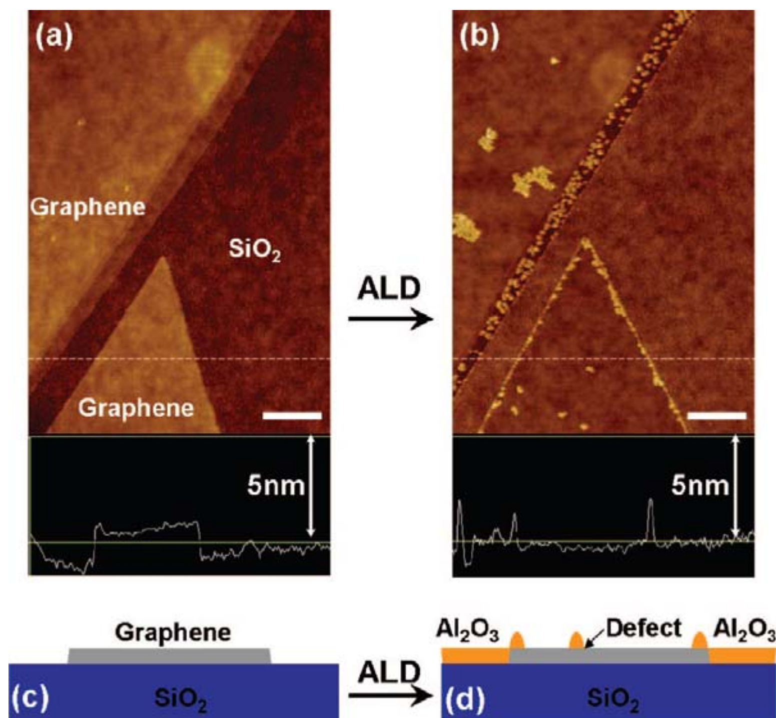
❖ Conventional electronic fabrication processes cannot be readily applied to graphene as many of these processes steps could create substantial damage to single atomic layer gaphene.

❖ Alterative material integration or device fabrication strategies are needed to retain the high electronic performance and truly capitalize the intrinsic merit of graphene.

Graphene-Dielectric Integration

ALD Dielectric Oxide Film on Graphene



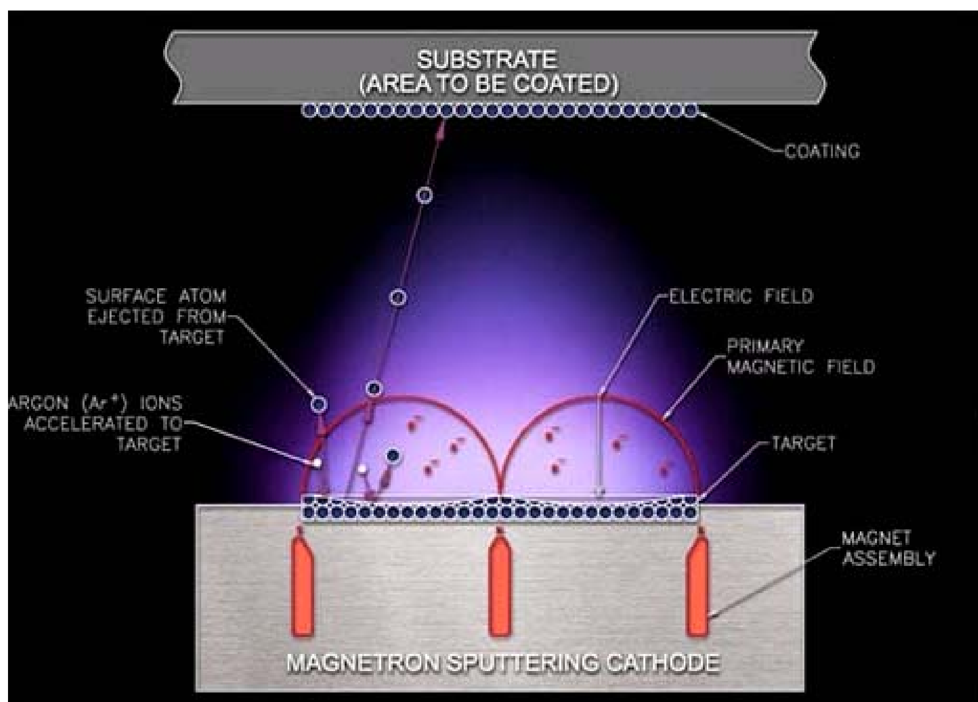


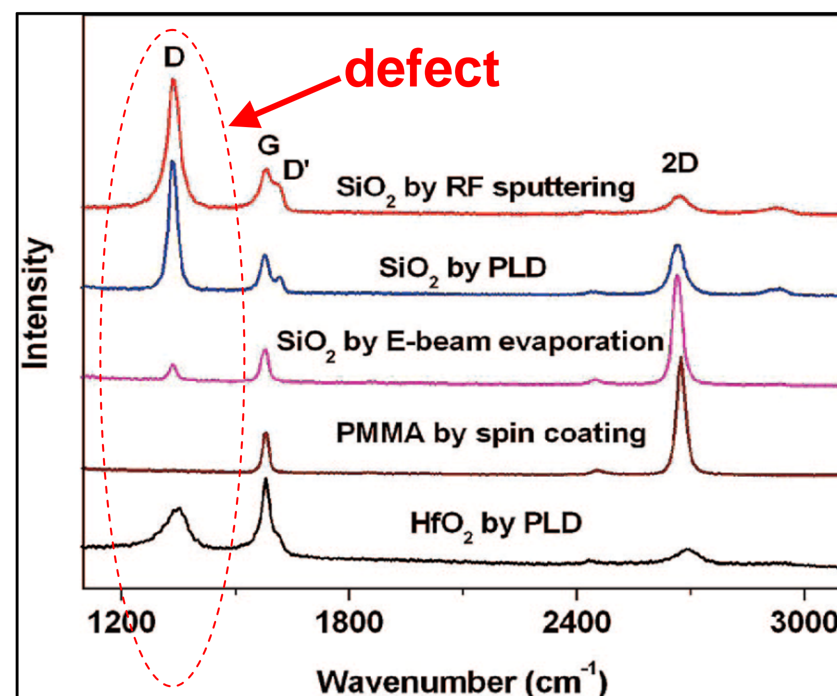
❖ Atomic-layer deposition (ALD) requires functionalization of graphene surface to render surface reactive groups for the deposition of high-k dielectrics.

❖ This process either introduces undesired impurities or breaks the chemical bond in pristine graphene lattice, inevitably leading to a significant degradation in carrier mobilities. *JACS 130, 8152 (2008).*

Graphene-Dielectric Integration

PVD Dielectric Oxide Film on Graphene





❖ Physical vapor deposition (PVD) such as electron-beam evaporation or sputtering process often results in lower quality dielectrics and also significant damages to graphene layer.

ACS Nano, 2, 1033 (2008).

Substantial Mobility Degradation in Top-Gated Devices

Top Gate Dielectrics	Mobility before Deposition	Mobility after Deposition
Al_2O_3 by ALD	1200 $cm^2/V{\cdot}s$	400 $cm^2/V{\cdot}s$
SiO_2 by evaporation	4790 $cm^2/V{\cdot}s$	790 $cm^2/V{\cdot}s$
SiO_2 by evaporation	1700 $cm^2/V{\cdot}s$	500 $cm^2/V{\cdot}s$
HfO_2 by ALD	2400 $cm^2/V{\cdot}s$	1200 $cm^2/V{\cdot}s$

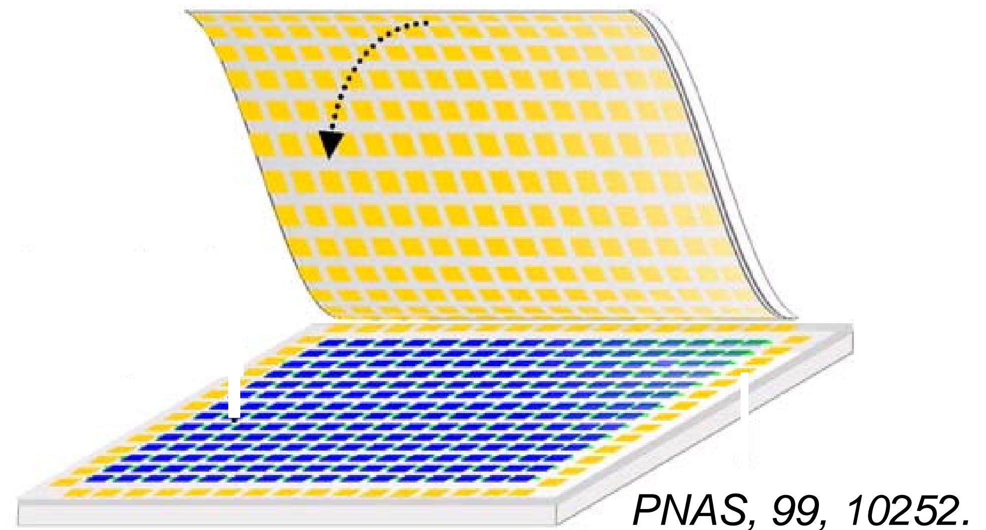
HfO_2 by ALD with polymer buffer layer: ~ 7600 $cm^2/V{\cdot}s$

The mobility values observed in the top-gated devices to date are often nearly one order of magnitude smaller than what can be achieved in the back-gated devices

Nano Lett. **9**, 422 (2009); *Nano Lett.* **9**, 4474 (2009); *Appl. Phys. Lett.* **95**, 033103 (2009); *IEEE Electron Dev. Lett.* **28**, 282 (2007); *Nat. Nanotech.* **3**, 654 (2008); *Appl. Phys. Lett.* **94**, 062107 (2009).

Post-growth Integration of Dielectric Thin film as Top gate Dielectrics

Physical Integration (e.g. Lamination)

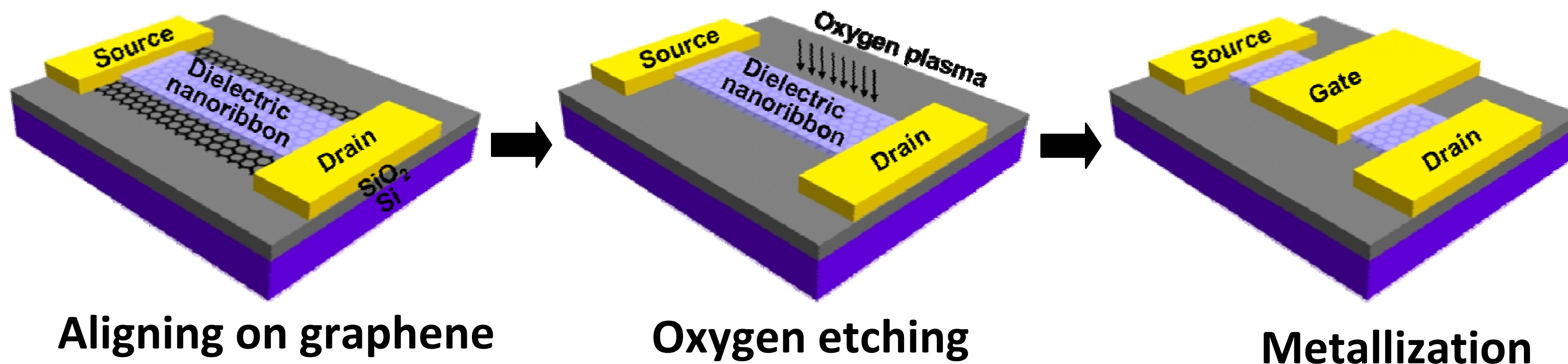


PNAS, 99, 10252.

❖ The post-growth can allow integration of distinct materials or processes that are normally either chemically or structurally incompatible.

Post-growth Integration of Dielectric Thin film as Top gate Dielectrics

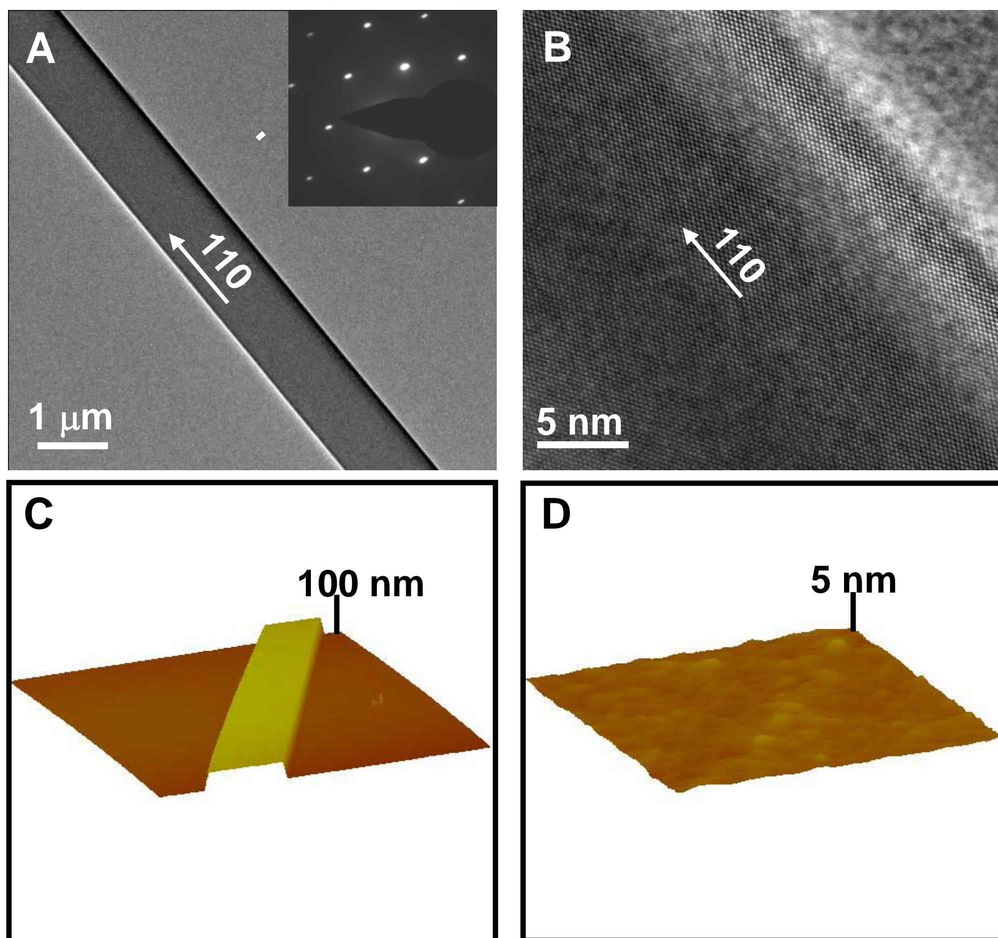
Physical Integration (e.g. Lamination)



The physical assembly approach can effectively integrate dielectric nanostructures with graphene without introducing any appreciable defects into the graphene lattice, and thus can effectively preserve the high carrier mobility in the resulting devices.

PNAS 107, 6711-6715 (2010).

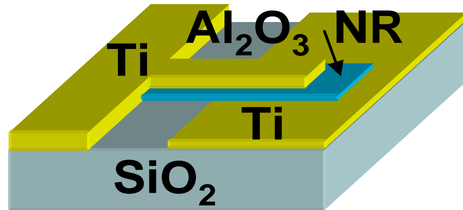
Al_2O_3 Nanoribbon



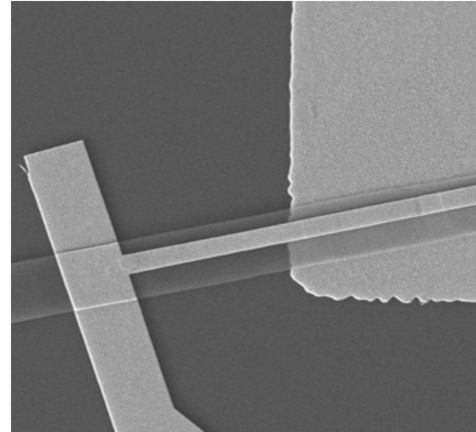
Single crystalline, Smooth surface, High dielectric constant

PNAS 107, 6711-6715 (2010).

Dielectric Properties of Al_2O_3 Nanoribbon



MIM device



$$J = AE_{OX}^2 \exp(-B/E_{OX})$$

$$A = 1.54 \times 10^{-6} \left\{ \frac{1}{m^* \Phi_B} \right\}$$

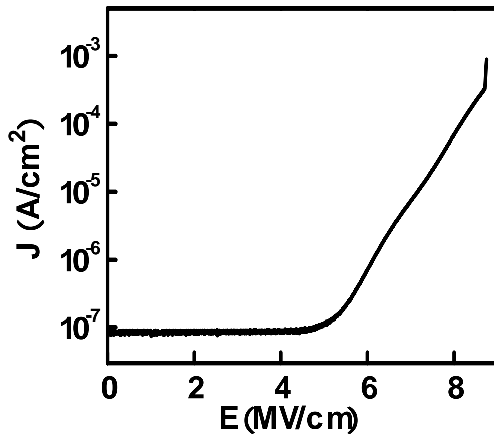
$$B = 6.83 \times 10^7 (m^*)^{1/2} (\Phi_B)^{3/2}$$

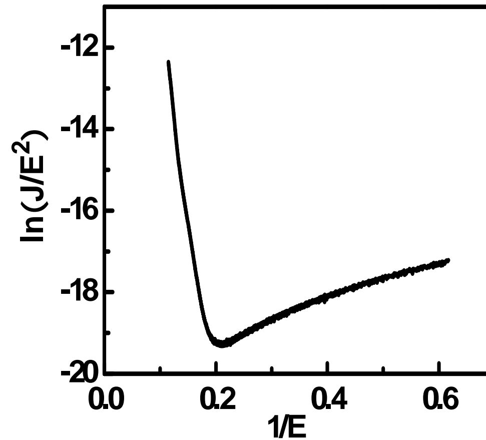
J : current density

E_{ox} : oxide electric field

m^* : effective mass of the charge carrier ~$0.23m_e$

Φ_B : barrier height



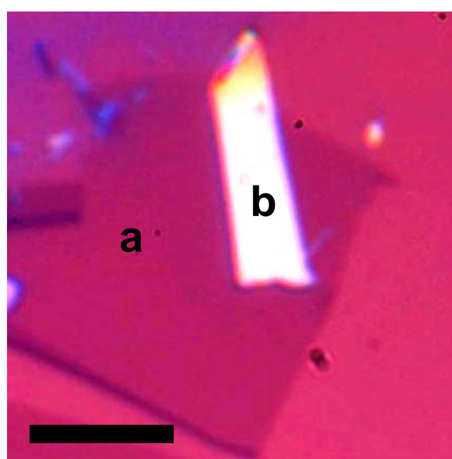


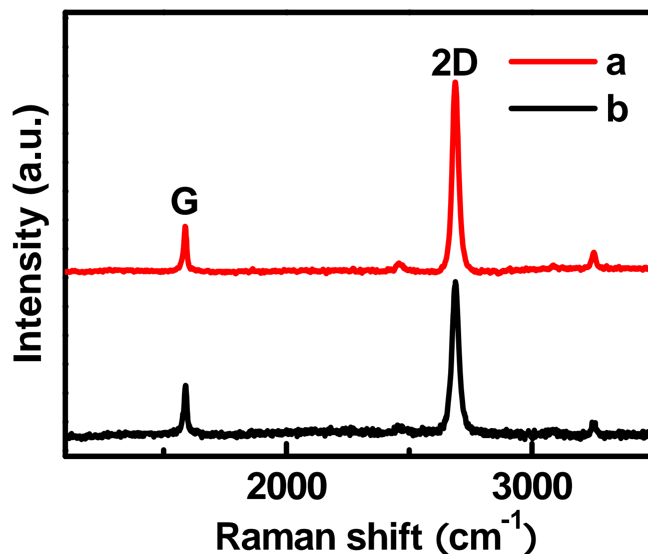
$\Phi_{B\,(Ti/Al2O3)}$ = 2.0 eV

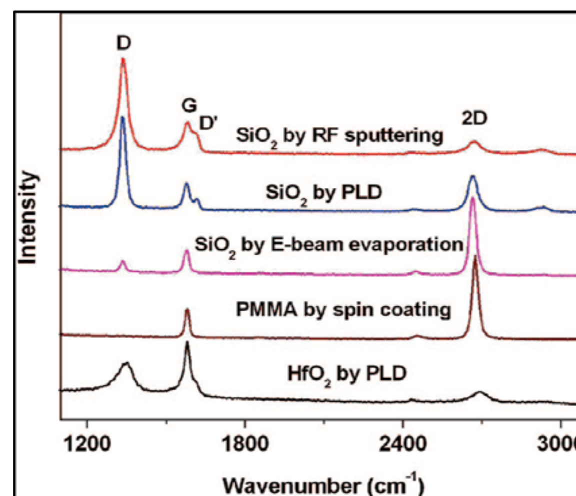
$\varepsilon_{(Al2O3)}$ = 8.5

The current-voltage (I-V) measurements show typical Fowler–Nordheim (F-N) tunnelling behaviour with a breakdown field of 8.5 MV/cm, comparable to/better than best reported ALD Al_2O_3 film.

Integration of Graphene and Nanoribbon



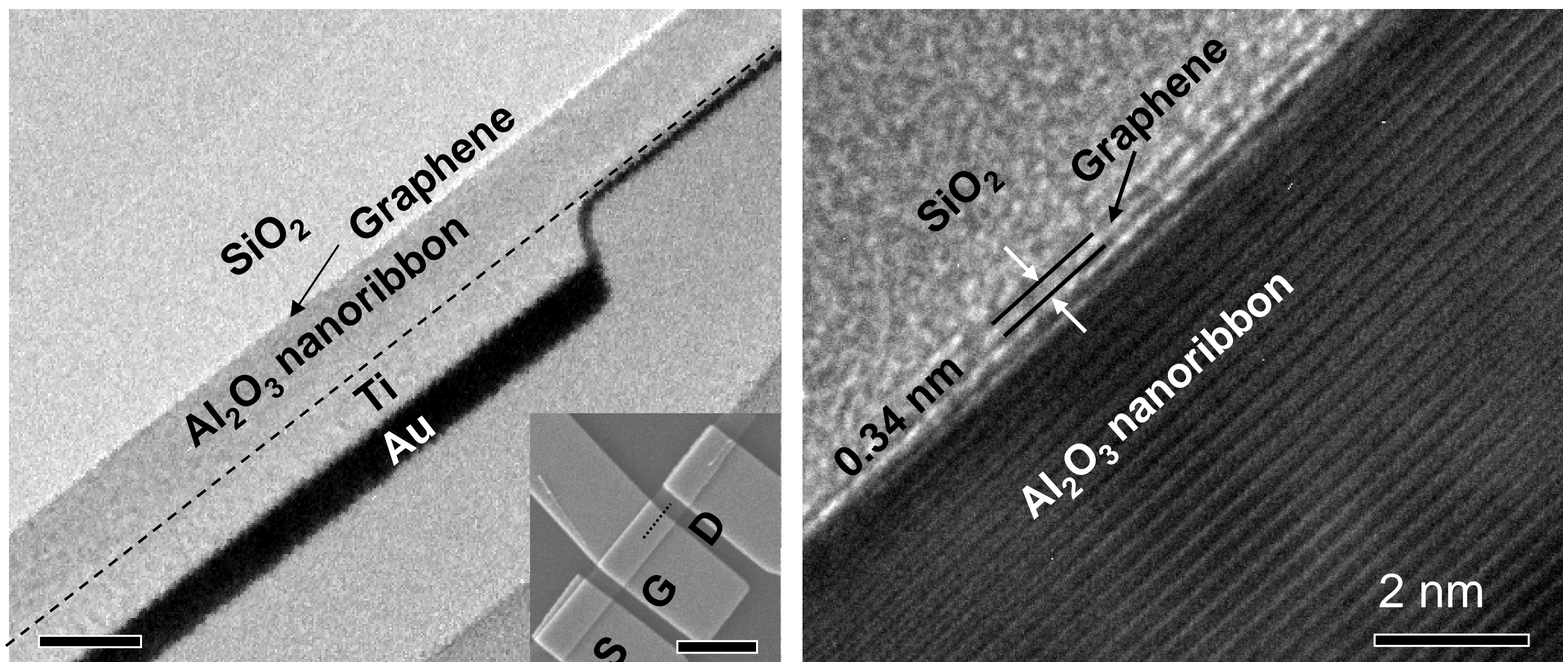




ACS Nano, 2, 1033 (2008)

Raman studies clearly demonstrate that the room-temperature physical assembly approach to integrate oxide nanostructures with graphene does not introduce any appreciable defects into the graphene lattice.

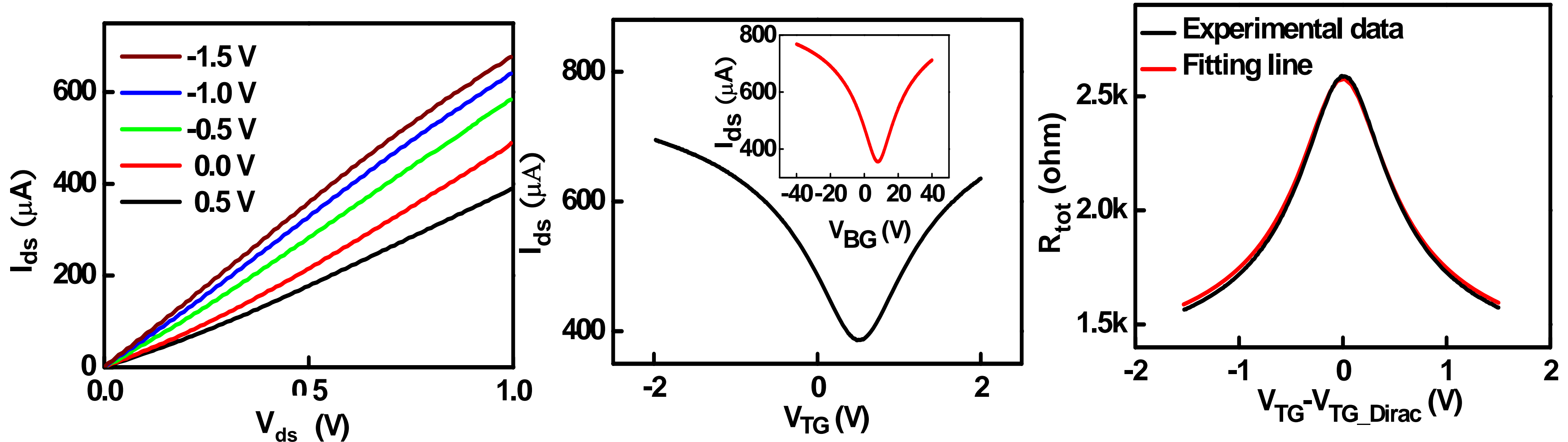
Seamless Integration between Graphene and Nanoribbon



Cross-sectional TEM studies show that there are no gaps or other impurities at the graphene/dielectric interface.

PNAS 107, 6711-6715 (2010).

Top-gated Graphene Transistor



❖ Top-gated device exhibits typical transistor characteristics with a max g_m of about 290 mS, which is more than 15 times larger than that of the back-gated device (g_m ~19.5 mS).

❖ The derived mobility value reaches 22,400 cm^2/V·s using the constant mobility model:

$$R_{tot} = R_{contact} + R_{channel} = R_{contact} + \frac{L/W}{ne\mu}$$

PNAS 107, 6711-6715 (2010).

Mobilities in Al_2O_3 Nano-ribbon Top-gated Graphene Transistors

Device No.	1	2	3	4	5	6	7	8	9
Thickness (nm)	38	45	48	50	60	65	75	82	150
Mobility ($cm^2/V \cdot s$)	23600	22400	18200	22600	11200	15300	21100	11800	13300

- The mobilities achieved in our device represent **the highest mobility** achieved to date in top-gated graphene devices.
- The presence of Al_2O_3 nanoribbon on top of graphene does not lead to any mobility degradation.

PNAS 107, 6711-6715 (2010).

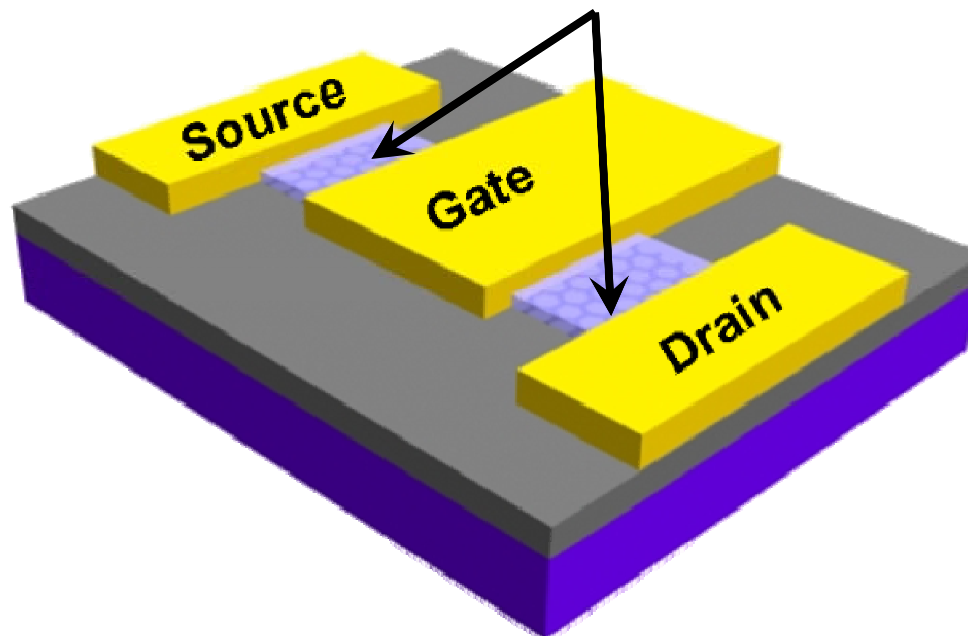
Towards a High Speed Transistor

Cutoff Frequency:

$$\tau_t = \frac{L_{gate}}{v_{drift}} = \frac{C_g}{g_m}$$

$$f_{T,intrinsic} = \frac{1}{2\pi\tau_t}$$

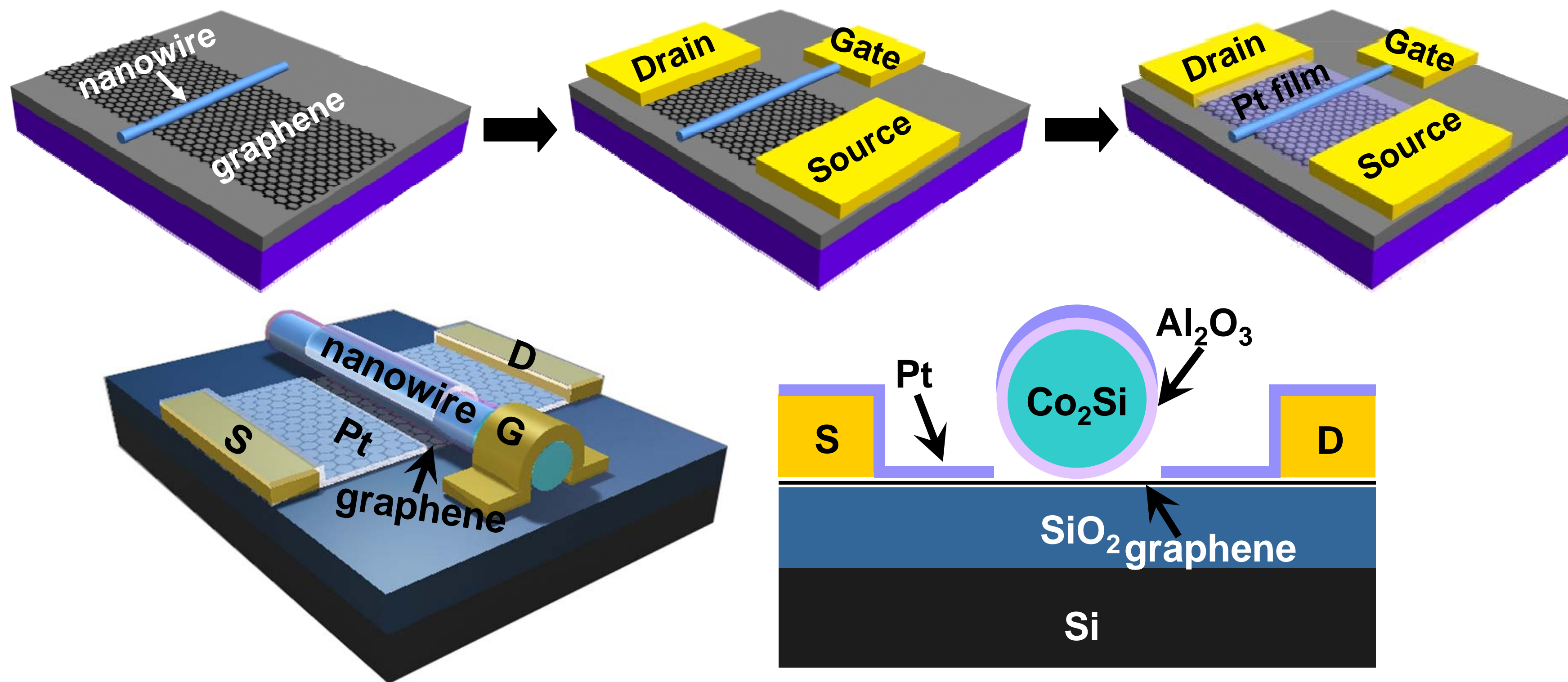
$$= \frac{v_{drift}}{2\pi L_{gate}} = \frac{g_m}{2\pi C_g}$$



❖ Substantial access resistance due to the significant gaps between the source-gate and gate-drain electrodes, where a large portion of the graphene channel in the gap area is not gated.

❖ With the size of the device shrinking into the deep nanometer regime, there is an increasing need for a more precise and reliable device fabrication process.

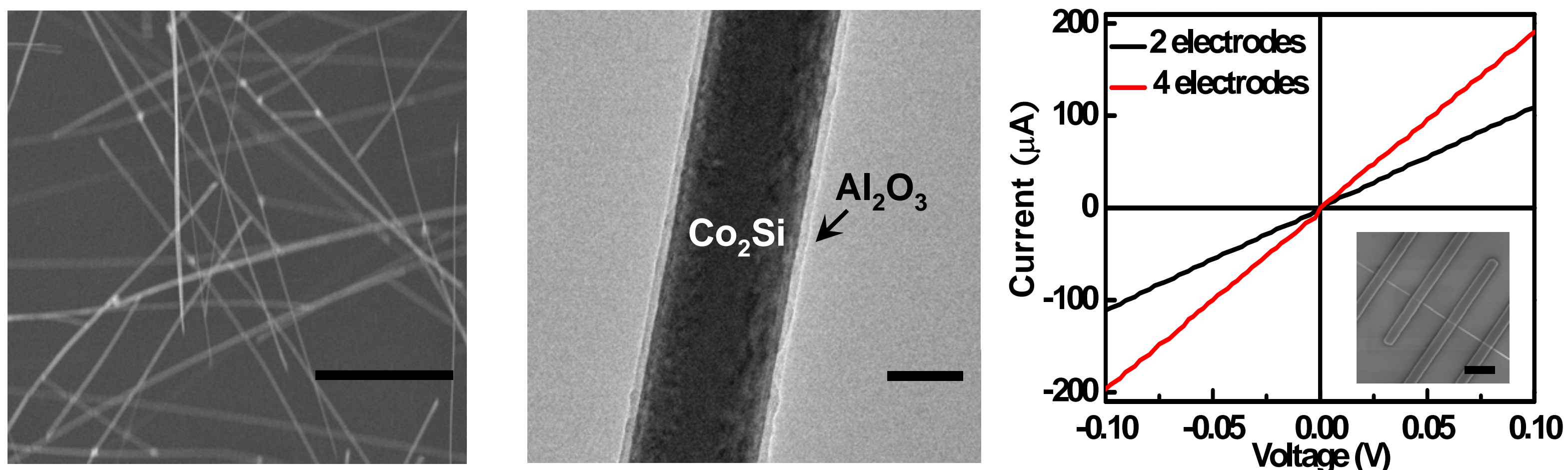
Self-Aligned Graphene Transistors with a Nanowire Gate



❖ **The physical assembly of nanowire gate preserves the high carrier mobility in graphene and the self-aligned source-drain electrodes minimize the access resistance and therefore can enable transistor performance not previously achievable.**

Nature 467, 305 (2010).

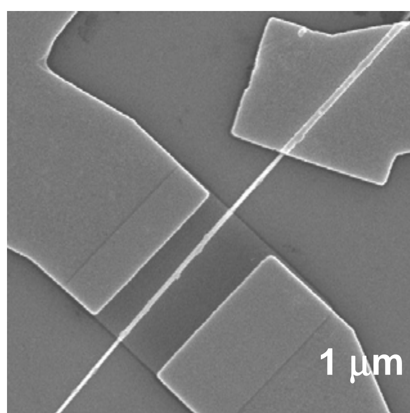
Co_2Si-Al_2O_3 Core-shell Nanowires

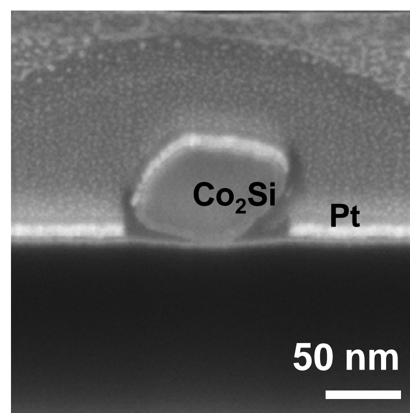


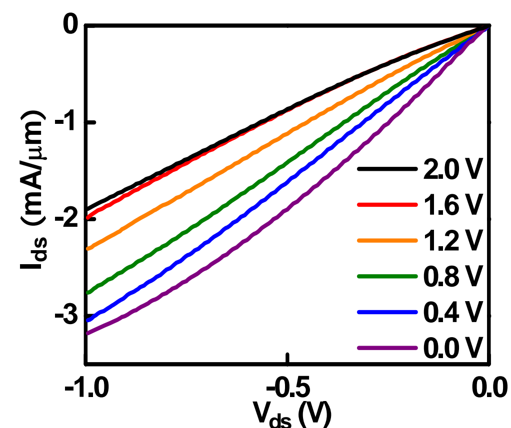
- The Co_2Si/Al_2O_3 core/shell nanowires can be synthesized through CVD growth of Co_2Si nanowires followed by ALD deposition of Al_2O_3 shell.
- The Co2Si/Al2O3 core/shell nanowires show a low resistivity, which is particularly important for them to function as effective gate electrodes for RF graphene transistors (to reduce gate RC delay).

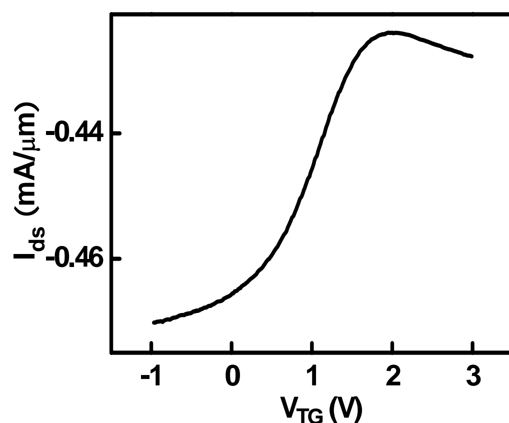
Nature 467, 305 (2010).

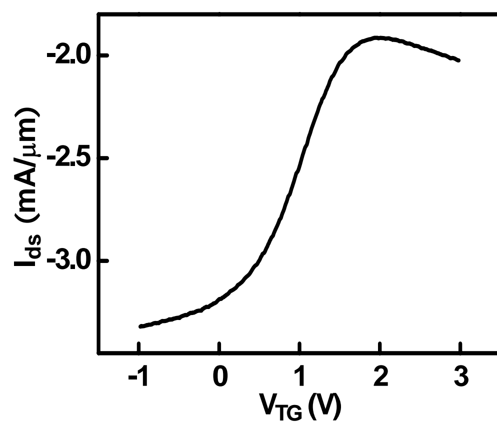
High Performance Short Channel Graphene Transistors

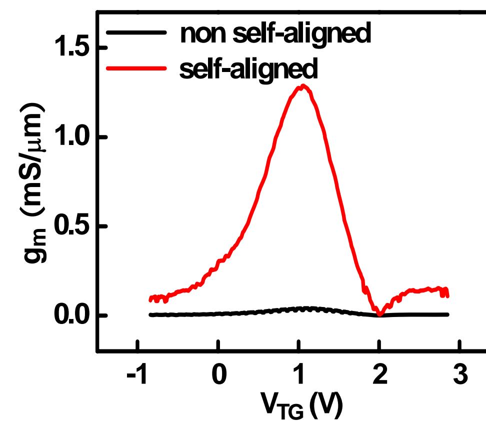






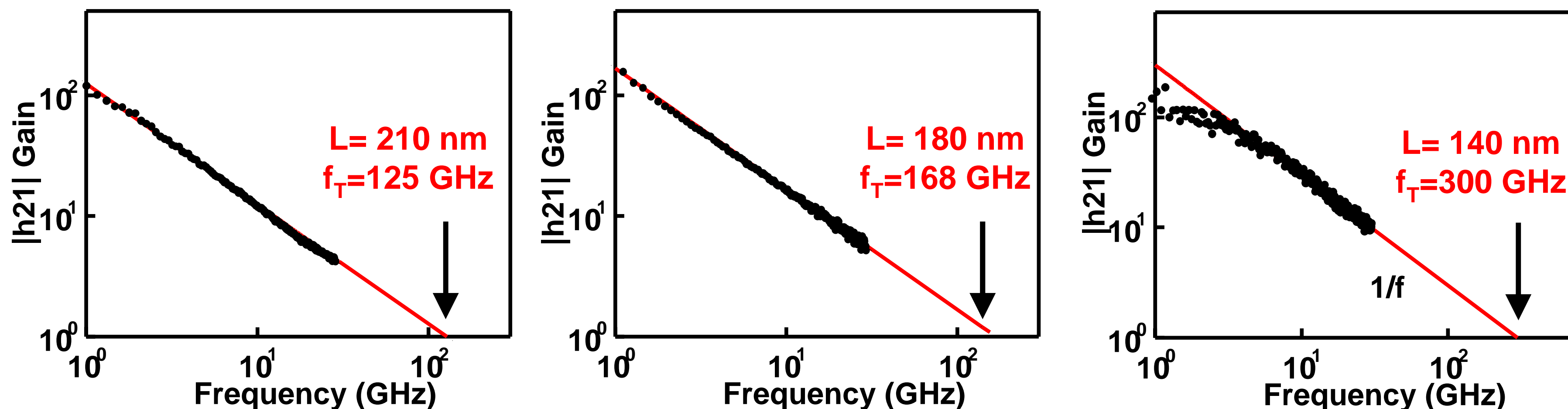






❖ The self-alignment allow a more 60 times improvement in trans-conductance to reach 1.27 ms/μm, promising ultrahigh speed transistors: $f_T = g_m/(2\pi C_g)$ ~323 GHz.

Graphene Transistor with f_T up to 300 GHz

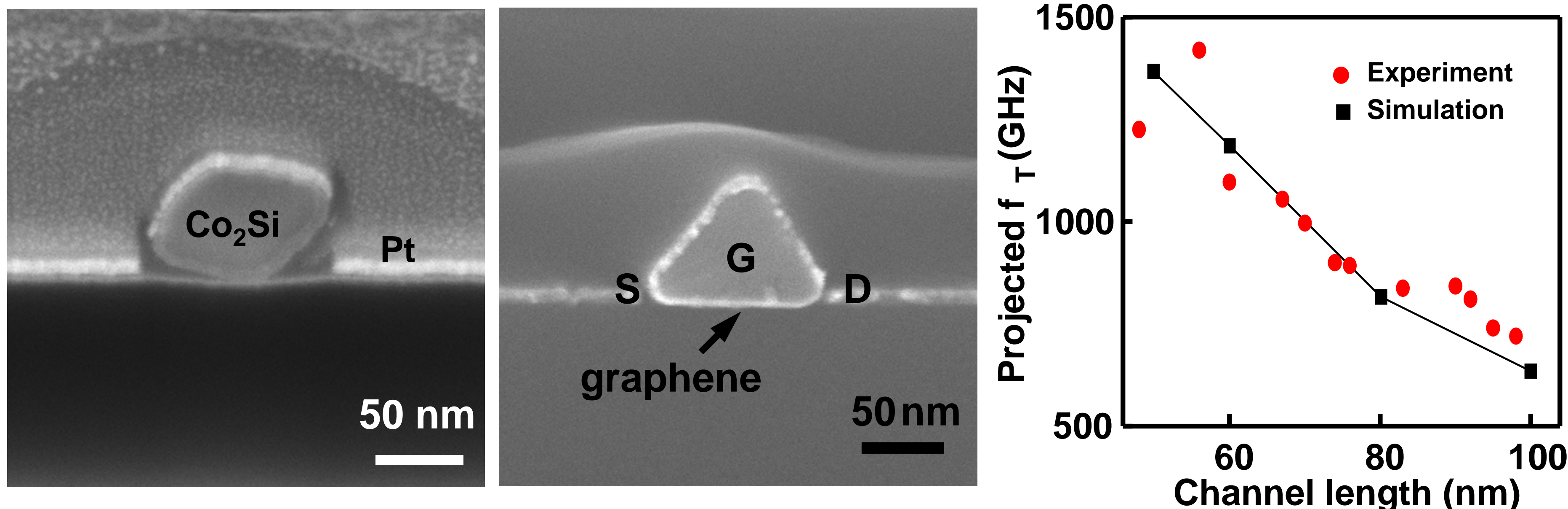


❖ On-chip microwave measurements demonstrate record high intrinsic cutoff frequency (f_T) in the range of 100-300 GHz,.

❖ The cutoff frequency of the graphene transistors is comparable to that of the very best high electron mobility transistors with similar gate lengths, marking an important milestone in graphene RF devices and can enable exciting opportunities in high-speed electronics.

Nature 467, 305 (2010).

Approaching Terahertz Transistors



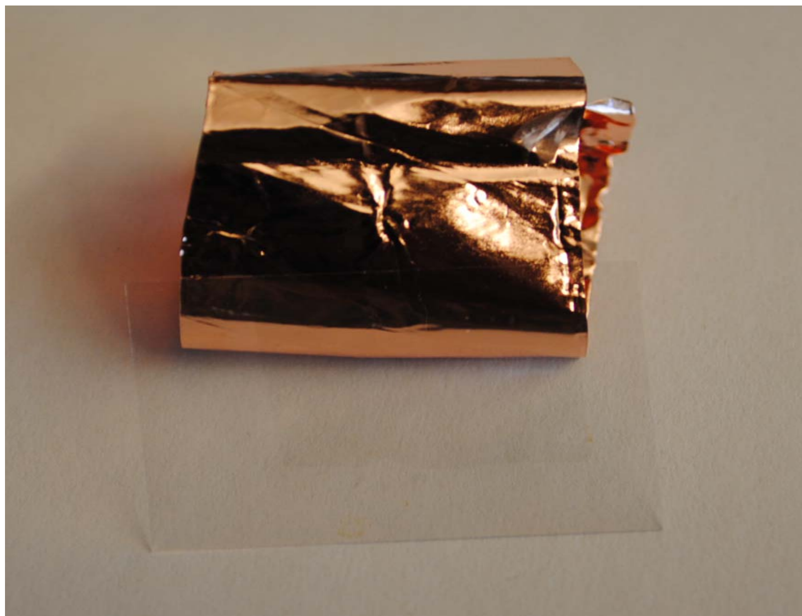
❖ Nanowire gate with a flat side surface allows seamless integration between the nanowire gate and graphene to ensure excellent gate coupling to further improve the device performance.

❖ Channel length dependent studies predicts terahertz graphene transistors is achievable in sub-70 nm graphene transistors: **$f_T \approx 70$ GHz/L_{gate}(in μm), matching well with parallel theory work using self-consistent quantum simulations (by Jing Guo, Nano Research, 2011, DOI: 10.1007/s12274-011-0113-1).**

Nano Lett. **10**, 3952-3956 (2010)

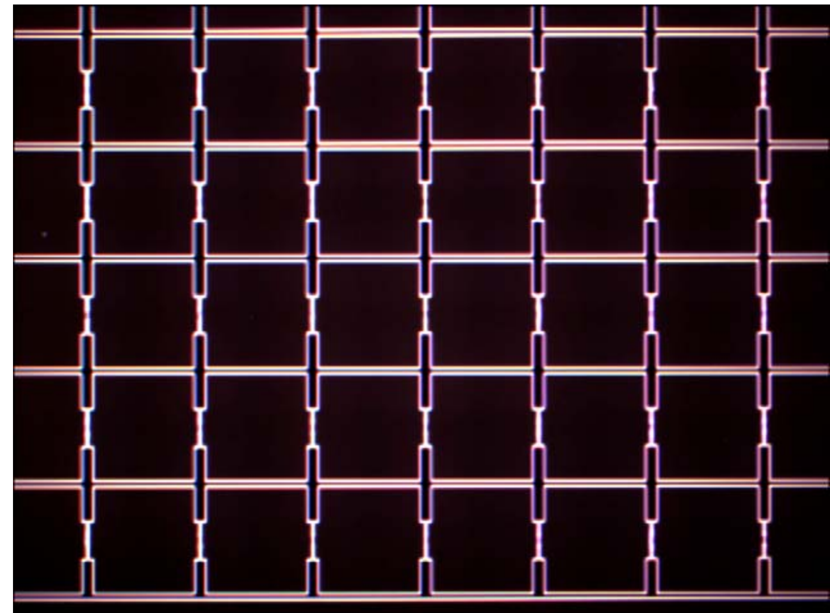
Towards Scalable Graphene Transistors

Large Area Graphene



Chemical vapor deposition and transfer of large area graphene on variable substrate

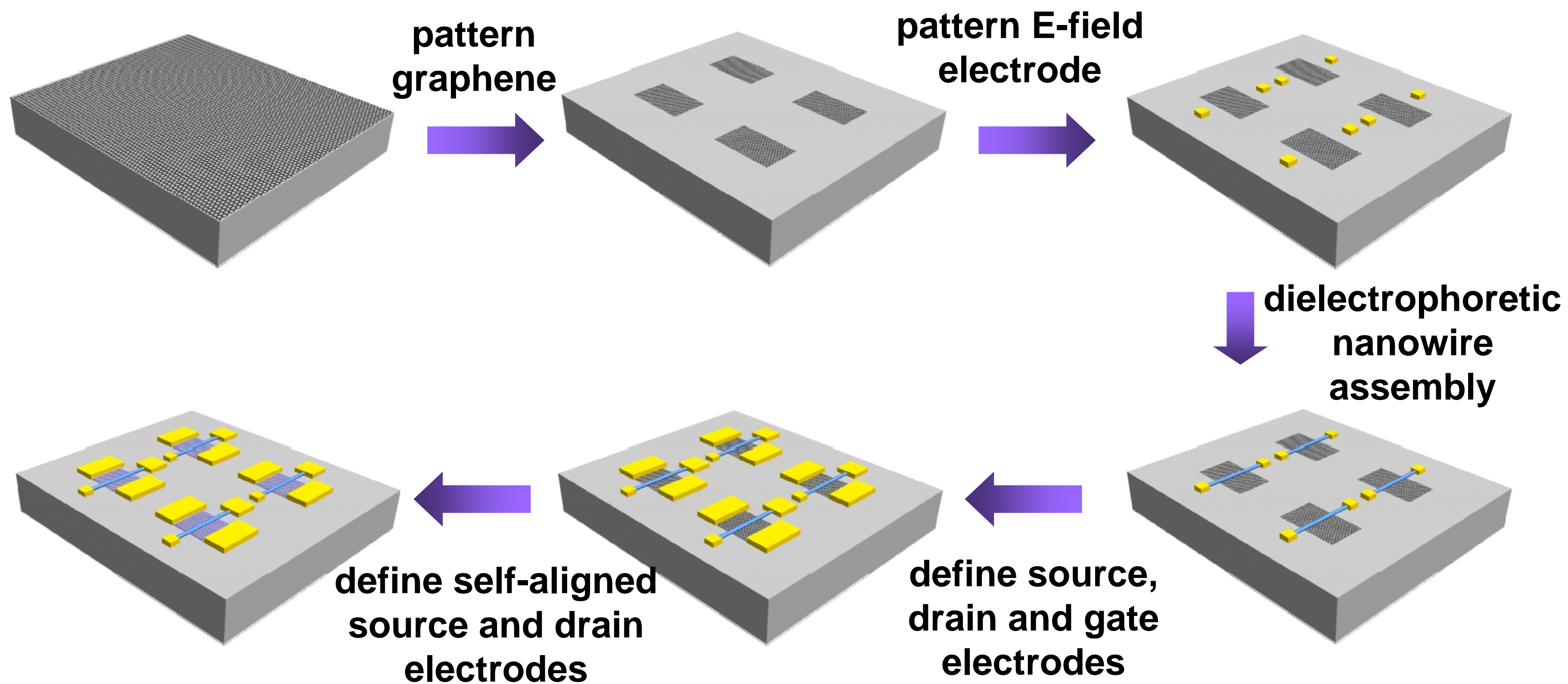
Nanowire Gate Array



High-yield self-limiting dielectrophoresis assembly of single nanowires

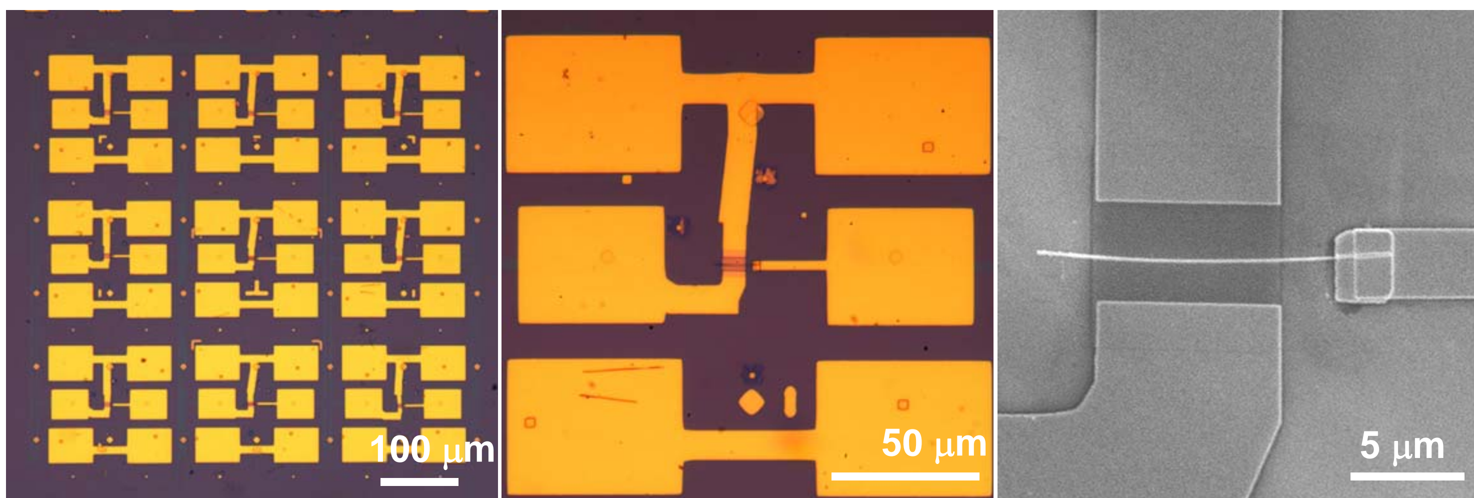
Nature Nanotechnol. **5**, 525 (2010)

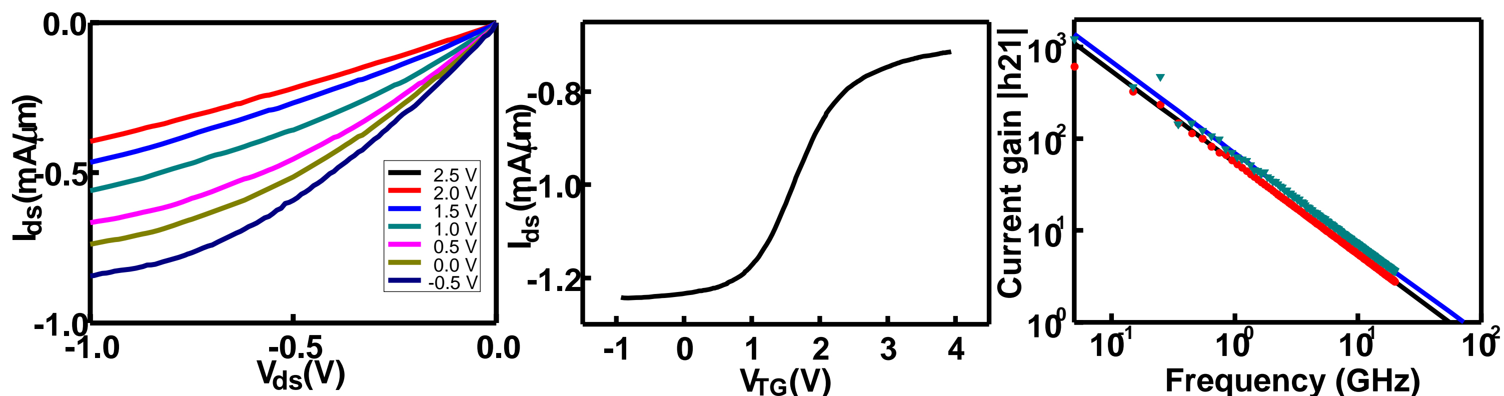
Towards Scalable Graphene Transistors



Nano Letters, 2011

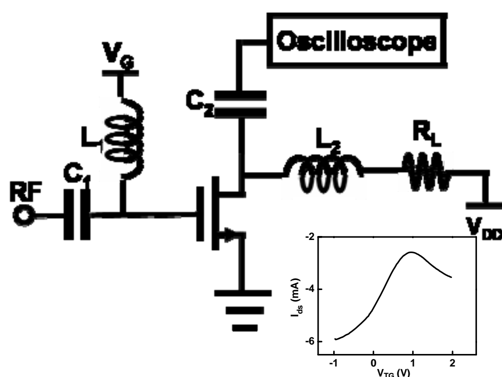
Towards Scalable Graphene Transistors

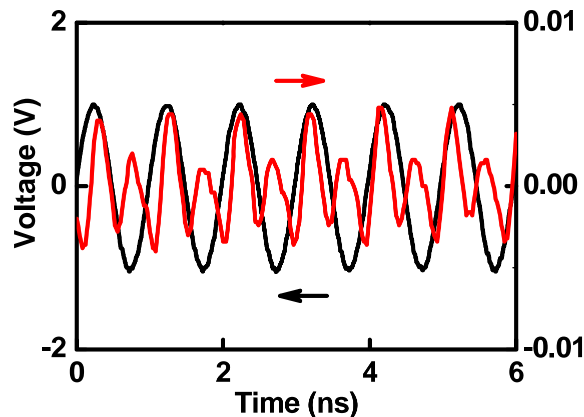


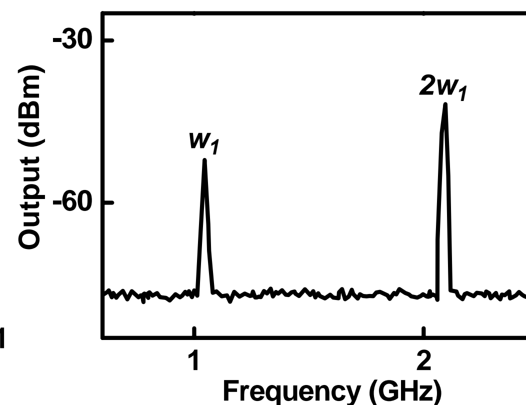


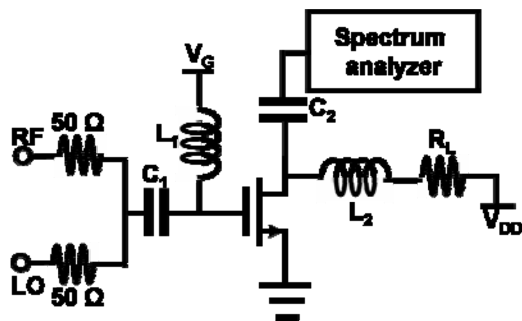
Nano Letters, 2011

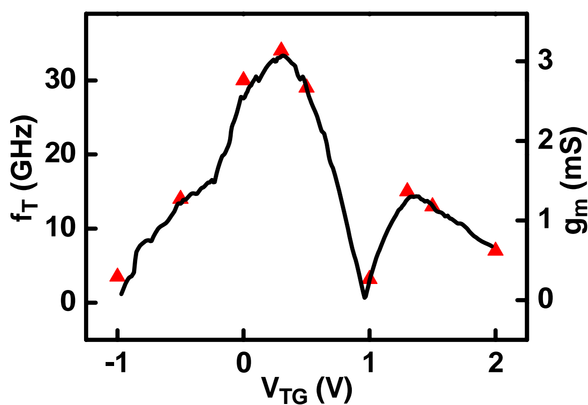
Gigahertz Graphene Functional Circuits RF Doubler and Mixer

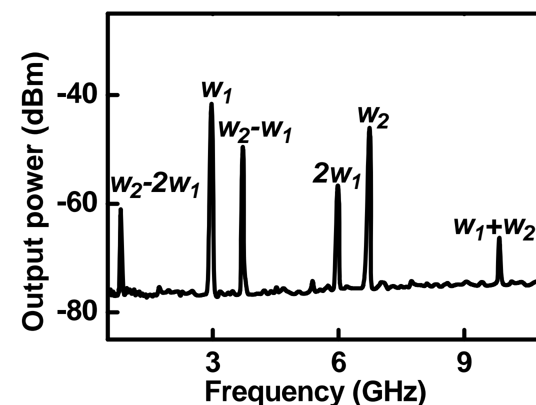












Nano Letters, 2011

Summary

- Graphene is emerging as an interesting material system for high speed electronics, but often require unconventional processes.
- The physical assembly approach allows seamless integration of graphene with top-gate dielectrics without introducing any appreciable defects to preserve the high carrier mobility.
- The self-aligned approach allows automatic and nearly perfect alignment of gate, source and drain electrodes, to enable short-channel graphene transistors with unprecedented speed.
- The combination of CVD graphene and dielectrophoretic assembly allows scalable fabrication high speed graphene transistors and circuits.