

IEEE P802.15
Wireless Personal Area Networks

Project	IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)	
Title	CRC contents for HCS and FCS	
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Re:		
Abstract	CRC related contents which will be moved to annex	
Purpose	[TG 7 received about PHY header related comments in LB. This document is the response about PHY header comments]	
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6.4.1.5 HCS

The PHY header shall be protected with a 2 octet CRC-16 header check sequence (HCS). A schematic of the CRC processing is shown in annex J. The HCS bits shall be processed in the transmit order. The registers shall be initialized to all ones.

7.2.1.9 FCS

The FCS field is 2 octets in length and contains a 16-bit ITU-T CRC. A schematic of the CRC processing is shown in annex J. The FCS is calculated over the MHR and MAC payload parts of the frame.

Annex J

The HCS and FCS shall be calculated using the following standard generator polynomial of degree 16:

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1 \quad (1)$$

The CRC shall be calculated for transmission using the following algorithm:

- Let $M(x) = b_0x^{k-1} + b_1x^{k-2} + \dots + b_{k-2}x + b_{k-1}$ be the polynomial representing the sequence of bits for which the checksum is to be computed.
- Multiply $M(x)$ by x^{16} , giving the polynomial $x^{16} \times M(x)$.
- Divide $x^{16} \times M(x)$ modulo 2 by the generator polynomial, $G_{16}(x)$, to obtain the remainder polynomial, $R(x) = r_0x^{15} + r_1x^{14} + \dots + r_{14}x + r_{15}$.
- The FCS field is given by the coefficients of the remainder polynomial, $R(x)$.

Here, binary polynomials are represented as bit strings, in highest polynomial degree first order.

As an example, consider an acknowledgment frame with no payload and the following 3 byte MHR:

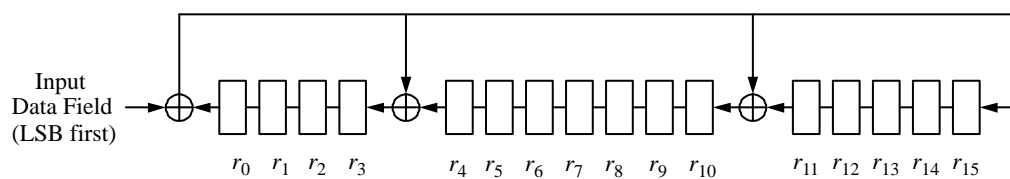
0100 0000 0000 0000 0101 0110 [leftmost bit (b_0) transmitted first in time]
 b_0 b_{23}

The HCS and FCS for this case would be the following:

0010 0111 1001 1110 [leftmost bit (r_0) transmitted first in time]
 r_0 r_{15}

A typical implementation is depicted in figure 63.

CRC-16 Generator Polynomial: $G(x) = x^{16} + x^{12} + x^5 + 1$



1. Initialize the remainder register (r_0 through r_{15}) to zero.
2. Shift MHR and payload into the divider in the order of transmission (LSB first).
3. After the last bit of the data field is shifted into the divider, the remainder register contains the FCS.
4. The FCS is appended to the data field so that r_0 is transmitted first.

Figure 63 Typical FCS implementation