

IEEE P802.15
Wireless Personal Area Networks

Project	IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)	
Title	Modified PHY Header	
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Re:		
Abstract	Modified PHY Header based on LB comments	
Purpose	[TG 7 received about PHY header related comments in LB. This document is a response about PHY header comments]	
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서식 있음: 글꼴: (한글) + 본문
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한글, (한글) 한국어

삭제됨: CSK constellation

삭제됨: CSK constellation

6.4 PDU format

This clause specifies the format of the PDU packet.

For convenience, the PDU packet structure is presented so that the leftmost field as written in this standard shall be transmitted or received first. All multiple octet fields shall be transmitted or received least significant octet first and each octet shall be transmitted or received least significant bit (LSB) first. The same transmission order should apply to data fields transferred between the PHY and MAC sublayer.

Each PDU packet consists of the following basic components:

- A SHR, which allows a receiving device to synchronize and lock onto the bit stream.
- A PHR, which contains frame length information.
- A variable length payload, which carries the MAC sublayer frame.

6.4.1 General packet format

The PDU packet structure shall be formatted as illustrated in Figure 21.

Preamble (see 6.4.1.1)	Burst mode (see 6.4.1.3.1)	Channel number (see 6.4.1.3.2)	MCS ID (see 6.4.1.3.3)	Length of PSDU (see 6.4.1.3.4)	Reserved fields (see 6.4.1.3.5)	HCS (see 6.4.1.3.6)	Channel estimation sequence (Option) (see 6.4.1.5)	PSDU (see 6.4.1.6)
SHR		PHR					PHY Payload	

Figure 21—Format of the PDU

6.4.1.1 Preamble field

The preamble field is used by the transceiver to obtain chip and symbol synchronization with an incoming message. The standard defines one fast locking pattern followed by choice of 4 preambles for the purposes of distinguishing different PHY topologies.

The preamble first starts with a fast locking pattern of at least 64 alternate 1's and 0's. This maximum transition sequence provides the ability to lock the clock and data recovery circuit in the quickest time. The fast locking pattern length shall not exceed 16384 bits. Before the clock and data recovery (CDR) attains lock and recovers the clock, it has no way of determining the logic value of the transmitted sequence. After the fast locking pattern, 4 repetitions of one of four preambles are sent.

Octets: variable	
Preamble	Frame (7 b)
SHR	

삭제됨:

In the case of CSK, the CSK PDU of Figure 22 is used after link establishment. . . . [1]

변경된 필드 코드

서식 있음: 가운데

Octets: variable	
Preamble	Frame length (7 bits)
SHR	

삭제됨:

서식 있음: 글꼴: (영어) Arial, (한글) 맑은 고딕, 10 pt

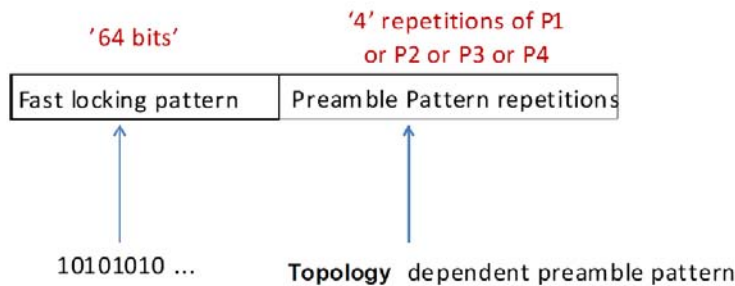


Figure 23—Default preamble transmission

P1:	1	1	1	1	0	1	0	1	1	0	0	1	0	0	0
P2:	0	0	1	0	1	1	1	0	1	1	1	1	1	1	0
P3:	1	0	0	1	1	0	0	0	0	0	1	0	0	1	1
P4:	0	1	0	0	0	0	1	1	0	1	0	0	1	0	1

Figure 24—Preambles for various topology modes

The preamble of Figure 24 shall be transmitted using an OOK modulation. If there are multiple light sources supported by the device, all light sources shall transmit the same preamble simultaneously.

It is also acceptable to invert the proposed preamble sequences and transmit; that is, the PHY can select whether to transmit each preamble sequence or its inversion. The advantage of doing this is that this allows for two preamble sequences to be searched for simultaneously at the receiver for a given MAC operating mode and allow co-existence of two piconets in a given operating mode, without any increase in complexity.

The same preamble sequences are used for low rate and high rate PHY. The number of repetitions of the fast locking pattern can be extended by the MAC during idle time or for different operating modes for better synchronization or to provide visibility or image array device discovery.

P1 can be used with any topology and can also be used for visibility support frames.

6.4.1.2 Preamble for burst mode

The fast locking pattern can be dropped for the burst mode since it is already synchronized to the transmitter. This reduces the preamble length by half and provides higher throughput at the MAC layer.

Table 21—Preamble for MAC operation code

Preamble	Topology operating mode
P1 or inverted P1	topology independent
P2 or inverted P2	peer to peer
P3 or inverted P3	star
P4 or inverted P4	broadcast

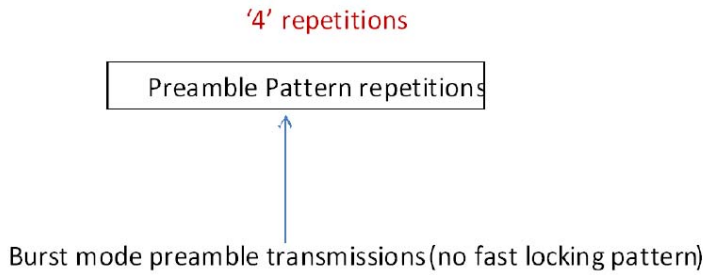


Figure 25—Burst preamble transmission

6.4.1.3 PHY header

The header, as shown in Table 23, shall be transmitted with an OOK modulation. If there are multiple light sources supported by the device, all light sources shall transmit the same header contents simultaneously. The band plan ID field in this case shall be that of the lowest band plan ID.

Table 23—PHY Header

PHY header fields	Bit width	Explanation on use
Burst mode	1	Reduce preamble and IFS
Channel number	3	Band plan ID
MCS ID	6	Provide information on PHY type and data rate
Length of PSDU	16	Length up to aMaxPHYPacketSize (Table 24)
Reserved fields	6	Future use
HCS	16	Header check sequence

서식 있음: 글꼴: 10 pt
 서식 있음: 가운데
 서식 있는 표

6.4.1.3.1 Burst mode

The burst mode bit is for the next packet. It indicates that next packet is burst mode. Refer to 6.4.1.2 Preamble for burst mode for more detailed information.

서식 있음: 글꼴: 10 pt
 서식 있음: 표준, 간격 단락 뒤: 0 pt
 서식 있음: 기본 단락 글꼴, 글꼴: (한글) + 본문 한글, 굵게 없음, (한글) 한국어

6.4.1.3.2 Channel number

Channel number is code in Table 1. The codes in Table 1 are used to indicate the frequency band containing the spectral peak (energy) for the transmitted packet. Refer to 6.1.2 Operating frequency range and channel assignments for more detailed information.

서식 있음: SC4008, 글꼴: (한글) 맑은 고딕, 12 pt, 굵게, 글꼴 색: 자동
 서식 있음: SP196634, 간격 앞: 24 pt
 서식 있음: 글꼴 색: 자동

6.4.1.3.3 MCS ID

서식 있음: 글꼴: 굵게 없음
 서식 있음: 글꼴: 10 pt
 서식 있음: SC4008, 글꼴: (한글) 맑은 고딕, 12 pt, 굵게, 글꼴 색: 자동

MCS indication	PHY type	Data rate	unit
0	000000	1	11.67 kbps
1	000001	1	24.44 kbps
2	000010	1	48.89 kbps
3	000011	1	73.3 kbps
4	000100	1	100 kbps
5	000101	1	35.56 kbps
6	000110	1	71.11 kbps
7	000111	1	124.4 kbps
8	001000	1	266.6 kbps
16	010000	2	1.25 mbps
17	010001	2	2 mbps
18	010010	2	2.5 mbps
19	010011	2	4 mbps
20	010100	2	5 mbps
21	010101	2	6 mbps
22	010110	2	9.6 mbps
23	010111	2	12 mbps
24	011000	2	19.2 mbps
25	011001	2	24 mbps
26	011010	2	38.4 mbps
27	011011	2	48 mbps
28	011100	2	76.8 mbps
29	011101	2	96 mbps
32	100000	3	12 mbps
33	100001	3	18 mbps
34	100010	3	24 mbps
35	100011	3	36 mbps
36	100100	3	48 mbps
37	100101	3	72 mbps
38	100110	3	96 mbps
others		Reserved	

서식 있음: 표준, 가운데, 간격 단락 뒤: 0 pt

서식 있음: 글꼴: 12 pt, 굵게 없음

서식 있음: 글꼴: 굵게

서식 있음: SC4008, 글꼴: (한글) 맑은 고딕, 12 pt, 굵게 없음, 글꼴 색: 자동

서식 있음: 글꼴: (한글) 맑은 고딕, 굵게, (한글) 한국어

서식 있음: 기본 단락 글꼴, 글꼴: (한글) +본문 한글, 굵게 없음

서식 있음: 표준, 간격 단락 뒤: 0 pt

서식 있음: SC4008, 글꼴: (한글) 맑은 고딕, 12 pt, 굵게 없음, 글꼴 색: 자동

서식 있음: SC4008, 글꼴: (한글) 맑은 고딕, 12 pt, 굵게 없음, 글꼴 색: 자동

삭제됨: .

6.4.1.3 Frame length field
The frame length field is 7 bits in length and specifies the total number of octets contained in the PSDU (i.e. PSDU). It is a value between 0 and *aMaxPHYPacketSize* as shown in 6.5. Table 22 summarizes the type of payload versus the frame length value.

Table 22—Fra

Frame length values
0-4
5
6-7
8 to aMaxPHYPacketSize

6.4.1.4 PSDU field
The PSDU field has a variable length and carries the data of the PHY packet.

서식 있음: 글꼴: 굵게 없음

삭제됨: 5

서식 있음: SP196992, 양쪽, 간격 앞: 12 pt, 단락 뒤: 12 pt

삭제됨: The CRC calculation used for the header is CCITT CRC-16 as per subclause 6.4.1.6. The combination of the PHY header and the MAC header shall be protected with a 2 oc... [2]

서식 있음: 위 첨자

서식 있음: 위 첨자

서식 있음: 위 첨자

서식 있음: 기본 단락 글꼴, 글꼴: (한글) 맑은 고딕

6.4.1.3.4 Length of PSDU

The PSDU length field is 16 bits in length and specifies the total number of octets contained in the PSDU (i.e. PSDU). It is a value between 0 and *aMaxPHYPacketSize* as shown in 6.5.1

6.4.1.3.5 Reserved fields

6.4.1.3.6 HCS

The PHY header shall be protected with a 2 octet CRC-16 header check sequence (HCS). A schematic of the CRC processing is shown in annex J. The HCS bits shall be processed in the transmit order. The registers shall be initialized to all ones.

6.4.1.3.7 Channel estimation sequence

The channel estimation sequence is optional and is used in PHY Type 3. The information about PHY type 3 is obtained after decoding the PHY header. The length of channel estimation sequence is 8 bit. Refer to 6.8.6.1 CSK Calibration for more detailed information.

6.4.1.5 PSDU field

The PSDU field has a variable length and carries the data of the PHY packet.

삭제됨: 6.4.2 PHY header
The header, as shown in Table 23, shall be transmitted with an OOK modulation. If there are multiple light sources supported by the device, all light sources shall transmit the same header contents simultaneously. The band plan ID field in this case shall be that of the lowest band plan ID.

PHY header fields	
Burst mode	
Channel number	
Data rate	
Length of MSDU	
Alternate Mode	
Reserved fields	

서식 있음: 왼쪽, 지정한 문자 수와 상관없이 오른쪽 들여쓰기 하지 않음, 간격 앞: 12 pt, 단락 뒤: 12 pt, 단락의 첫 줄이나 마지막 줄 분리 허용, 한글과 영어 간격을 자동으로 조절하지 않음, 한글과 숫자 간격을 자동으로 조절하지 않음

Octets: variable	3			variable	2
Preamble	Frame length (7 bits)	Reserved (1 bit)	HCS (16 bits as defined in 6.4.1.5)	PSDU	Frame Check Sequence (as defined in 6.4.1.6)
SHR	PHR			PSDU	FCS

Figure 21—Format of the PPDU

In the case of CSK, the CSK PPDU of Figure 22 is used after link establishment.

The CRC calculation used for the header is CCITT CRC-16 as per subclause 6.4.1.6. The combination of the PHY header and the MAC header shall be protected with a 2 octet header check sequence (HCS). The HCS shall be the one's complement of the remainder generated by the modulo-2 division of the PHY header by the polynomial: $x^{16}+x^{12}+x^5+1$. The HCS bits shall be processed in the transmit order. All HCS calculations shall be made prior to data scrambling. The registers shall be initialized to all ones.

6.4.1.6 Frame Check Sequence

The frame shall be protected with a CCITT CRC-16 frame check sequence (FCS). The FCS shall be the one's complement of the remainder generated by the modulo-2 division of the protected frame by the polynomial $x^{16}+x^{12}+x^5+1$. The protected bits shall be processed in transmitted order. All FCS calculations shall be made prior to data scrambling. A schematic of the processing is shown in Figure 26.

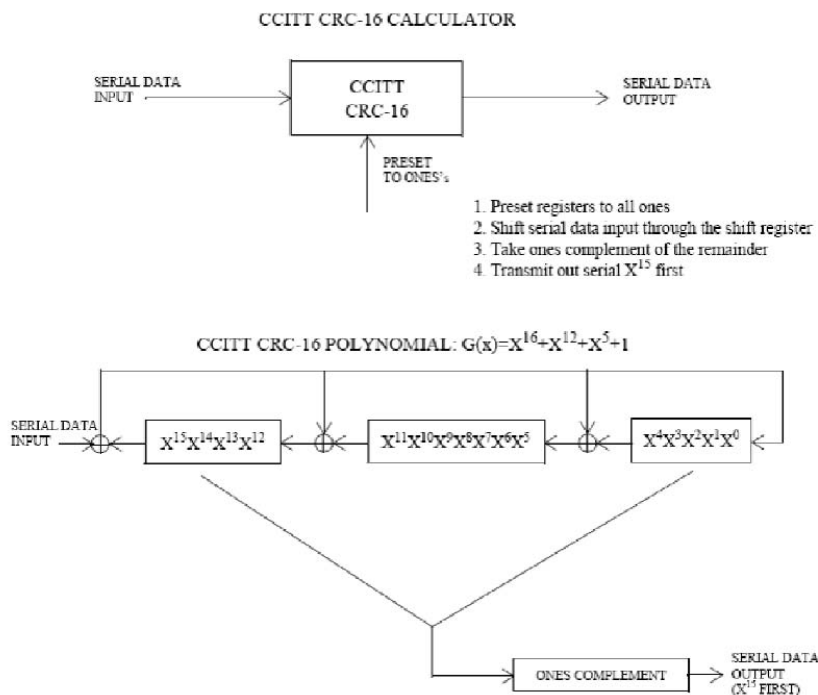


Figure 26—CCITT CRC-16 Implementation

As an example, consider the following 32-bit length sequence to be protected by the CRC-16

0101 0000 0000 0000 0000 0011 0000 0000

b0.....b31

The leftmost bit (b0) is transmitted first in time.

The ones complement for this sequence would be the following:

0101 1011 0101 0111

b0.....b15

The leftmost bit (b0) is transmitted first in time. Bit b0 corresponds to x^{15} in the Figure 26.

An illustrative example of the HCS calculation using the information from Figure 26 is shown in Figure 27.

Data	CRC Registers	
	msb	lsb
	1111111111111111	; Initialize preset to ones
0	1110111111011111	
1	1101111110111110	
0	1010111101011101	
1	0101111010111010	
0	1011110101110100	
0	0110101011001001	
0	1101010110010010	
0	1011101100000101	
0	0110011000101011	
0	1100110001010110	
0	1000100010001101	
0	0000000100111011	
0	0000010011101110	
0	0000010011101100	
0	0000100111011000	
0	0001001110110000	
0	0010011101100000	
0	0100111011000000	
0	1001110110000000	
0	0010101100100001	
0	0101011001000010	
0	1010110010000100	
1	0101100100001000	
1	1010001000110001	
0	0101010001000011	
0	1010100010000110	
0	0100000100101101	
0	1000001001011010	
0	0001010010010101	
0	0010100100101010	
0	0101001001010100	
0	1010010010101000	

Figure 27—Example of CRC calculations