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Wireless Personal Area Networks

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Re	Task Group 15.4g
Abstract	This document is a draft of an amendment for Clause 6, containing the parts of the MR-O-QPSK PHY.
Purpose	Review
Notice	This document has been prepared to assist the IEEE P802.15. It is offered as a basis for discussion and is not binding on the contributing individual(s) or organization(s). The material in this document is subject to change in form and content after further study. The contributor(s) reserve(s) the right to add, amend or withdraw material contained herein.
Release	The contributor acknowledges and accepts that this contribution becomes the property of IEEE and may be made publicly available by P802.15.

6. PHY specification

Insert the following text

In further additions to the PHYs supported in IEEE Std 802.15.4-2006, and IEEE Std 802.15.4a-2007, and IEEE Std 802.15.4c-2009, an additional multi-rate and multi-regional O-QPSK (MR-O-QPSK) PHY has been added, operating in the 780 MHz, 868 MHz, 915 MHz, and 2450 MHz band.

6.1 General requirements and definitions

6.1.1 Operating frequency range

Insert the following four rows in Table 1

Table 1—Frequency bands and data rates

PHY (MHz)	Frequency band (MHz)	Spreading parameters		Data parameters		
		Chip rate (kchip/s)	Modulation	Bit rate (kb/s)	Symbol rate (ksymbol/s)	Symbols
MR-O-QPSK-780	779-787	1000	O-QPSK	31.25 125 250 500		
MR-O-QPSK-868	868-870	125	O-QPSK	15.625 62.5		
MR-O-QPSK-915	902-928	1000	O-QPSK	31.25 62.5 125 250 500		
MR-OQPSK-2450	2400-2483.5	2000	O-QPSK	31.25 62.5 125 250 500		

6.1.2 Channel assignments

6.1.2.1 Channel numbering

Insert the following new subclause after 6.1.2.5:

6.1.2.2 Channel numbering for MR-O-QPSK PHY

6.1.2.2.1 Channel numbering for 779–787 MHz frequency band

For channel page 0, 4 channels numbered 0 to 3 are available across the 779-787 MHz band. The center frequency of these channels is defined as follows:

$$F_c = 780 + 2k \text{ in megahertz, for } k = 0, \ldots, 3$$

where k is the channel number.

6.1.2.2.2 Channel numbering for 868–870 MHz frequency band

For channel page 1, 3 channels numbered 0 to 2 are available across the 868-870 MHz band. The center frequency of these channels is shown in Table 2.

Table 2—Center frequencies for the MR-O-QPSK PHY of the 868-870 MHz band

Channel number	Center Frequency (MHz)
0	868.300
1	868.950
2	869.525

6.1.2.2.3 Channel numbering for 902–928 MHz frequency band

For channel page 2, 10 channels numbered 0 to 9 are available across the 902-928 MHz band. The center frequency of these channels is defined as follows:

$$F_c = 906 + 2k \text{ in megahertz, for } k = 0, \ldots, 9$$

where k is the channel number.

6.1.2.2.4 Channel numbering for 2400–2483.5 MHz frequency band

For channel page 3, 16 channels numbered 0 to 15 are available across the 2400-2483.5 MHz band. The center frequency of these channels is defined as follows:

$$F_c = 2405 + 5k \text{ in megahertz, for } k = 0, \ldots, 15$$

where k is the channel number.

6.1.2.3 Channel pages

6.1.3 Minimum long interframe spacing (LIFS) and short interframe spacing (SIFS) periods

6.1.4 RF power measurement

6.1.5 Transmit power

6.1.6 Out-of-band spurious emission

6.1.7 Receiver sensitivity definitions

6.2 PHY service specifications

6.2.1 PHY data service

6.2.1.1 PD-DATA.request

6.2.1.1.1 Semantics of the service primitive

6.2.1.1.2 Appropriate usage

6.2.1.1.3 Effect on receipt

6.2.1.2 PD-DATA.confirm

6.2.1.2.1 Semantics of the service primitive

6.2.1.2.2 When generated

6.2.1.2.3 Appropriate usage

6.2.1.3 PD-DATA.indication

6.2.1.3.1 Semantics of the service primitive

6.2.1.3.2 When generated

6.2.1.3.3 Appropriate usage

6.2.2 PHY management service

6.2.2.1 PLME-CCA.request

6.2.2.1.1 Semantics of the service primitive

6.2.2.1.2 Appropriate usage

6.2.2.1.3 Effect on receipt

6.2.2.2 PLME-CCA.confirm

6.2.2.2.1 Semantics of the service primitive

6.2.2.2.2 When generated

6.2.2.2.3 Appropriate usage

6.2.2.3 PLME-ED.request

6.2.2.3.1 Semantics of the service primitive

6.2.2.3.2 Appropriate usage

6.2.2.3.3 Effect on receipt

6.2.2.4 PLME-ED.confirm

6.2.2.4.1 Semantics of the service primitive

6.2.2.4.2 When generated

6.2.2.4.3 Appropriate usage

6.2.2.5 PLME-GET.request

6.2.2.5.1 Semantics of the service primitive

6.2.2.5.2 Appropriate usage

6.2.2.5.3 Effect on receipt

6.2.2.6 PLME-GET.confirm

6.2.2.6.1 Semantics of the service primitive

6.2.2.6.2 When generated

6.2.2.6.3 Appropriate usage

6.2.2.7 PLME-SET-TRX-STATE.request

6.2.2.7.1 Semantics of the service primitive

6.2.2.7.2 Appropriate usage

6.2.2.7.3 Effect on receipt

6.2.2.8 PLME-SET-TRX-STATE.confirm

6.2.2.8.1 Semantics of the service primitive

6.2.2.8.2 When generated

6.2.2.8.3 Appropriate usage

6.2.2.9 PLME-SET.request

6.2.2.9.1 Semantics of the service primitive

6.2.2.9.2 Appropriate usage

6.2.2.9.3 Effect on receipt

6.2.2.10 PLME-SET.confirm

6.2.2.10.1 Semantics of the service primitive

6.2.2.10.2 When generated

6.2.2.10.3 Appropriate usage

6.2.3 PHY enumerations description

6.3 PPDU format

Insert the following text and figure:

Figure 15 shows the PPDU format of the MR-O-QPSK PHY.

Octets				
4 / 8 (see 6.3.1)	1	2		4-2047
Preamble	SFD	Frame Control (5 bit)	Frame Length (11 bit)	PSDU (incl. FCS-32)
SHR		PHR		PHY payload

Figure 15—PPDU Format of the MR-O-QPSK PHY

6.3.1 Preamble field

Insert the following text

The Preamble field for the MR-O-QPSK PHY is a sequence of 8 zero octets for the 780 MHz, 915 MHz and 2450 MHz band, and a sequence of 4 zero octets for the 868 MHz band.

6.3.2 SFD field

Insert the following text and table

The SFD field of the MR-O-QPSK PHY shall be an 8-bit sequence selected from the list of Table 3. In addition to boundary synchronisation, the SFD serves as a mode indication mechanism for *SpreadingMode* when operating in the 915 MHz or 2450 MHz band.

Table 3—Format of the SFD field for the MR-O-QPSK PHY

SFD value Bits(0:7)	Indicates
1 1 1 0 0 1 0 1	*SpreadingMode* is "DSSS" during PSDU
0 0 0 1 1 0 1 0	*SpreadingMode* is "M-DSSS" during PSDU for the 915 MHz and 2450 MHz band.
	Not supported for the 780 MHz and 868 MHz band.

The transmission sequence starts with LSB in the left to MSB in the right.

Insert the following new subclauses after 6.3.2:

6.3.2a Control field

The Control field of the MR-O-QPSK PHY is 5 bits in length and is shown in Figure 16.

Bits(0:4)		
2	**2**	**1**
Parity Check	*RateMode*	reserved

Figure 16—Format of the Control field

6.3.2a.1 Parity check field

Two parity bits as a function of the Rate Mode field, the Reserved field and the Frame Length field shall be transmitted.

Let $(p_0, p_1, \ldots, p_{15})$ be the bits of the PHR field, where p_0 refers to the least significant bit (transmittet first in time) and p_{15} refers to the most significant bit (transmittet last in time). The parity check entries at positions p_0 and p_1 shall satisfy the constraints:

$$p_0 \oplus p_2 \oplus p_3 \oplus p_4 \oplus p_5 \oplus p_6 \oplus p_7 \oplus p_8 = 0 \quad (1)$$

and

$$p_1 \oplus p_9 \oplus p_{10} \oplus p_{11} \oplus p_{12} \oplus p_{13} \oplus p_{14} \oplus p_{15} = 0 \quad (2)$$

for all combinations of $(p_2, p_3, \ldots, p_{15})$, where addition is modulo-2 addition (addition over GF(2)).

6.3.2a.2 Rate Mode field

The MR-O-QPSK PHY supports up to four different PSDU rate modes within each frequency band. Table 4 shows the mapping of the bit values to the variable *RateMode*.

Table 4—Rate mode mapping of the MR-O-QPSK PHY

Bits(0:1)	*RateMode*
00	0
10	1
01	2
11	3

6.3.2a.3 Reserved field

The reserved subfield is for future usage and should be set to "0" if not used.

6.3.3 Frame Length field

Insert the following new paragraph after the first paragraph of 6.3.3:

For the MR-O-QPSK PHY, the Frame Length field is 11 bits in length and specifies the total number of octets contained in the PSDU (i.e., PHY payload). It is a value between 4 and *aMaxSUNPacketSize* octets (see 6.4).

Insert the following new row at the end of Table 29:

Table 5—Frame length values

Frame length values	Payload
4 to *aMaxSUNPacketSize*	MPDU

6.3.4 PSDU field

6.4 PHY constants and PIB attributes

6.4.1 PHY constants

Insert the following new row at the end of Table 30:

Table 6—PHY constants

Constant	Description	Value
aMaxSUNPacketSize	The maximum PSDU size (in octets) any of the SUN PHYs shall be able to receive.	2047
aSUNTurnaroundTime	RX-to-TX or TX-to-RX maximum turnaround time (in milliseconds) (see 6.13.1 and 6.13.2).	1

6.4.2 PHY PIB attributes

Table 7—PHY PIB attributes

Attribute	Identifier	Type	Range	Description

6.5 2450 MHz PHY specifications

6.6 2450 MHz PHY chirp spread spectrum (CSS) PHY

6.7 868/915/950 MHz band binary phase-shift keying (BPSK) PHY specifications

6.8 780 MHz band (optional) O-QPSK PHY specifications

6.9 868/915 MHz band (optional) amplitude shift keying (ASK) PHY specifications

6.10 868/915 MHz band (optional) O-QPSK PHY specifications

6.11 950 MHz band Gaussian frequency-shift keying (GFSK) PHY specifications

6.12 UWB PHY specification

Insert after 6.12.15.3 the following new subclauses (6.12a through 6.12c.x.x):

6.12a SUN FSK

<editor's note: we need to come up with an appropriate name for this PHY>

6.12a.1 Data rates

6.12a.2 Data transfer

6.12a.3 Modulation and coding

6.12a.3.1 Reference modulator diagram

6.12a.3.2 Bit-to-symbol mapping

6.12a.3.3 Modulation parameters

6.12a.3.4 Forward error correction (FEC)

6.12a.3.5 Pulse shape

6.12a.4 Radio specification

<editor's note: The term "radio specification" is consistent with the subclause names in other PHYs.>

6.12b SUN OFDM

<editor's note: we need to come up with an appropriate name for this PHY>

6.12b.1 Data rates

6.12b.2 Data transfer

6.12b.3 Modulation and coding

6.12b.3.1 Reference modulator diagram

6.12b.3.2 Bit-to-symbol mapping

6.12b.3.3 Modulation parameters

6.12b.3.4 Forward error correction (FEC)

6.12b.3.5 Pulse shape

6.12b.4 Radio specification

<editor's note: The term "radio specification" is consistent with the subclause names in other PHYs.>

6.12c MR-O-QPSK PHY specifications

The MR-O-QPSK PHY is a multi-regional and multi-rate PHY supporting the following independent bands of operation:

— the Chinese frequency band 779-787 MHz

— the European frequency band 868-870 MHz

— the ISM band 902-928 MHz

— the ISM band 2400-2483.5 MHz.

The MR-O-QPSK PHY supports multiple PSDU data rates within each frequency band, employing a concatenation of outer forward error correction coding (FEC), interleaving and spreading. For all frequency bands, spreading is supported by *direct sequence spread spectrum* (DSSS) applying various spreading factors. For the frequency bands 915 MHz and 2450 MHz, this PHY supports a co-alternative spreading mode during the PSDU part, called *multiplexed direct sequence spread spectrum* (M-DSSS). For the frequency bands 915 MHz and 2450 MHz, a compliant device shall support at least one of the spreading modes. The selection of *SpreadingMode* (either "DSSS" or "M-DSSS") is obtained by a dedicated SFD value of the SHR, (see 6.3.2).

During SHR and PHR, no FEC is applied but the spreading factor is considerably larger than the spreading factor during the PSDU part.

For the frequency bands 780 MHz, 915 MHz and 2450 MHz, this PHY supports communication with legacy devices according to the specification of sections 6.8, 6.10 and 6.5, respectively, as described in subclause 6.12c.5.

Modulation is raised cosine shaped quadrature phase-shift keying (O-QPSK).

6.12c.1 SHR and PHR spreading

For the (SHR,PHR) part of the PPDU, (N,1)-DSSS in conjunction with differential encoding shall be applied independent of the spreading method during the PSDU part (*SpreadingMode* is either "DSSS" or "M-DSSS").

Table 8 shows the spreading parameters of (N,1)-DSSS bit-to-symbol mapping as described in 6.12c.4.4.

6.12c.2 PSDU data rates for DSSS

The supported PSDU parameters for *SpreadingMode* "DSSS" are shown in Table 9.

6.12c.3 PSDU data rates for M-DSSS

The supported PSDU parameters for *SpreadingMode* "M-DSSS" are shown in Table 10.

Table 8—SHR,PHR parameters

Frequency band (MHz)	Chip Rate (kchip/s)	Differential Encoding	Spreading	(SHR,PHR) duration [us]
779-787	1000	yes	(64,1)-DSSS	5632
868-870	125	yes	$(16,1)_0$-DSSS	7168
902-928	1000	yes	(64,1)-DSSS	5632
2400-2483.5	2000	yes	(128,1)-DSSS	5632

Table 9—PSDU parameters for *SpreadingMode* "DSSS"

Frequency band (MHz)	Chip rate (kchip/s)	Rate-Mode	Differential Encoding	Spreading	1/2 rate-FEC + inter-leaving	data rate (kbps)
779-787	1000	0	yes	$(16,1)_{0/1}$-DSSS	yes	31.25
		1	no	(16,4)-DSSS	yes	125
		2	no	(8,4)-DSSS	yes	250
		3	no	none	yes	500
868-870	125	0	yes	(4,1)-DSSS	yes	15.625
		1	no	none	yes	62.5
		2/3	not supported			
902-928	1000	0	yes	$(16,1)_{0/1}$-DSSS	yes	31.25
		1	no	(16,4)-DSSS	yes	125
		2	no	(8,4)-DSSS	yes	250
		3	no	none	yes	500
2400-2483.5	2000	0	yes	$(32,1)_{0/1}$-DSSS	yes	31.25
		1	no	(32,4)-DSSS	yes	125
		2	no	(16,4)-DSSS	yes	250
		3	no	(8,4)-DSSS	yes	500

6.12c.4 Modulation and coding

During the PSDU part, the MR-O-QPSK PHY shall employ forward error correction coding (FEC) and spreading of variable spreading factors. The spreading method is either "DSSS" (for all frequency bands) or co-alternatively, "M-DSSS" (for the 915 MHz and 2450 MHz frequency band).

6.12c.4.1 Reference modulator diagram for DSSS.

Figure 17 shows the reference modulator diagram when DSSS is applied during the PSDU.

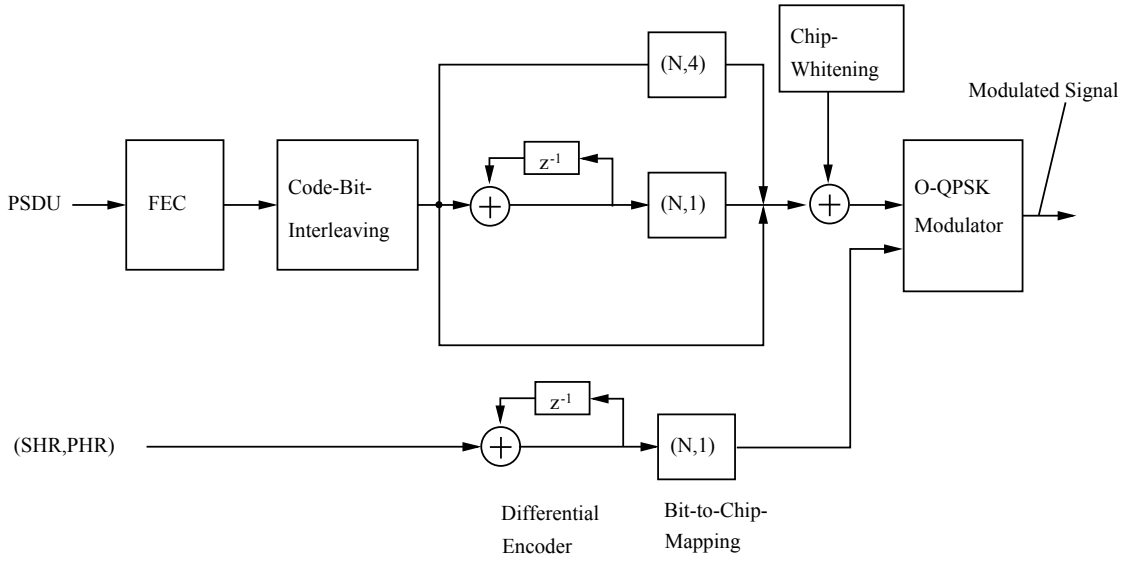

Figure 17—Coding, interleaving, DSSS and modulation

Table 10—PSDU parameters for *SpreadingMode* "M-DSSS"

Frequency band (MHz)	Chip rate (kchip/s)	Rate-Mode	Differential Encoding	Spreading	1/2 rate-FEC + inter-leaving	data rate (kbps)
779-787	not supported					
868-870						
902-928	1000	0	no	(64,8)-M-DSSS	yes	62.5
		1	no	(32,8)-M-DSSS	yes	125
		2	no	(32,8)-M-DSSS	no	250
		3	no	(16,8)-M-DSSS	no	500
2400-2483.5	2000	0	no	(128,8)-M-DSSS	yes	62.5
		1	no	(64,8)-M-DSSS	yes	125
		2	no	(64,8)-M-DSSS	no	250
		3	no	(32,8)-M-DSSS	no	500

Each bit in the (SHR,PHR) shall be processed in octet-wise order, beginning with the Preamble field and ending with the last octet of the PHR. Within each octet, the LSB, b_0, is processed first and the MSB, b_7, is processed last. The bits of the SHR and PHR shall be differentially encoded (see 6.12c.4.3) and in addition (*N*,1)-DSSS bit-to-chip mapping shall be applied as described in 6.12c.4.4.

Each bit in the PSDU shall be processed in octet-wise order, beginning with the first octet and ending with the last octet of the PSDU. Within each octet, the LSB, b_0, is processed first and the MSB, b_7, is processed last. The bits of the PSDU shall be first processed by forward error correction coding (FEC) as described in 6.12c.4.8, delivering a sequence of code-bits. The code-bits shall be interleaved as described in 6.12c.4.9. Depending on the frequency band and *RateMode*, spreading by DSSS shall be applied.

The first DSSS method applies differentially encoding of the interleaved code-bits (see 6.12c.4.3) and subsequently (*N*,1)-bit-to-chip mapping as described in 6.12c.4.4.

The second DSSS method applies (*N*,4)-bit-to-chip mapping of the interleaved code-bits as described in 6.12c.4.4.

Depending on the frequency band and *RateMode*, the output sequences of the bit-to-chip mapper shall be whitened, as shown in subclause 6.12c.4.6.

The chip sequences are modulated onto the carrier using O-QPSK modulation as described in 6.12c.4.7.

6.12c.4.2 Reference modulator diagram for M-DSSS

Figure 18 shows the reference modulator diagram when M-DSSS is applied during the PSDU.

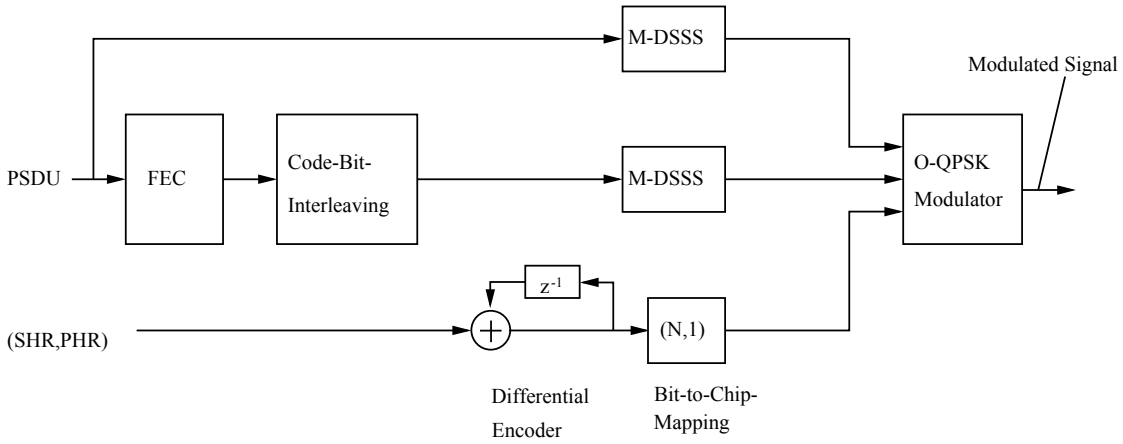

Figure 18—Coding, interleaving, M-DSSS and modulation

Each bit in the (SHR,PHR) shall be processed in octet-wise order, beginning with the Preamble field and ending with the last octet of the PHR. Within each octet, the LSB, b_0, is processed first and the MSB, b_7, is processed last. The bits of the SHR and PHR shall be differentially encoded (see 6.12c.4.3) and in addition (*N*,1)-DSSS bit-to-chip mapping shall be applied as described in 6.12c.4.4.

Each bit in the PSDU shall be processed in octet-wise order, beginning with the first octet and ending with the last octet of the PSDU. Within each octet, the LSB, b_0, is processed first and the MSB, b_7, is processed last.

Depending on *RateMode,* (see Table 10)*,* the bits of the PSDU shall be first processed by forward error correction coding (FEC) as described in 6.12c.4.8, delivering a sequence of code-bits. When FEC is employed, the code-bits shall be interleaved as described in 6.12c.4.9, otherwise the interleaver is bypassed.

Depending on *RateMode*, M-DSSS of different spreading factors shall be applied*,* see Table 10 and subclause 6.12c.4.5.

The chip sequences are modulated onto the carrier using O-QPSK modulation as described in 6.12c.4.7.

6.12c.4.3 Differential encoding

Differential encoding is the modulo-2 addition (addition over GF(2)) of a raw bit with the previous encoded bit. This is performed by the transmitter and can be described by Equation (3):

$$E_n = R_n \oplus E_{n-1} \tag{3}$$

where

R_n is the raw bit being encoded

E_n is the corresponding differentially encoded bit

E_{n-1} is the previous differentially encoded bit

For each packet transmitted, R_0 is the first raw data bit to be encoded and E_{-1} is assumed to be zero.

If differential encoding is enabled during the PSDU part depending on the frequency band and *RateMode* (see Table 9), it shall be continuously applied to the bits of the SHR, PHR and to the sequence of cod-bits at the output of the interleaver, see subclauses 6.12c.4.8 and 6.12c.4.9.

If differential encoding is not enabled during the PSDU part depending on the frequency band and *RateMode* (see Table 9), it shall be applied to the bits of the SHR and PHR only.

6.12c.4.4 DSSS bit-to-chip mapping

For (N,1)-DSSS, a single bit is mapped to a sequences of N binary valued chips: $\{0, 1\}^1 \rightarrow \{0, 1\}^N$. The number N of chips depends on the frequency band and *RateMode*, see Table 9. This mapping defines a binary (N, k) block code with $k = 1$.

Table 11 to Table 15 show (N,1)-DSSS used in the MR-O-QPSK PHY. For $N = 1$, the chip value is equal to the input bit value (no spreading).

Table 11—(4,1)-DSSS bit-to-chip mapping

Input bit	Chip values (c_0 c_1 … c_3)
0	1010
1	0101

Table 12—$(16,1)_k$-DSSS bit-to-chip mapping

k	Input bit	Chip values (c_0 c_1 … c_{15})
0	0	0010_0011_1101_0110
	1	1101_1100_0010_1001
1	0	0100_0111_1010_1100
	1	1011_1000_0101_0011

Table 13—$(32,1)_k$-DSSS bit-to-chip mapping

k	Input bit	Chip values (c_0 c_1 … c_{31})
0	0	1101_1110_1010_0010_0111_0000_0110_0101
	1	0010_0001_0101_1101_1000_1111_1001_1010
1	0	1110_1111_0101_0001_0011_1000_0011_0010
	1	0001_0000_1010_1110_1100_0111_1100_1101

Table 14—(64,1)-DSSS bit-to-chip mapping

Input bit	Chip values (c_0 c_1 … c_{63})
0	1011_0010_0010_0101_1011_0001_1101_0000_ _1101_0111_0011_1101_1111_0000_0010_1010
1	0100_1101_1101_1010_0100_1110_0010_1111_ _0010_1000_1100_0010_0000_1111_1101_0101

Table 15—(128,1)-DSSS bit-to-chip mapping

Input bit	Chip values (c_0 c_1 … c_{127})
0	1001_1000_1000_1011_0100_1110_0100_0010_ _0101_0010_0110_1101_1100_0111_1010_0000_ _1101_0100_0110_0101_1101_1000_0111_0101_ _1110_0111_1101_1111_1000_0000_1010_1011
1	0110_0111_0111_0100_1011_0001_1011_1101_ _1010_1101_1001_0010_0011_1000_0101_1111_ _0010_1011_1001_1010_0010_0111_1000_1010_ _0001_1000_0010_0000_0111_1111_0101_0100

Note that for $N > 1$, $(N,1)$-DSSS is always preceded by differential encoding, supporting non-coherent detection of the interleaved code-bits, see Table 8 and Table 9. For $N = 1$ (no spreading), coherent detection is required, employing a phase control loop based on the received chip samples.

For $N = 16$, two spreading codes are defined, denoted as $(16,1)_0$-DSSS and $(16,1)_1$-DSSS, respectively. Similarly, for $N = 32$, two spreading codes are defined, denoted as denoted as $(32,1)_0$-DSSS and $(32,1)_1$-DSSS, respectively. When used during the (SHR,PHR), only $(16,1)_0$-DSSS is applied, see Table 8. When used during the PSDU, the two spreading codes are alternatingly applied, denoted as $(16,1)_{0/1}$-DSSS, see Table 9. Similarly, for $N = 32$, the two alternating spreading codes are denoted as $(32,1)_{0/1}$-DSSS, see Table 9. The time variance of the spreading code during the PSDU part improves spectral properites while preserving a robust and simple mechanism for carrier sense[6]. In particular, let $E_n = R_n \oplus E_{n-1}$ be the bit

value at the output of the differential encoder (see Equation (3)) where R_n refers to the first code-bit at the output of the interleaver. For $k = 0, 1, \ldots$, the bits E_{n+2k} shall be spread with $(N,1)_0$-DSSS and the bits E_{n+2k+1} shall be spread with $(N,1)_1$-DSSS.

In order to exploit the capabilities of a trellis-based decoder for the outer forward error correction code (see 6.12a.3.4), it is recommended to compute a soft decision value of the detected information bits.

When applying (N,4)-DSSS, a 4-tuple of bits is mapped to a sequence of N binary valued chips: $\{0, 1\}^4 \rightarrow \{0, 1\}^N$. This mapping defines a binary (N, k) block code with $k = 4$.

Table 16 to Table 18 show (N,4)-DSSS supported by the MR-O-QPSK PHY.

Table 16—(8,4)-DSSS bit-to-chip mapping

Input bits (b_0 b_1 b_2b_3)	Chip values (c_0 c_1 … c_7)
0000	0000_0001
1000	1101_0000
0100	0110_1000
1100	1011_1001
0010	1110_0101
1010	0011_0100
0110	1000_1100
1110	0101_1101
0001	1010_0010
1001	0111_0011
0101	1100_1011
1101	0001_1010
0011	0100_0110
1011	1001_0111
0111	0010_1111
1111	1111_1110

For (N,4)-DSSS, coherent detection is recommended, employing a phase control loop based on the maximum likelihood decision of the optimal codeword with respect to the (N,4) block code. In order to exploit the capabilities of a trellis-based decoder for the outer forward error correction code (see 6.12a.3.4), it is recommended to compute a soft decision value of each individual bit of the 4-tuple of information bits[7].

[6]When applying chip whitening according to subclause 6.12c.4.6, the spectral properties can be improved as well but carrier sense is difficult to achieve. Since the signal-to-noise ratio (SNR) is low for modes applying (16,1)-DSSS or (32,1)-DSSS, a mechanism for carrier sense is beneficial for clear channel assessment (CCA). For the modes where chip whitening is applied (see 6.12c.4.6), the SNR is larger implying that CCA based on energy-detect may suffice.

[7]Since a binary (N,4) block code consists of 16 codewords only, even a brute force estimate of the a posteriori probability (or some equivalent metric) of each information bit is feasible at low implementation cost.

Table 17—(16,4)-DSSS bit-to-chip mapping

Input bits (b_0 b_1 b_2b_3)	Chip values (c_0 c_1 … c_{15})
0000	0011_1110_0010_0101
1000	0100_1111_1000_1001
0100	0101_0011_1110_0010
1100	1001_0100_1111_1000
0010	0010_0101_0011_1110
1010	1000_1001_0100_1111
0110	1110_0010_0101_0011
1110	1111_1000_1001_0100
0001	0110_1011_0111_0000
1001	0001_1010_1101_1100
0101	0000_0110_1011_0111
1101	1100_0001_1010_1101
0011	0111_0000_0110_1011
1011	1101_1100_0001_1010
0111	1011_0111_0000_0110
1111	1010_1101_1100_0001

Table 18—(32,4)-DSSS bit-to-chip mapping

Input bits (b_0 b_1 b_2b_3)	Chip values (c_0 c_1 … c_{31})
0000	1101_1001_1100_0011_0101_0010_0010_1110
1000	1110_1101_1001_1100_0011_0101_0010_0010
0100	0010_1110_1101_1001_1100_0011_0101_0010
1100	0010_0010_1110_1101_1001_1100_0011_0101
0010	0101_0010_0010_1110_1101_1001_1100_0011
1010	0011_0101_0010_0010_1110_1101_1001_1100

Table 18—(32,4)-DSSS bit-to-chip mapping

0110	1100_0011_0101_0010_0010_1110_1101_1001
1110	1001_1100_0011_0101_0010_0010_1110_1101
0001	1000_1100_1001_0110_0000_0111_0111_1011
1001	1011_1000_1100_1001_0110_0000_0111_0111
0101	0111_1011_1000_1100_1001_0110_0000_0111
1101	0111_0111_1011_1000_1100_1001_0110_0000
0011	0000_0111_0111_1011_1000_1100_1001_0110
1011	0110_0000_0111_0111_1011_1000_1100_1001
0111	1001_0110_0000_0111_0111_1011_1000_1100
1111	1100_1001_0110_0000_0111_0111_1011_1000

For each codeword $(c_0, \ldots, c_{N-1})$, the first component, c_0, shall be transmitted first in time, and the last component, c_{N-1}, shall be transmitted last in time.

6.12c.4.5 M-DSSS bit-to-chip mapping

The functional block diagram in Figure 19 is provided as a reference for specifying the Multiplexed Direct Sequence Spread Spectrum (M-DSSS). Each bit in the PSDU shall be processed through the Turbo Product Code (TPC) encoding and multiplexing module. As for the horizontal code of TPC, 3 bits are encoded into *n* bits with the (*n*, 3) Hadamard code. The (4, 3) odd parity code is employed as the vertical code of TPC.

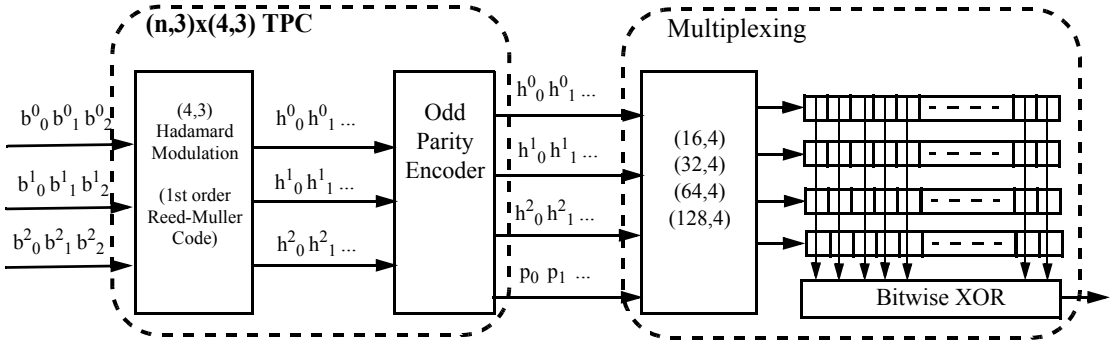

Figure 19—M-DSSS signal flow

Each octet of the PSDU shall be mapped into three horizontal input rows as specified in Table 19. The 3 LSBs (b_0, b_1, b_2) of each octet shall map into the 1st horizontal input row (b^0_0, b^0_1, b^0_2), and the next 3 bits (b_3, b_4, b_5) of each octet shall map into the 2nd horizontal input row (b^1_0, b^1_1, b^1_2). The last horizontal input row (b^2_0, b^2_1, b^2_2) shall be mapped with the last 2 bits (b_6, b_7) of each octet and the single parity bit of the octet provided with Equation (4).

$$p = b^0_0 \oplus b^1_0 \oplus b^2_0 \oplus b^0_1 \oplus b^1_1 \oplus b^2_1 \oplus b^0_2 \oplus b^1_2 \quad (4)$$

.

Table 19—PSDU bit stream to horizontal code input mapping

Horizontal code input	$b^0{}_0$	$b^0{}_1$	$b^0{}_2$	$b^1{}_0$	$b^1{}_1$	$b^1{}_2$	$b^2{}_0$	$b^2{}_1$	$b^2{}_2$
PSDU bit stream	Bits:0	1	2	3	4	5	6	7	*p*

For the horizontal coding of TPC, the three parallel 3-bit streams ($b^x{}_0$, $b^x{}_1$, $b^x{}_2$: x=0, 1, 2) are converted to the three parallel *n*-bit streams ($h^x{}_0$, $h^x{}_1$, $h^x{}_2$, $h^x{}_3$, ..., $h^x{}_{n-1}$) through the (*n*, 3) Hadamard modulator. A (*n*, 3) Hadamard modulation code set of the eight codewords is obtained from the first four rows of ((*n*/2) x (*n*/2)) Hadamard matrix by augmenting it with the negative of each signal. The first four rows of (*n* x *n*) Hadamard matrix are equivalent to that of (*n* / 4) times repeated (4 x 4) Hadamard matrix. The (4x4) Hadamard matrix, H_2, is described by Equation (5). So, the (*n*, 3) Hadamard modulation codes are equivalent to that of *n*/4 times repeated (4, 3) codes described Table 20.

$$H_2 = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \tag{5}$$

.

Table 20—Symbol-to-chip mapping for (4,3) Hadamard modulation

Data symbol (decimal)	**Data symbol ($b^x{}_0$, $b^x{}_1$, $b^x{}_2$)**	**Modulator output ($h^x{}_0$, $h^x{}_1$, $h^x{}_2$, $h^x{}_3$)**
0	0 0 0	1 1 1 1
1	0 0 1	1 -1 1 -1
2	0 1 0	-1 -1 1 1
3	0 1 1	-1 1 1 -1
4	1 0 0	1 -1 -1 1
5	1 0 1	1 1 -1 -1
6	1 1 0	-1 1 -1 1
7	1 1 1	-1 -1 -1 -1

As the minimum Hamming distance of (*n* x *n*) Hadamard matrix is (*n*/2), the minimum distance of (16,3), (32,3), (64,3), and (128,3) Hadamard modulation codes is 8, 16, 32, and 64, respectively.

For the vertical coding of TPC, the odd parity encoder converts the three parallel 4-bit streams to four parallel 4-bit streams as specified in Equation (6), where the odd parity bit is specified in Equation (7).

$$T_{unit} = \begin{bmatrix} h^0{}_0 & h^0{}_1 & h^0{}_2 & h^0{}_3 \\ h^1{}_0 & h^1{}_1 & h^1{}_2 & h^1{}_3 \\ h^2{}_0 & h^2{}_1 & h^2{}_2 & h^2{}_3 \\ p_0 & p_1 & p_2 & p_3 \end{bmatrix} \tag{6}$$

$$\begin{aligned} p_0 &= h^0{}_0 \oplus h^1{}_0 \oplus h^2{}_0 \\ p_1 &= h^0{}_1 \oplus h^1{}_1 \oplus h^2{}_1 \\ p_2 &= h^0{}_2 \oplus h^1{}_2 \oplus h^2{}_2 \\ p_3 &= h^0{}_3 \oplus h^1{}_3 \oplus h^2{}_3 \end{aligned} \tag{7}$$

As a result of (4,3) horizontal and (4,3) vertical coding with a parity bit per byte, the PSDU bit stream is transformed into a (4,3)x(4,3) TPC code block, forming (4x4) 2-dimensional data, as shown in Figure 20.

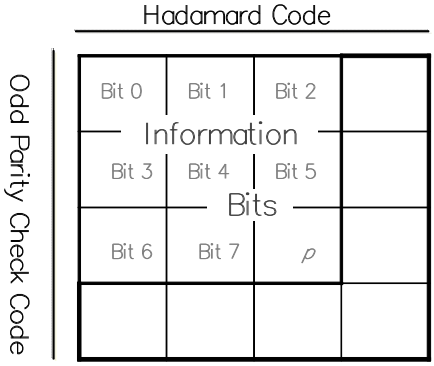

Figure 20—Structure of turbo product codeword

The TPC encoded (4x4) bit matrix, T_{unit}, is the unit matrix for (16,8), (32,8), (64,8), and (128,8) M-DSSS of Table 10. The (16,3) Hadamard modulation output for (16, 8) M-DSSS is specified in Equation (8). Similarly, the (32,3), (64,3), and (128,3) Hadamard modulation output for (32, 8), (64,8), and (128,8) M-DSSS are specified in Equation (9), Equation (10), and Equation (11), respectively.

$$T_{(4\times 16)} = \underbrace{\begin{bmatrix} T_{unit} & T_{unit} & T_{unit} & T_{unit} \end{bmatrix}}_{4} \tag{8}$$

$$T_{(4\times 32)} = \underbrace{\left[T_{unit}\ T_{unit}\ T_{unit}\ T_{unit}\ T_{unit}\ T_{unit}\ T_{unit}\ T_{unit}\right]}_{8} \tag{9}$$

$$T_{(4\times 64)} = \underbrace{\left[T_{unit}\ T_{unit}\ T_{unit}\ \cdots\ T_{unit}\ T_{unit}\ T_{unit}\right]}_{16} \tag{10}$$

$$T_{(4\times 128)} = \underbrace{\left[T_{unit}\ T_{unit}\ T_{unit}\ \cdots\ T_{unit}\ T_{unit}\ T_{unit}\right]}_{32} \tag{11}$$

The TPC encoded output shall be transformed to the chip sequence by multiplexing four parallel bit streams vertically. As for the multiplexing code for (*n,* 3) M-DSSS, H_2 matrix is expanded by adding the each row ($\log_2 n$)-times. To multiplex (4x16) TPC encoded output into (1x16) M-DSSS chip sequence, (4x16) multiplexing code, $H_{m(4\text{x}16)}$ of Equation (12), is bitwise XOR-ed as specified in Equation (13).

$$H_{m(4\times 16)} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & 1 & 1 & 1 & 1 \end{bmatrix} \tag{12}$$

$$X = T_{(4\times 16)} \oplus H_{m(4\times 16)}$$

$$= \begin{bmatrix} h^0_0 & h^0_1 & h^0_2 & h^0_3 & h^0_0 & h^0_1 & h^0_2 & h^0_3 & h^0_0 & h^0_1 & h^0_2 & h^0_3 & h^0_0 & h^0_1 & h^0_2 & h^0_3 \\ h^1_0 & h^1_1 & h^1_2 & h^1_3 & -h^1_0 & -h^1_1 & -h^1_2 & -h^1_3 & h^1_0 & h^1_1 & h^1_2 & h^1_3 & -h^1_0 & -h^1_1 & -h^1_2 & -h^1_3 \\ h^2_0 & h^2_1 & h^2_2 & h^2_3 & h^2_0 & h^2_1 & h^2_2 & h^2_3 & -h^2_0 & -h^2_1 & -h^2_2 & -h^2_3 & -h^2_0 & -h^2_1 & -h^2_2 & -h^2_3 \\ p_0 & p_1 & p_2 & p_3 & -p_0 & -p_1 & -p_2 & -p_3 & -p_0 & -p_1 & -p_2 & -p_3 & p_0 & p_1 & p_2 & p_3 \end{bmatrix} \tag{13}$$

Similarly, The TPC encoded (4x32), (4x64), and (4x128) bit matrix shall be multiplexed into the (1,32), (1,64), and (1,128) output chip sequence with the (4x32), (4x64), and (4x128) multiplexing code as specified in Equation (14).

$$X = T \oplus H_m$$

$$= \begin{cases} \left[T_{(4\times 16)} \oplus H_{m(4\times 16)}\right] & ,n = 16 \\ \left[T_{(4\times 16)} \oplus H_{m(4\times 16)}\ T_{(4\times 16)} \oplus H_{m(4\times 16)}\right] & ,n = 32 \\ \left[T_{(4\times 16)} \oplus H_{m(4\times 16)}\ T_{(4\times 16)} \oplus H_{m(4\times 16)}\ T_{(4\times 16)} \oplus H_{m(4\times 16)}\right] & ,n = 64 \\ \left[T_{(4\times 16)} \oplus H_{m(4\times 16)}\ T_{(4\times 16)} \oplus H_{m(4\times 16)}\ T_{(4\times 16)} \oplus H_{m(4\times 16)}\ T_{(4\times 16)} \oplus H_{m(4\times 16)}\right] & ,n = 128 \end{cases} \tag{14}$$

$$= \left[\bar{c}_0\ \bar{c}_1\ \bar{c}_2\ \bar{c}_3\ \bar{c}_4\ \ \cdots\ \ \bar{c}_{i+j}\right] \quad ,(0 \le i \le 31,\quad 0 \le j < (n \div 16))$$

The multiplexed output bit stream shall be bitwise XOR-ed by the covering code for the chip and symbol synchronization. For each of (16,8), (32,8), (64,8), (128,8) M-DSSS, covering code shall be bit 0 of $(16,1)_0$-DSSS, $(32,1)_0$-DSSS, (64,1)-DSSS, (128,1)-DSSS code, which are described in Table 12, Table 13, Table 14, and Table 15, respectively.

Then, the final output chip sequence of length (*n*,8) M-DSSS shall be described in Equation (15).

$$c_{i+j} = \overline{c_i} \oplus m_{i+j}, (0 \le i \le 31, \quad 0 \le j < (n \div 16))$$

where

$$\begin{aligned}
\overline{c_0} &= (h^0{}_0) + (h^1{}_0) + (h^2{}_0) + (p_0) \\
\overline{c_1} &= (h^0{}_1) + (h^1{}_1) + (h^2{}_1) + (p_1) \\
\overline{c_2} &= (h^0{}_2) + (h^1{}_2) + (h^2{}_2) + (p_2) \\
\overline{c_3} &= (h^0{}_3) + (h^1{}_3) + (h^2{}_2) + (p_3) \\
\overline{c_4} &= (h^0{}_0) + (-h^1{}_0) + (h^2{}_0) + (-p_0) \\
\overline{c_5} &= (h^0{}_1) + (-h^1{}_1) + (h^2{}_1) + (-p_1) \\
\overline{c_6} &= (h^0{}_2) + (-h^1{}_2) + (h^2{}_2) + (-p_2) \\
\overline{c_7} &= (h^0{}_3) + (-h^1{}_3) + (h^2{}_2) + (-p_3) \\
\overline{c_8} &= (h^0{}_0) + (h^1{}_0) + (-h^2{}_0) + (-p_0) \\
\overline{c_9} &= (h^0{}_1) + (h^1{}_1) + (-h^2{}_1) + (-p_1) \\
\overline{c_{10}} &= (h^0{}_2) + (h^1{}_2) + (-h^2{}_2) + (-p_2) \\
\overline{c_{11}} &= (h^0{}_3) + (h^1{}_3) + (-h^2{}_2) + (-p_3) \\
\overline{c_{12}} &= (h^0{}_0) + (-h^1{}_0) + (-h^2{}_0) + (p_0) \\
\overline{c_{13}} &= (h^0{}_1) + (-h^1{}_1) + (-h^2{}_1) + (p_1) \\
\overline{c_{14}} &= (h^0{}_2) + (-h^1{}_2) + (-h^2{}_2) + (p_2) \\
\overline{c_{15}} &= (h^0{}_3) + (-h^1{}_3) + (-h^2{}_2) + (p_3)
\end{aligned} \tag{15}$$

6.12c.4.6 Chip whitening

When *SpreadingMode* is “DSSS”, the chip sequences shall be whitened, depending on the frequency band and *RateMode* as shown in Table 21. For all other modes, no chip whitening shall be applied.

Chip whitening is the modulo-2 addition (addition over GF(2)) of a chip of the PSDU part at the output of the bit-to-chip mapper with the value of a cyclic *m*-sequence $S_{(k \bmod (2^m - 1))}$ of length $2^m - 1$ for $m = 9$. This shall be performed by the transmitter and is described by Equation (16):

$$c'_k = c_k \oplus S_{(k \bmod 511)} \tag{16}$$

where

c_k is the raw PSDU chip being whitened

Table 21—Chip Whitening for "DSSS"

Frequency band (MHz)	RateMode
778-780	2,3
868-870	0,1
902-928	2,3
2400-2483.5	3

c'_k is the whitened chip.

Index k starts at 0, referring to the first chip of the PSDU part at the output of the bit-to-chip mapper and is increased by one at every chip interval. Figure 21 shows the whitening process. At $k = 0$, the register shall be initialized with

$$(u_{k-1}, u_{k-1}, \ldots, u_{k-9}) = (1, 0, 0, 0, 0, 0, 0, 0, 0) \tag{17}$$

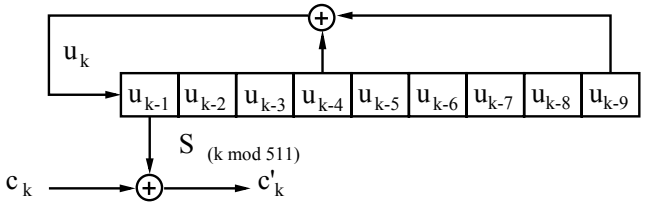

Figure 21—Chip whitening

6.12c.4.7 Modulation parameters for O-QPSK

A chip value shall be mapped into a binary real valued symbol out of {-1,1} by the mapping

$$\zeta(c) = \begin{cases} -1, c = 0 \\ 1, c = 1 \end{cases} \tag{18}$$

The raised cosine pulse shape with roll-off factor of $r = 0.8$ is used to represent each baseband symbol and is described by

$$p(t) = \begin{cases} \dfrac{\sin(\pi t/T_c)}{\pi t/T_c} \times \dfrac{\cos(r\pi t/T_c)}{1 - 4r^2t^2/T_c^2}, t \neq 0 \\ 1, t = 0 \end{cases} \tag{19}$$

where the chip duration T_c is the inverse of the chip rate, see Table 9 and Table 10.

Given the discrete-time sequence $\{c_k\}_0^{N_{PPDU}-1}$ of N_{PPDU} consecutive chip samples, the continuous-time pulse shaped complex baseband signal is given by

$$y_{OQPSK}(t) = \sum_{k=0}^{N_{PPDU}-1} \zeta(c_{2k})p(t-2kT_c) + j\zeta(c_{2k+1})p(t-2kT_c-T_c) \quad (20)$$

with ζ according to Equation (18).

6.12c.4.8 Forward error correction (FEC)

Depending on *RateMode* and *SpreadingMode*, forward error correction coding shall be employed on the PSDU bits, applying 1/2 rate convolutional coding with constraint length K = 7 using the generator polynomials shown in Equation (21) and Equation (22).

$$G_0(x) = 1 + x^2 + x^3 + x^5 + x^6 \quad (21)$$

$$G_1(x) = 1 + x + x^2 + x^3 + x^6 \quad (22)$$

The encoder is shown in Figure 22 where addition is over GF(2).

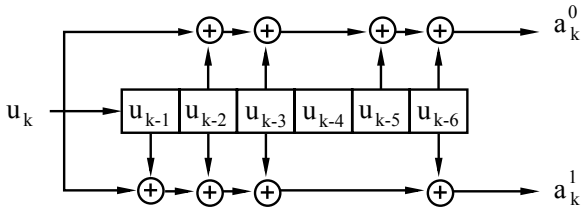

Figure 22—Convolutional encoder

Prior to convolutional encoding, the PSDU shall be extended by appending a termination sequence of 6 zero bits and a sequence of additional bits (pad bits) as shown inFigure 23. The pad bits shall be set to zero and the number of pads bits, N_{PAD}, is computed from the length of the PSDU in octets (LENGTH) as follows:

$$N_B = \text{ceiling}((8 \times \text{LENGTH} + 6)/(N_{\text{INTRLV}}/2)) \quad (23)$$

$$N_D = N_B \times (N_{\text{INTRLV}}/2) \quad (24)$$

$$N_{\text{PAD}} = N_D - (8 \times \text{LENGTH} + 6) \quad (25)$$

The number of code-bits referring to a single interleaving block, N_{INTRLV}, is defined in subclause 6.12c.4.9. The function ceiling (.) is a function that returns the smallest integer value greater than or equal to its argument value.

PSDU	000000	pad bits

Figure 23—PSDU extension prior to encoding

The output sequence of code-bits z shall be generated according to Equation (26):

$$z = \{\ldots\ a_k^0, a_k^1, a_{k+1}^0, a_{k+1}^1, a_{k+2}^0, a_{k+2}^1\ \ldots\} = \{z_0, z_1, \ldots, z_{2N_D-1}\} \quad (26)$$

The first sample, z_0, shall be passed to the interleaver first in time, and the last sample, z_{2N_D-1}, shall be passed to the interleaver last in time.

6.12c.4.9 Code-bit interleaving

Interleaving of code-bits shall be employed in conjunction with FEC in order to improve robustness against burst errors and to break correlation of consecutive bits when applying (N,4) or (N,8) bit-to-chip mapping. No interleaving shall be employed if FEC is not used, see Table 10.

The sequence of code-bits, z, consists of N_B subsequences

$$z^j = \{z_{jN_{\text{INTRLV}}}, \ldots, z_{((j+1)N_{\text{INTRLV}}-1)}\} = \{z_0^j, \ldots, z_{N_{\text{INTRLV}}-1}^j\} \quad j = 0, \ldots, N_B - 1$$

of length N_{INTRLV}, with N_B described in Equation (23) and N_{INTRLV} shown in Table 22.

The interleaver is defined by a permutation. The index of the code-bits before the permutation shall be denoted by k, where $k = 0$ refers to the first sample, z_0^j, and $k = N_{\text{INTRLV}} - 1$ refers to the last sample, $z_{N_{\text{INTRLV}}-1}^j$, passed to the interleaver for a given subsequence z^j. The index i shall be the index after the permutation. The permutation is defined by the rule

$$i = \frac{N_{\text{INTRLV}}}{\lambda}((N_{\text{INTRLV}} - 1 - k) \bmod \lambda) + \text{floor}\left(\frac{N_{\text{INTRLV}} - 1 - k}{\lambda}\right) \quad k = 0, \ldots, N_{\text{INTRLV}} - 1\ . \quad (27)$$

Table 22—Parameters of the interleaver

degree λ	**depth** N_{INTRLV}
11	$16 \times 11 = 176$

where the degree λ is given in Table 22. The function floor (.) is a function that returns the largest integer value less than or equal to its argument value. The process of interleaving a subsequence is shown in Figure 24.

The first subsequence, z^0, shall be processed first in time and the last subsequence, z^{N_B-1}, shall be processed last in time.

The deinterleaver, which performs the inverse relation is defined by the rule

$$k = \lambda(N_{\text{INTRLV}} - 1 - i) - (N_{\text{INTRLV}} - 1) \times \text{floor}\left(\frac{\lambda(N_{\text{INTRLV}} - 1 - i)}{N_{\text{INTRLV}}}\right) \quad i = 0, \ldots, N_{\text{INTRLV}} - 1 \quad (28)$$

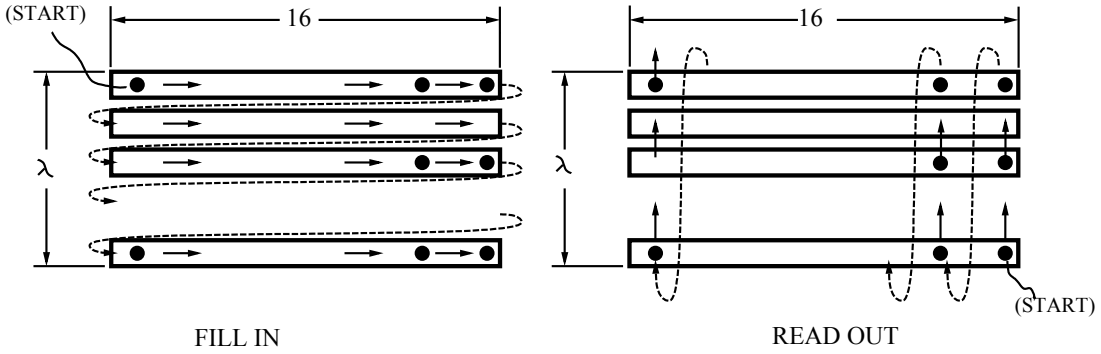

Figure 24—Interleaver

6.12c.5 Support of legacy devices of the 780 MHz, 915 MHz and 2450 MHz O-QPSK PHY

When operating in the 779-787 MHz frequency band, a compliant device of the MR-O-QPSK PHY shall be able to communicate with devices of the 780 MHz band O-QPSK PHY within the specifications given in section 6.8.

When operating in the 906-928 MHz frequency band, a compliant device of the MR-O-QPSK PHY shall be able to communicate with devices of the 915 MHz band O-QPSK PHY within the specifications given in section 6.10.

When operating in the 2400-2483.5 MHz frequency band, a compliant device of the MR-O-QPSK PHY shall be able to communicate with devices of the 2450 MHz band O-QPSK PHY within the specifications given in section 6.5.

Legacy support is feasible at low additional implementation cost due to the following specifications of the MR-O-QPSK PHY:

- O-QPSK modulation is used. O-QPSK with half-sine shaping is very similar to O-QPSK with raised cosine shaping. Since the impulse response of a raised cosine shaping filter satisfies the first Nyquist criteria, EVM specification of 6.13.3 can be easily met.
- For operation in the 779-787 MHz or 902-928 MHz band, the chip rate is 1000 kchip/s. This simplifies sensing of legacy preambles while sensing for a preamble of the MR-O-QPSK PHY.
- For operation in the 779-787 MHz band, the center frequencies of the channels are the same as the center frequencies specified in 6.1.2.3 (**PLEASE REPLACE 6.1.2.3 by CROSS-REFERENCE**).
- For operation in the 902-928 MHz band, the center frequencies of the channels are the same as the center frequencies specified in 6.1.2.1.
- For operation in the 779-787 MHz band, the (16,4)-DSSS code used for bit-to-chip mapping (see Table 17) is the same the code as specified in 6.8. Transmitting a legacy signal can be achieved by bypassing FEC and interleaver and passing a legacy IEEE 802.15.4 PPDU according to 6.3 to the (16,4)-DSSS unit, see Figure 25.
- For operation in the 902-928 MHz band, the (16,4)-DSSS code used for bit-to-chip mapping (see Table 17) is the same the code as specified in 6.10. Transmitting a legacy signal can be achieved by bypassing FEC and interleaver and passing a legacy IEEE 802.15.4 PPDU according to 6.3 to the (16,4)-DSSS unit, see Figure 25.
- For operation in the 2400-2483.5 MHz band, the chip rate is 2000 kchip/s. This simplifies sensing of legacy preambles while sensing for a preamble of the MR-O-QPSK PHY.

— For operation in the 2400-2483.5 MHz band, the (32,4)-DSSS code used for bit-to-chip mapping (see Table 18) is the same the code as specified 6.5. Transmitting a legacy signal can be achieved by bypassing FEC and interleaver and passing a legacy IEEE 802.15.4 PPDU according 6.3 to the (32,4)-DSSS unit, see Figure 25.

— For operation in the 2400-2483.5 MHz band, the center frequencies of the channels are the same as the center frequencies specified in 6.1.2.1.

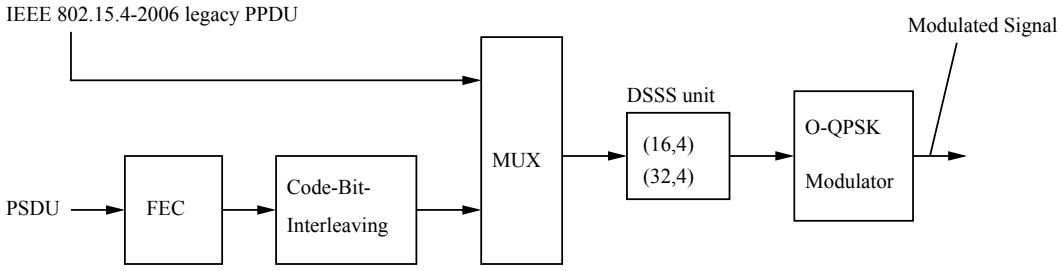

Figure 25—Legacy support for the 780 MHz, 915 MHz and 2450 MHz O-QPSK PHY

6.12c.6 Radio specification

<editor's note: The term "radio specification" is consistent with the subclause names in other PHYs.>

6.12c.6.1 Clock offset tolerance

The clock offset tolerance shall be less or equal to ± 20 ppm. Carrier frequency offset and symbol timing drift due to clock offset shall be locked. When communicating with legacy devices the receiver shall be capable to receive signals with a clock offset tolerance of less or equal to ± 40 ppm.

6.12c.6.2 Receiver sensitivity

Under the conditions specified in 6.1.7, a compliant device shall be capable of achieving a sensitivity of the values given in Table 23 and Table 24 or better.

Table 23—Required receiver sensitivity for *SpreadingMode* "DSSS" [dBm]

Frequency band (MHz)	***RateMode***			
	0	1	2	3
779-787	-105	-100	-95	-90
868-870	-105	-100	not supported	
902-928	-105	-100	-95	-90
2400-2483.5	-105	-100	-95	-90

Table 24—Required receiver sensitivity for S*preadingMode* "M-DSSS" [dBm]

Frequency band (MHz)	*RateMode*			
	0	1	2	3
779-787	not supported			
868-870				
902-928	-105	-100	-95	-90
2400-2483.5	-105	-100	-95	-90

6.12c.6.3 Adjacent channel rejection

The interference-to-signal ratio (ISR) is the maximum ratio of the signal power of an interferer relative to the signal power of the desired signal that leads to a frame error rate (FER) less than 0.01. The adjacent channel rejection shall be measured as follows: the desired signal shall be a compliant signal of this PHY, of pseudo-random PSDU data. For a given *RateMode*, the desired signal is input to the receiver at a level 3 dB above the maximum allowed receiver sensitivity of Table 23 and Table 24.

The interfering signal shall be a compliant signal of this PHY with:

pseudo-random PSDU ,

SpreadingMode is "DSSS",

the same chip rate as the as the desired signal,

chip-withening enabled.

The interferer is separated in frequency by $|\Delta f|$ from the carrier frequency of the desired channel with a minimum ISR as shown in Table 25. The test shall be performed for only one interfering signal at a time. The receiver shall meet the error rate criteria defined in 6.1.7, under these conditions.

Table 25—Minimum interference-to-signal ratio (ISR) depending on $|\Delta f|$

frequency band (MHz) 779-787	$\|\Delta f\|$ (MHz)	2.0	4.0
	ISR (dB)	0	30
frequency band (MHz) 868-870	$\|\Delta f\|$ (MHz)	0.25	0.5
	ISR (dB)	0	20
frequency band (MHz) 902-928	$\|\Delta f\|$ (MHz)	2.0	4.0
	ISR (dB)	0	30
frequency band (MHz) 2400-2483.5	$\|\Delta f\|$ (MHz)	5.0	10.0
	ISR (dB)	0	30

6.12c.6.4 CCA duration

The detection time T_{CCA} for clear channel assessment (CCA) is shown in Table 26.

Table 26—CCA duration

Frequency band (MHz)	T_{CCA} in *microseconds* (us)
779-787	512
868-870	1024
902-928	512
2400-2483.5	512

6.13 General radio specifications

6.13.1 TX-to-RX turnaround time

6.13.2 RX-to-TX turnaround time

Insert the following paragraph at the end of 6.13.2:

In the case of the MR-O-QPSK PHY, the RX-to-TX turnaround time is defined as the shortest time possible at the air interface from the trailing edge of the last chip sample of a received PPDU (including chip samples due to PSDU extension when FEC and interleaving is applied, see 6.12a.3.4) to the leading edge of the first chip sample of the next transmitted PPDU. The RX-to-TX turnaround time shall be less than or equal to *aSUNTurnaroundTime*.

6.13.3 Error-vector magnitude (EVM) definition

6.13.4 Transmit center frequency tolerance

6.13.5 .Transmit power

6.13.6 Receiver maximum input level of desired signal

6.13.7 Receiver ED

6.13.8 Link quality indicator (LQI)

6.13.9 Clear channel assessment (CCA)

Delete the text indicated by strikethrough, insert the text indicated by underline.

The PHY shall provide the capability to perform CCA on the channel specified by *phyCurrentChannel* and *phyCurrentPage* according to at least one of the following six methods (modes 4, 5, and 6 apply only to the UWB PHY):

- *CCA Mode 1: Energy above threshold*. CCA shall report a busy medium upon detecting any energy above the ED threshold.
- *CCA Mode 2: Carrier sense only*. CCA shall report a busy medium only upon the detection of an IEEE 802.15.4 signal with the same modulation and spreading characteristics of the PHY that is currently in use by the device. This signal may be above or below the ED threshold.
- *CCA Mode 3: Carrier sense with energy above threshold*. CCA shall report a busy medium using a logical combination of
  - Detection of a signal with the modulation and spreading characteristics of IEEE Std 802.15.4 and
  - Energy above the ED threshold, where the logical operator may be AND or OR.
- *CCA Mode 4: ALOHA*. CCA shall always report an idle medium.
- *CCA Mode 5: UWB preamble sense based on the SHR of a frame*. CCA shall report a busy medium upon detection of a preamble symbol as specified in 6.12.6. An idle channel shall be reported if no preamble symbol is detected up to a period not shorter than the maximum packet duration plus the maximum period for acknowledgment.
- *CCA mode 6: UWB preamble sense based on the packet with the multiplexed preamble as specified in 6.12.14*. CCA shall report a busy medium upon detection of a preamble symbol as specified in 6.12.6.

For any of the CCA modes, if the PLME-CCA.request primitive (see 6.2.2.1) is received by the PHY during reception of a PPDU, CCA shall report a busy medium. PPDU reception is considered to be in progress following detection of the SFD, and it remains in progress until the number of octets specified by the decoded PHR has been received.

A busy channel shall be indicated by the PLME-CCA.confirm primitive (see 6.2.2.2) with a status of BUSY.

A clear channel shall be indicated by the PLME-CCA.confirm primitive with a status of IDLE.

For the 950 MHz band, if channel 14 is supported CCA shall be performed on channel 13 and channel 14, if channel 17 is supported CCA shall be performed on channel 16 and channel 17 (English translation of ARIB STD-T96 [B1a]).

The PHY PIB attribute *phyCCAMode* (see 6.4) shall indicate the appropriate operation mode. The CCA parameters are subject to the following criteria:

a) The ED threshold shall correspond to a received signal power of at most 10 dB above the specified receiver sensitivity (see 6.7.3.4, 6.8.3.4, 6.9.3.4, 6.10.3.4, ~~and~~ 6.11.3.4, and 6.12c.6.2).

b) Except for the MR-O-QPSK PHY, the ~~The~~ CCA detection time shall be equal to 8 symbol periods for the 868/915 MHz and the 2450 MHz bands or *phyCCADuration* symbol periods for the 950 MHz band PHY. The UWB CCA detection time for CCA mode 6 shall be equal to 40 mandatory symbol periods, which includes at least 8 (multiplexed) preamble symbols (see 6.12.14). For the

MR-O-QPSK PHY, the CCA detection time shall be equal to the time specified in subclause 6.12c.6.4.