A First Look at the Performance of SUN DSSS

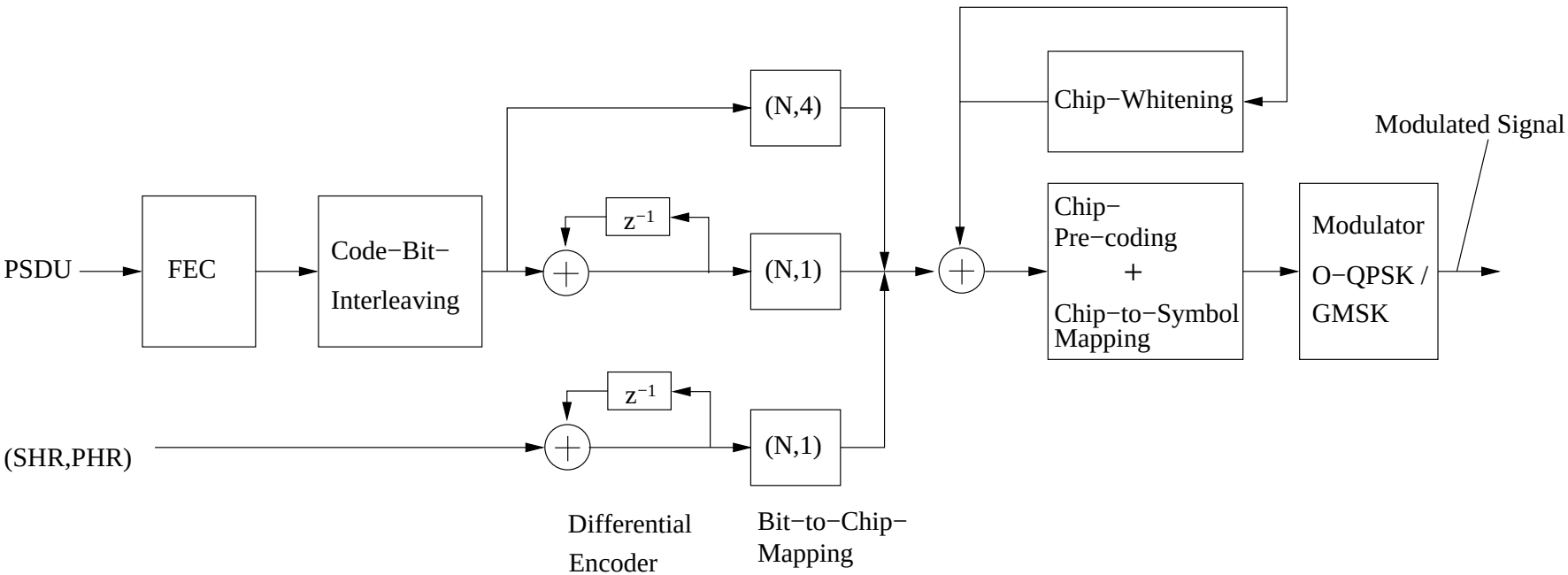
Michael Schmidt (Atmel)

November 14, 2009

- This document refers to the SUN DSSS PHY of document P802.15-09-0738-00-004g colored in Magenta.

- This document refers to the SUN DSSS PHY of document P802.15-09-0738-00-004g colored in Magenta.
- Proposers: Michael Schmidt (Atmel), Y X Fu, J Shen, X Wang, Haituo Liu, L Li, Z Zhao, Z.F Zhao (Huawei/SIMIT/VINNO), Ted Myers, David Howard (On-Ramp Wireless)

Reference Diagram



PPDU Spreading

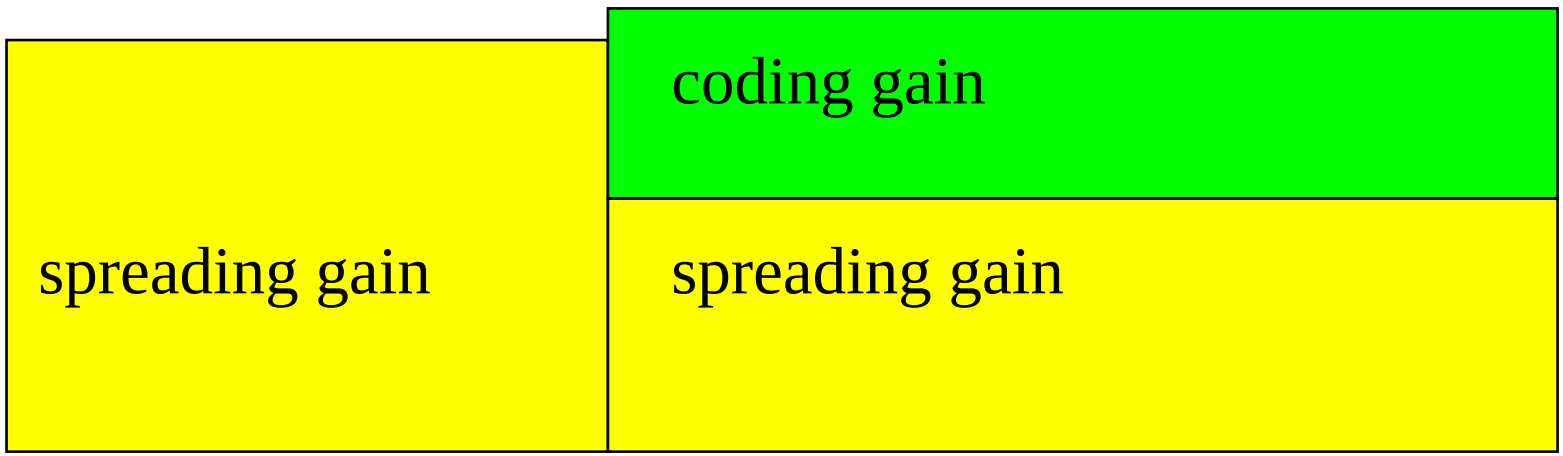
- Current IEEE 802.15.4-2006 PHYs apply a non-variable spreading over the whole PPDU.

PPDU Spreading

- Current IEEE 802.15.4-2006 PHYs apply a non-variable spreading over the whole PPDU.
- Coding gain should be utilized during PSDU.

PPDU Spreading

- Current IEEE 802.15.4-2006 PHYs apply a non-variable spreading over the whole PPDU.
- Coding gain should be utilized during PSDU.



PPDU Spreading

- multiple data rates during PSDU part employing different spreading modes

PPDU Spreading

- multiple data rates during PSDU part employing different spreading modes
- single preamble suitable for the lowest data rate and antenna diversity algorithms

PPDU Spreading

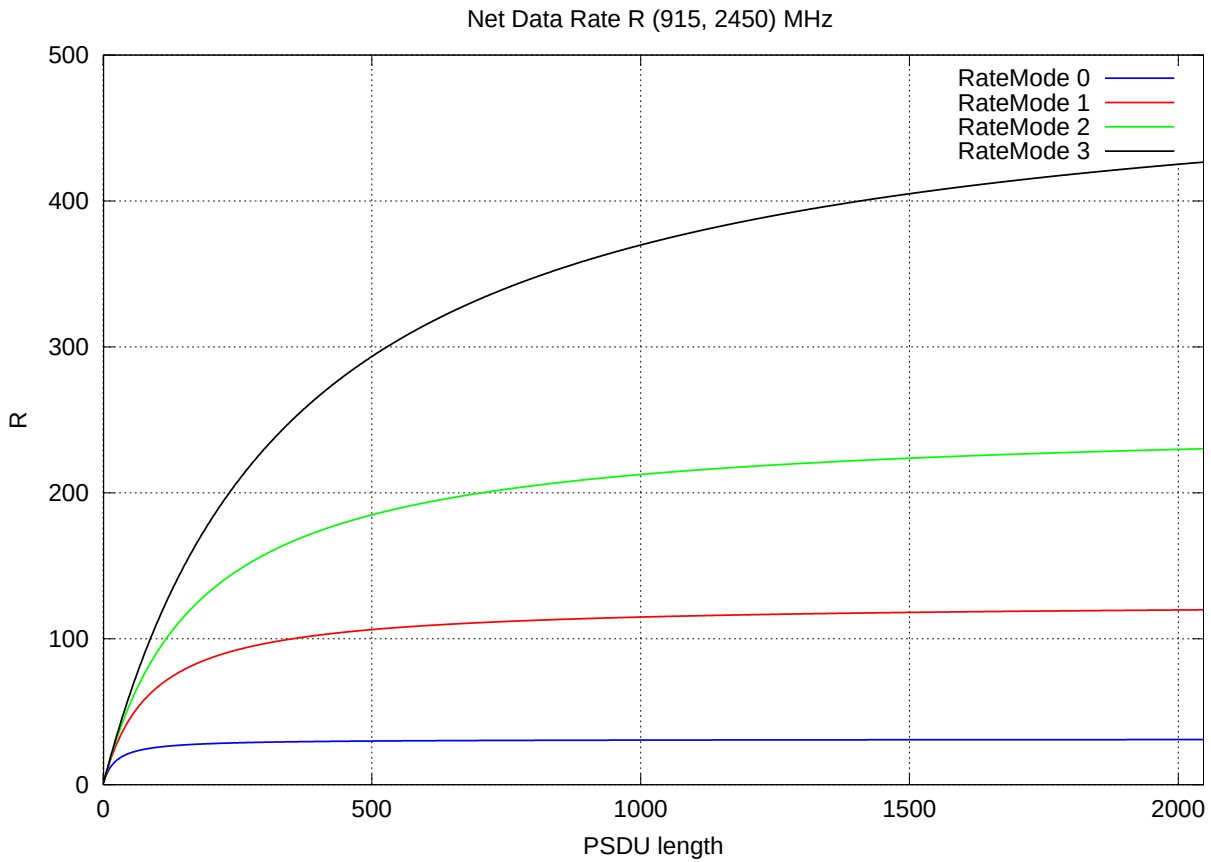
- multiple data rates during PSDU part employing different spreading modes
- single preamble suitable for the lowest data rate and antenna diversity algorithms
- advantage: transceiver can communicate based on the lowest data rate

PPDU Spreading

- multiple data rates during PSDU part employing different spreading modes
- single preamble suitable for the lowest data rate and antenna diversity algorithms
- advantage: transceiver can communicate based on the lowest data rate
- disadvantage: considerable overhead for the higher data rates

Effective Data Rate

$$R = R_0 \frac{t_{PSDU}}{t_{PSDU} + t_{SHR,PHR}}$$



Approach

- outer FEC (convolutional coding)

Approach

- outer FEC (convolutional coding)
- code bit interleaving

Approach

- outer FEC (convolutional coding)
- code bit interleaving
- inner low complexity block coding (DSSS)

Approach

- outer FEC (convolutional coding)
- code bit interleaving
- inner low complexity block coding (DSSS)
- chip whitening (for some modes)

Why not using Rate 1/n FEC only?

- lower complexity

Why not using Rate 1/n FEC only?

- lower complexity
- easier to synchronize (e. g. phase control loop)

Why not using Rate 1/n FEC only?

- lower complexity
- easier to synchronize (e. g. phase control loop)
- improved multipath robustness

DSSS Types

- no spreading at all

DSSS Types

- no spreading at all
- $(N, 1)$ spreading combined with differential encoding

DSSS Types

- no spreading at all
- $(N, 1)$ spreading combined with differential encoding
- $(N, 4)$ spreading

$(N, 1)$ Spreading

- 2-ary code set C

$(N, 1)$ Spreading

- 2-ary code set C
- processing gain but no coding gain

$(N, 1)$ Spreading

- 2-ary code set C
- processing gain but no coding gain
- no phase control required due to differential encoding

$(N, 1)$ Spreading

- 2-ary code set C
- processing gain but no coding gain
- no phase control required due to differential encoding
- simple way for carrier sense for $N \geq 16$

$(N, 1)$ Spreading

- 2-ary code set C
- processing gain but no coding gain
- no phase control required due to differential encoding
- simple way for carrier sense for $N \geq 16$
- simple way to compute soft outputs

$$L(b_i) = \mathrm{Re}\left\{\xi(\underline{c}_{b=1})\underline{r}_i^T \cdot \mathrm{conj}\xi(\underline{c}_{b=1})\underline{r}_{i-1}^T\right\}$$

$(N, 4)$ Spreading

- 16-ary code set C

$(N, 4)$ Spreading

- 16-ary code set C
- processing gain with moderate coding gain

$(N, 4)$ Spreading

- 16-ary code set C
- processing gain with moderate coding gain
- more suitable to obtain lower spreading factors $\{2, 4, 8\}$

$(N, 4)$ Spreading

- 16-ary code set C
- processing gain with moderate coding gain
- more suitable to obtain lower spreading factors $\{2, 4, 8\}$
- phase control required

$(N, 4)$ Spreading

- 16-ary code set C
- processing gain with moderate coding gain
- more suitable to obtain lower spreading factors $\{2, 4, 8\}$
- phase control required
- carrier sense less obvious and not possible for $(8, 4)$

$(N, 4)$ Spreading

- 16-ary code set C
- processing gain with moderate coding gain
- more suitable to obtain lower spreading factors $\{2, 4, 8\}$
- phase control required
- carrier sense less obvious and not possible for $(8, 4)$
- computation of soft outputs is less elegant

$$L(b_i) = \max_{\underline{c} \in C_{b_i=1}} \mathrm{Re}\{\xi(\underline{c}) \underline{r}_k^T\} - \max_{\underline{\tilde{c}} \in C_{b_i=0}} \mathrm{Re}\{\xi(\underline{\tilde{c}}) \underline{r}_k^T\}$$

Modulation

- O-QPSK with raised cosine shaping
- GMSK

- binary symbols

Modulation

- O-QPSK with raised cosine shaping
- GMSK

- binary symbols
- reduced side lobes

Modulation

- O-QPSK with raised cosine shaping
- GMSK

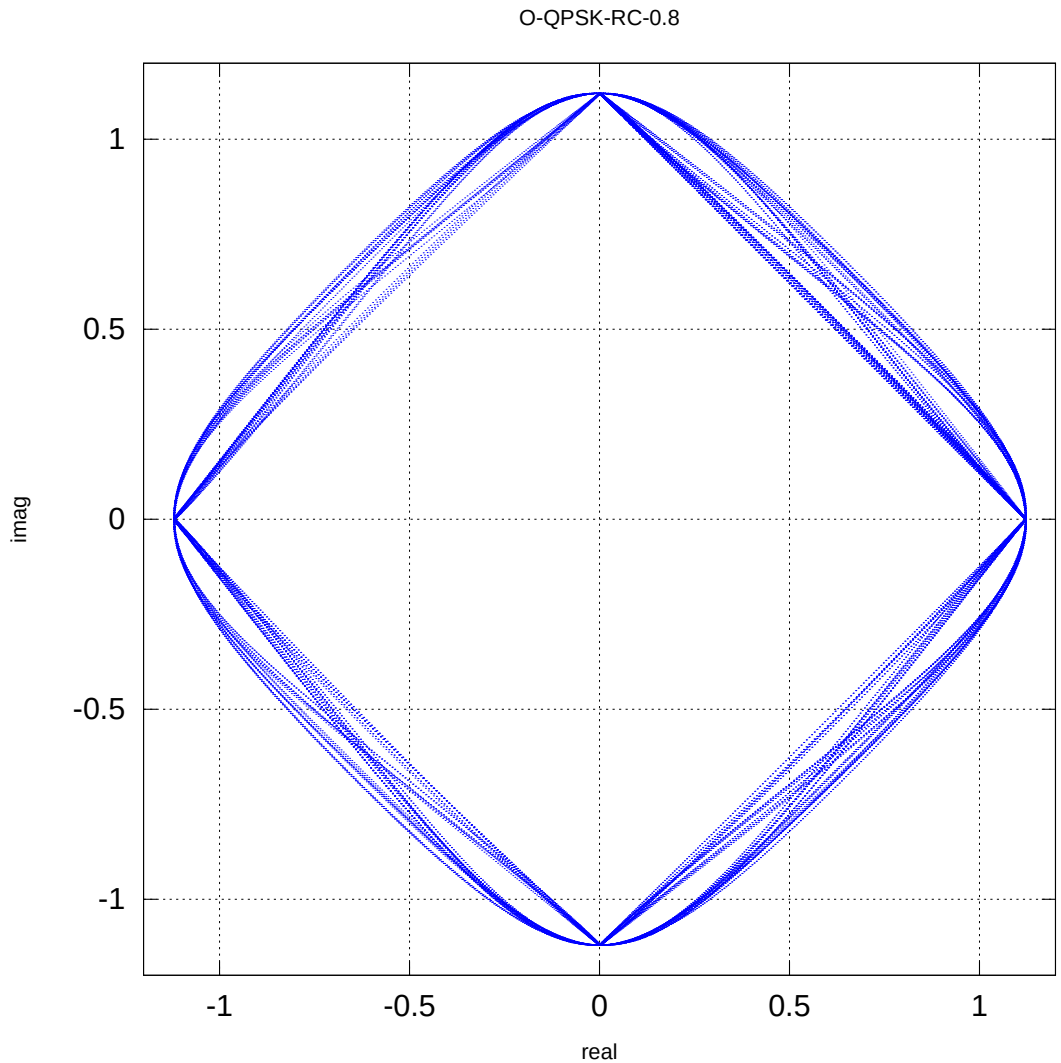
- binary symbols
- reduced side lobes
- low peak-to-average ratio / constant envelope

Modulation

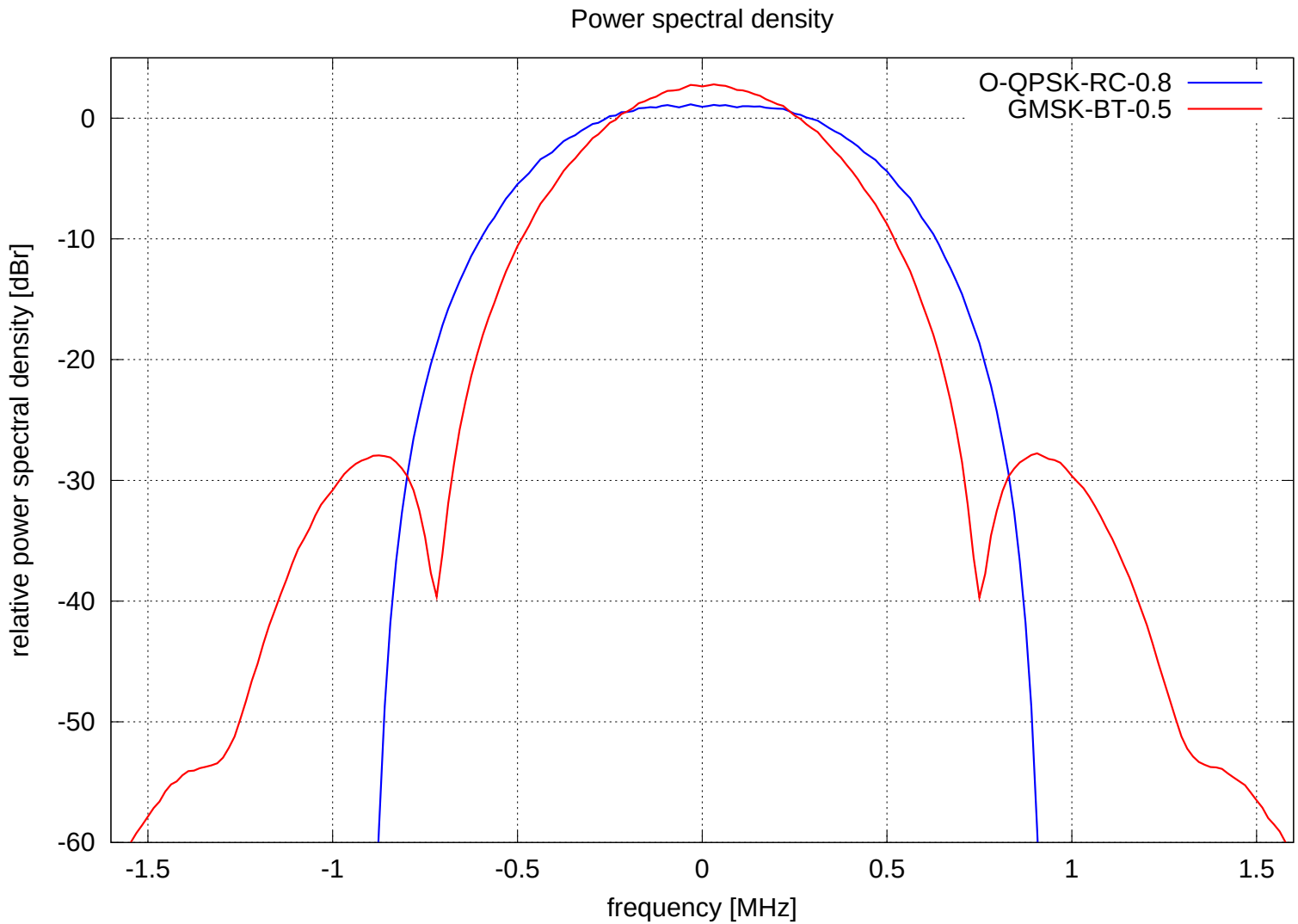
- O-QPSK with raised cosine shaping
- GMSK

- binary symbols
- reduced side lobes
- low peak-to-average ratio / constant envelope
- Compared to BPSK, truly complex baseband signal (in order to resolve symmetric IQ images)

O-QPSK-RC-0.8 I/Q Plot



O-QPSK-RC-0.8/ GMSK-BT-0.5 Spectrum



O-QPSK-RC-0.8 vs GMSK-BT-0.5

O-QPSK-RC-0.8:

- better spectral efficiency
- Nyquist

GMSK:

- constant envelope
- direct modulation

Pre-Coding for O-QPSK / GMSK

- Allow both co-alternatively using pre-coding

$$c'_k = \begin{cases} c_k \quad \text{for } k \bmod 4 \in \{0,1\} \\ \overline{c}_k \quad \text{for } k \bmod 4 \in \{2,3\} \end{cases} \qquad \text{O-QPSK}$$

$$c_k \oplus c_{k-1} \qquad \text{GMSK}$$

- baseband signal after pre-coding

$$y(t) \underset{\approx}{=} \begin{cases} \sum_k \xi\{c_k\} j^k p(t - kT_c) & \text{O-QPSK} \\ \sum_k \xi\{c_k\} j^k h_0(t - kT_c) & \text{GMSK} \end{cases}$$

Frequency Band 915 /2450 MHz

chip rate: 1000 kchip/s
Why not less?

- Target *digital modulation* according to FCC 247 part 15 for both GMSK and O-QPSK

Frequency Band 915 /2450 MHz

chip rate: 1000 kchip/s
Why not less?

- Target *digital modulation* according to FCC 247 part 15 for both GMSK and O-QPSK
- For high output power transmission, frequency hopping is not required (dwell time on a channel can be considerably increased).

Frequency Band 915 /2450 MHz

chip rate: 1000 kchip/s
Why not less?

- Target *digital modulation* according to FCC 247 part 15 for both GMSK and O-QPSK
- For high output power transmission, frequency hopping is not required (dwell time on a channel can be considerably increased).
- The 6-dB bandwidth must be larger than 500 kHz.

Frequency Band 915 /2450 MHz

chip rate: 1000 kchip/s
Why not less?

- Target *digital modulation* according to FCC 247 part 15 for both GMSK and O-QPSK
- For high output power transmission, frequency hopping is not required (dwell time on a channel can be considerably increased).
- The 6-dB bandwidth must be larger than 500 kHz.
- Spectral density limit of 8 dBm in any 3 kHz band during any time interval of continuous transmission: Maximum output power is approx. 25 dBm (O-QPSK-RC-0.8) or 23 dBm (GMSK) depending on the spectral properties of the chip sequence.

Simulation Model

Monte Carlo Simulation. For each frame, select:

- random timing offset

Simulation Model

Monte Carlo Simulation. For each frame, select:

- random timing offset
- random phase

Simulation Model

Monte Carlo Simulation. For each frame, select:

- random timing offset
- random phase
- random channel (in case of multipath)

Cont. Simulation Model

Radio model

- Low IF receiver

Cont. Simulation Model

Radio model

- Low IF receiver
- LNA noise: -174 dBm/Hz + 5 dB noise figure

Cont. Simulation Model

Radio model

- Low IF receiver
- LNA noise: -174 dBm/Hz + 5 dB noise figure
- 4-th order Butterworth filter

Cont. Simulation Model

Radio model

- Low IF receiver
- LNA noise: -174 dBm/Hz + 5 dB noise figure
- 4-th order Butterworth filter
- 2-x 50 kHz high pass filter

Cont. Simulation Model

Radio model

- Low IF receiver
- LNA noise: -174 dBm/Hz + 5 dB noise figure
- 4-th order Butterworth filter
- 2-x 50 kHz high pass filter
- clock offset: up to $\pm$20 ppm

Cont. Simulation Model

Radio model

- Low IF receiver
- LNA noise: -174 dBm/Hz + 5 dB noise figure
- 4-th order Butterworth filter
- 2-x 50 kHz high pass filter
- clock offset: up to $\pm$20 ppm
- ADC resolution: 1 bit (I/Q)

Cont. Simulation Model

Radio model

- Low IF receiver
- LNA noise: -174 dBm/Hz + 5 dB noise figure
- 4-th order Butterworth filter
- 2-x 50 kHz high pass filter
- clock offset: up to $\pm$20 ppm
- ADC resolution: 1 bit (I/Q)
- discrete time post filter (5-th order elliptic filter)

Cont. Simulation Model

Radio model

- Low IF receiver
- LNA noise: -174 dBm/Hz + 5 dB noise figure
- 4-th order Butterworth filter
- 2-x 50 kHz high pass filter
- clock offset: up to $\pm$20 ppm
- ADC resolution: 1 bit (I/Q)
- discrete time post filter (5-th order elliptic filter)

chip rate (kchip/s)	IF (MHz)	f_{cut}	ADC rate (MHz)
125	0.2	0.1	4
500	0.5	0.3	16
1000	1.0	0.6	16

Simulation Model

Baseband signal processing

- peak search time resolution: twice the chip rate

Simulation Model

Baseband signal processing

- peak search time resolution: twice the chip rate
- clock offset estimation: 256 frequency point Rake correlator ($\pm$40 ppm range)

Simulation Model

Baseband signal processing

- peak search time resolution: twice the chip rate
- clock offset estimation: 256 frequency point Rake correlator ($\pm$40 ppm range)
- SFD search: exact pattern match

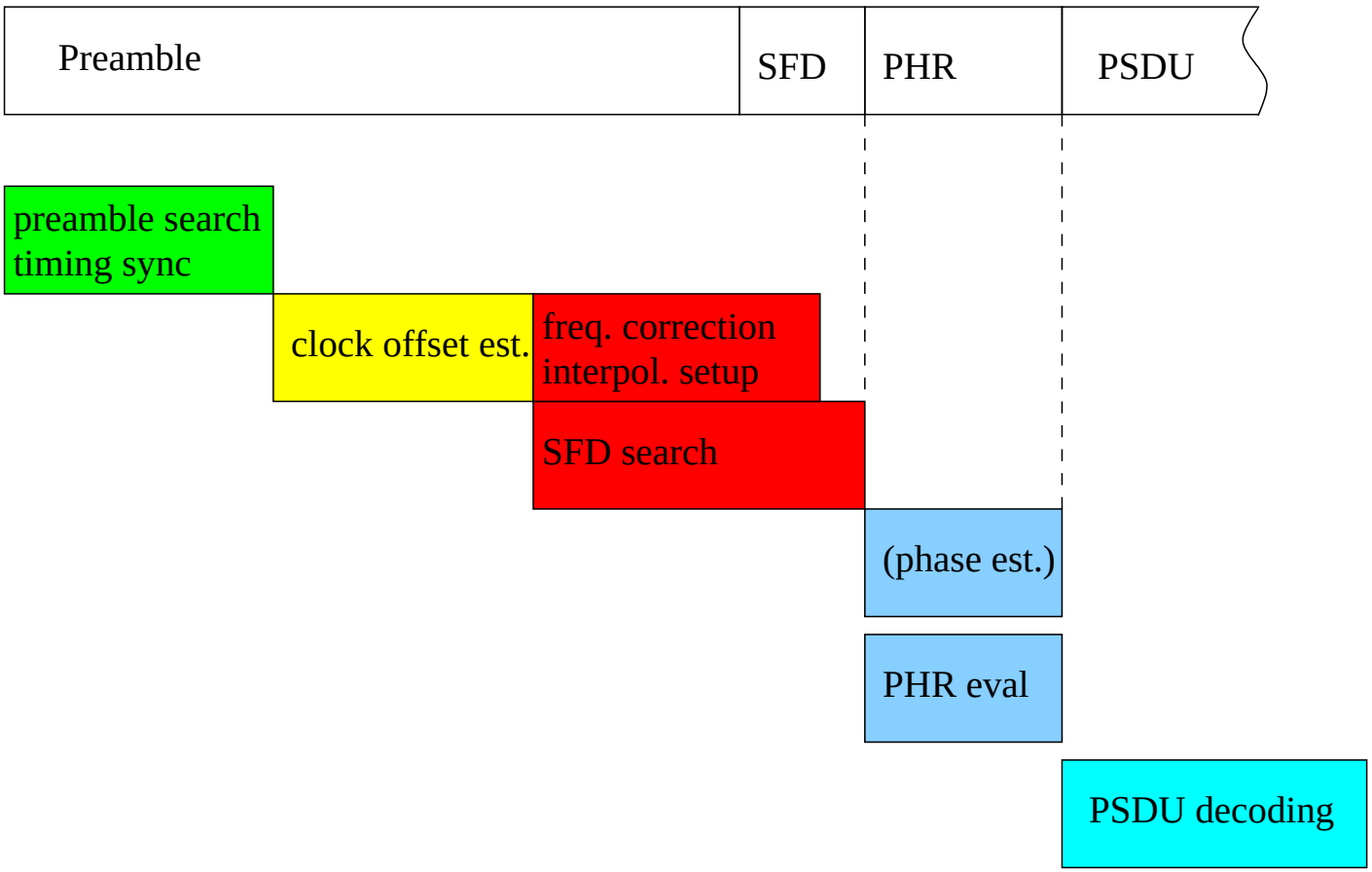
Simulation Model

Baseband signal processing

- peak search time resolution: twice the chip rate
- clock offset estimation: 256 frequency point Rake correlator ($\pm$40 ppm range)
- SFD search: exact pattern match
- phase control during PSDU (if applicable): 1-st order loop filter

Simulation Model

Baseband signal processing



Clock Offset Estimation

- Accurate clock offset estimation is one of the challenges of DSSS.

Clock Offset Estimation

- Accurate clock offset estimation is one of the challenges of DSSS.
- relative long correlation sequences

Clock Offset Estimation

- Accurate clock offset estimation is one of the challenges of DSSS.
- relative long correlation sequences
- Chip differential correlation will give insufficient performance for spreading factors larger than 8.

Cont. Clock Offset Estimation

example: Rake-type clock offset estimator

- 915 MHz

Cont. Clock Offset Estimation

example: Rake-type clock offset estimator

- 915 MHz
- 1000 kchip/s

Cont. Clock Offset Estimation

example: Rake-type clock offset estimator

- 915 MHz
- 1000 kchip/s
- (64,1) spreading during SHR

Cont. Clock Offset Estimation

example: Rake-type clock offset estimator

- 915 MHz
- 1000 kchip/s
- (64,1) spreading during SHR
- receive power: -116 dBm

Cont. Clock Offset Estimation

example: Rake-type clock offset estimator

- 915 MHz
- 1000 kchip/s
- (64,1) spreading during SHR
- receive power: -116 dBm
- select random clock offset within $(-40, 40)$ ppm

Cont. Clock Offset Estimation

example: Rake-type clock offset estimator

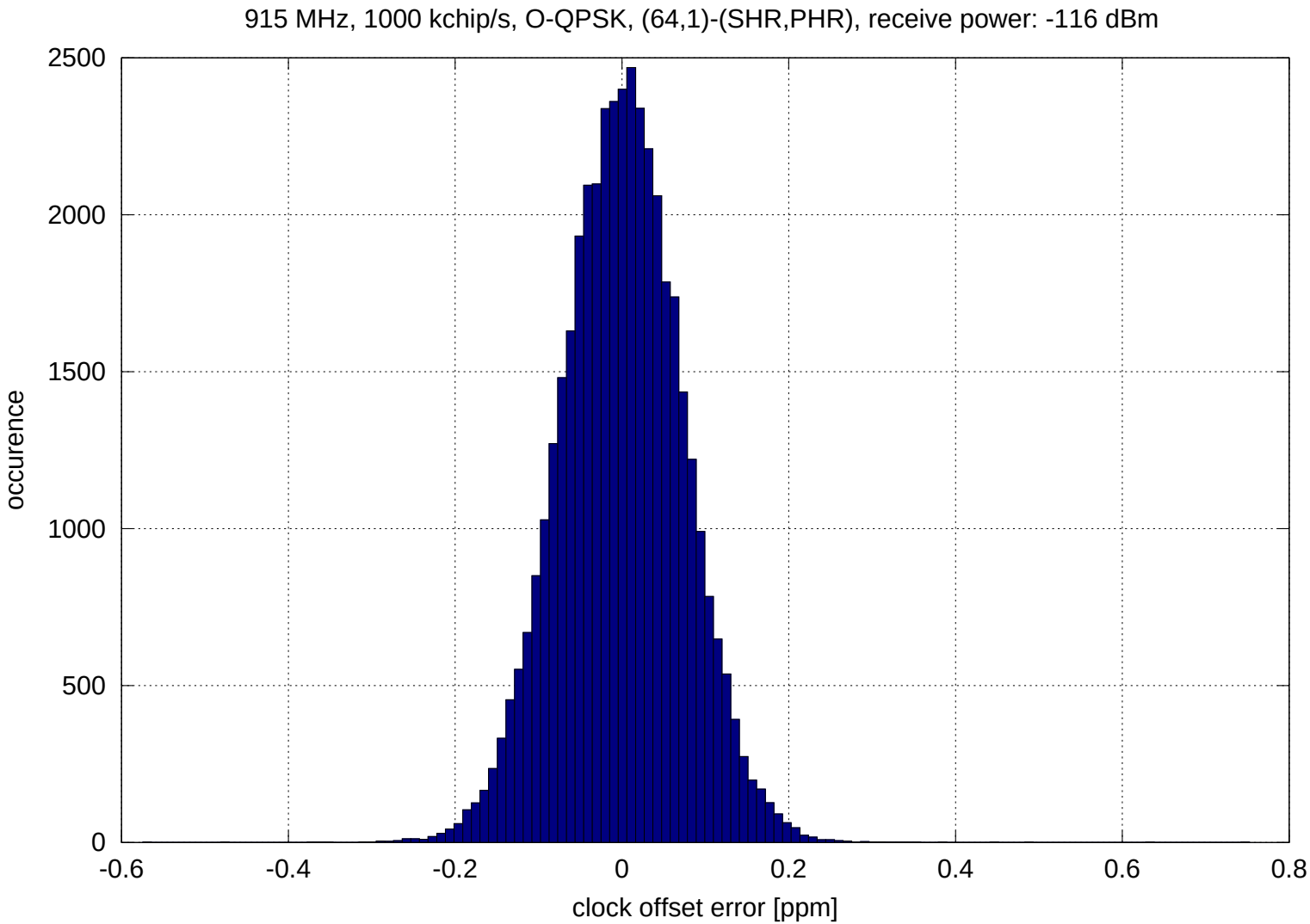
- 915 MHz
- 1000 kchip/s
- (64,1) spreading during SHR
- receive power: -116 dBm
- select random clock offset within $(-40, 40)$ ppm
- estimate clock offset

Cont. Clock Offset Estimation

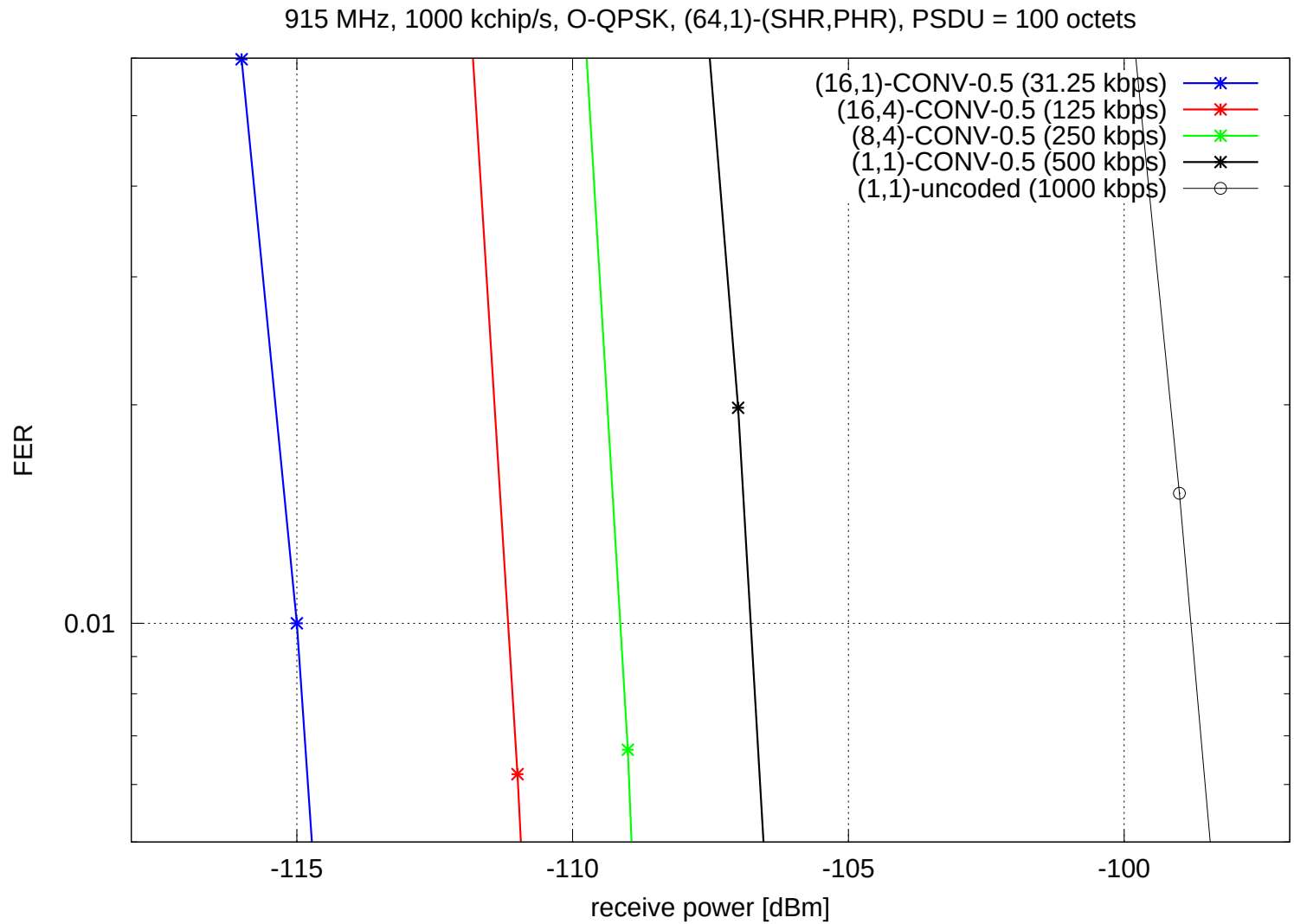
example: Rake-type clock offset estimator

- 915 MHz
- 1000 kchip/s
- (64,1) spreading during SHR
- receive power: -116 dBm
- select random clock offset within $(-40, 40)$ ppm
- estimate clock offset
- compute estimation error

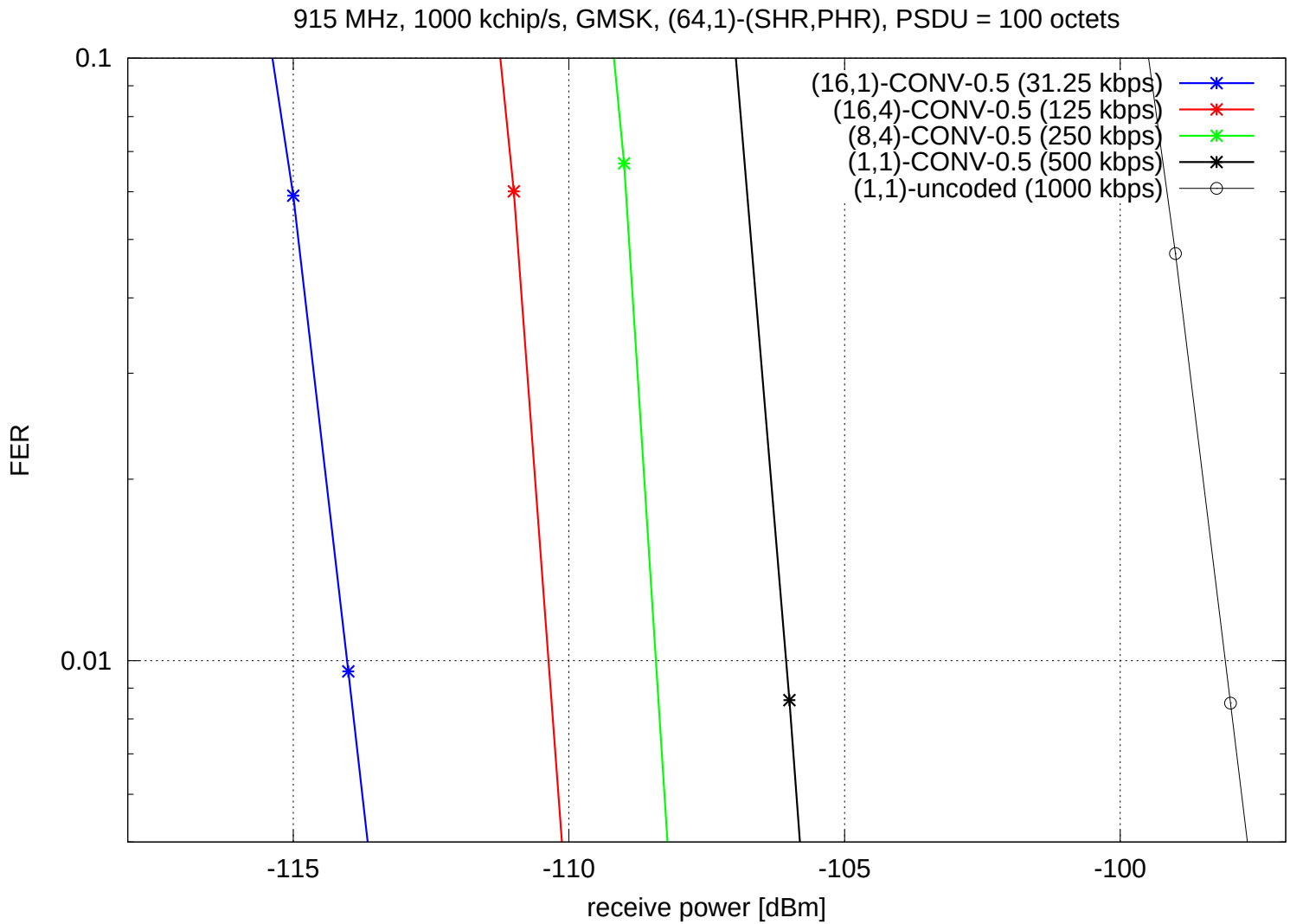
Cont. Clock Offset Estimation



915 MHz, O-QPSK, AWGN



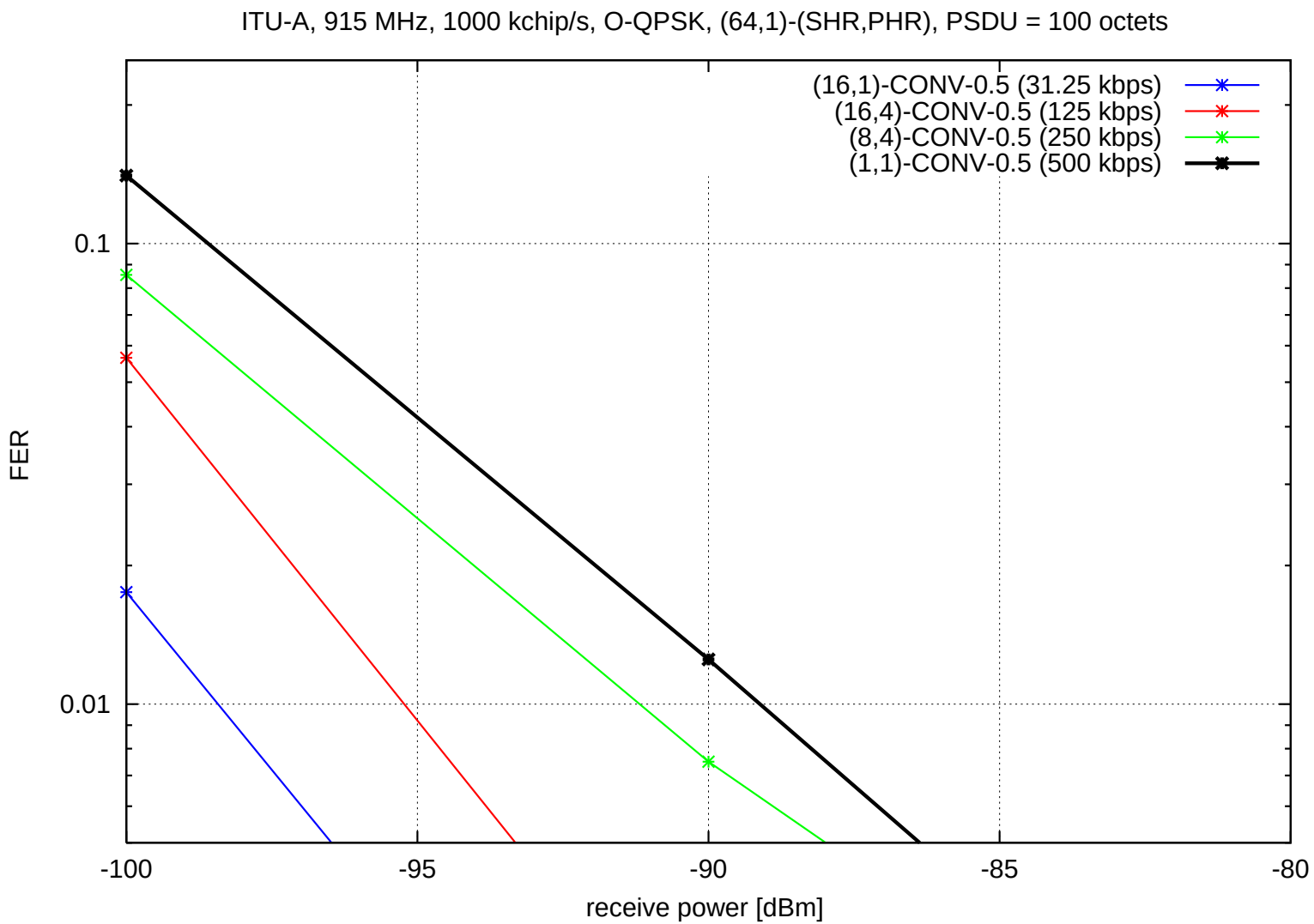
915 MHz, GMSK, AWGN



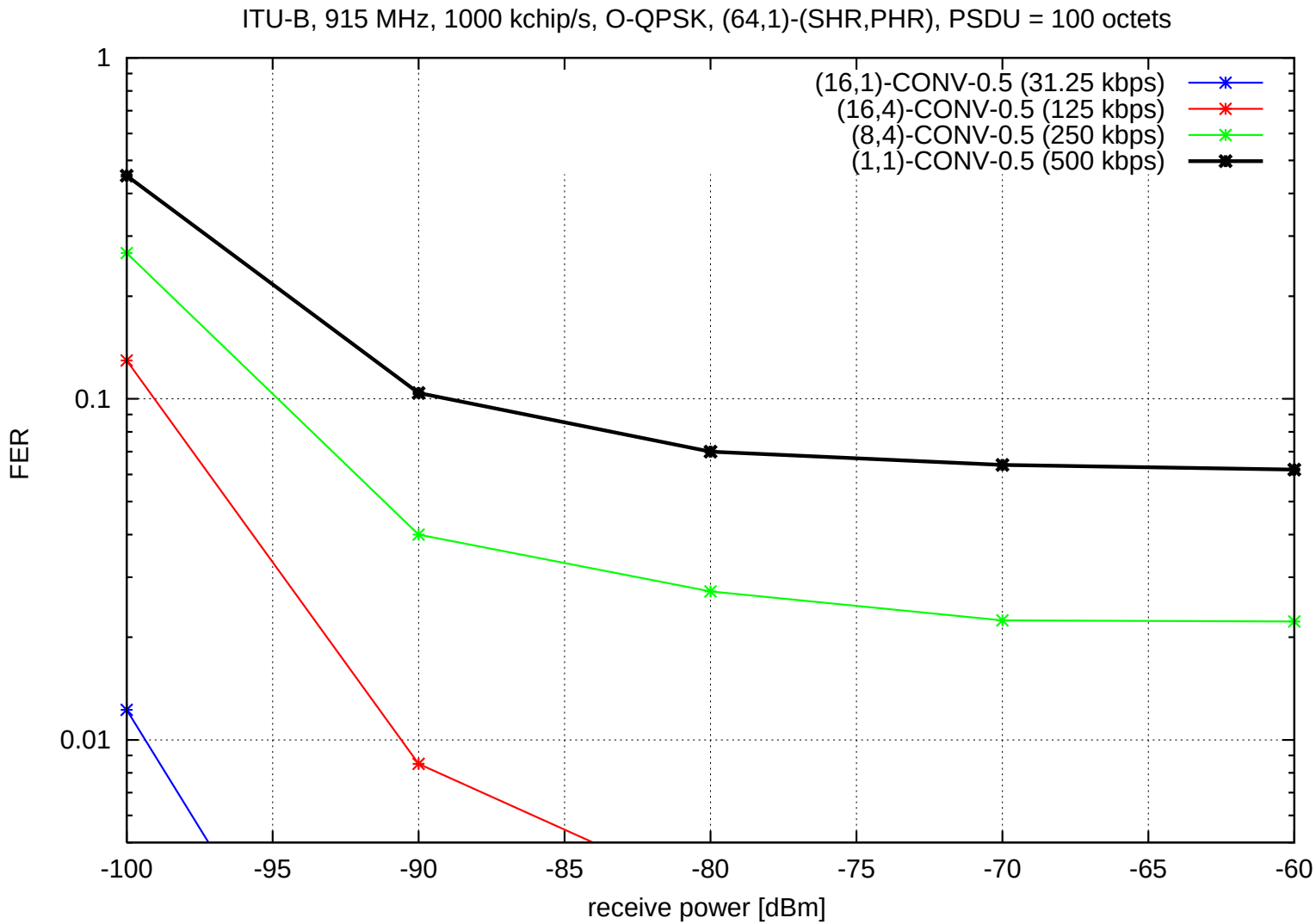
Multipath Fading: Channel Model

ITU-A		ITU-B		2-PATH	
rD (ns)	rP (dB)	rD (ns)	rP (dB)	rD (ns)	rP (dB)
0	0	0	0	0	0
110	-9.7	200	-0.9	5000	-3
190	-19.2	800	-4.9		
410	-22.8	1200	-8		
		2300	-7.8		
		3700	-23.9		

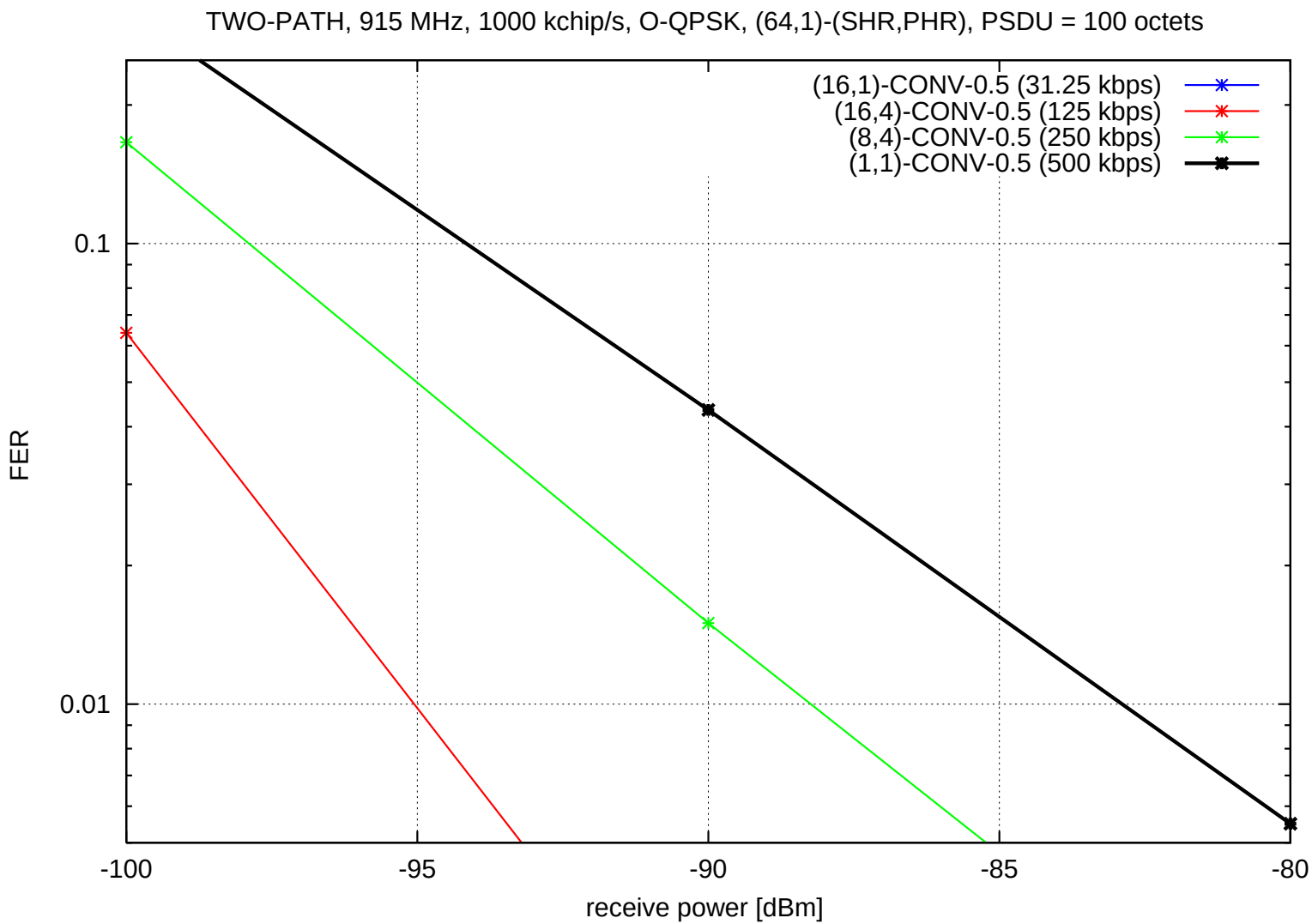
915 MHz, O-QPSK, ITU-A



915 MHz, O-QPSK, ITU-B



915 MHz, O-QPSK, 2-PATH



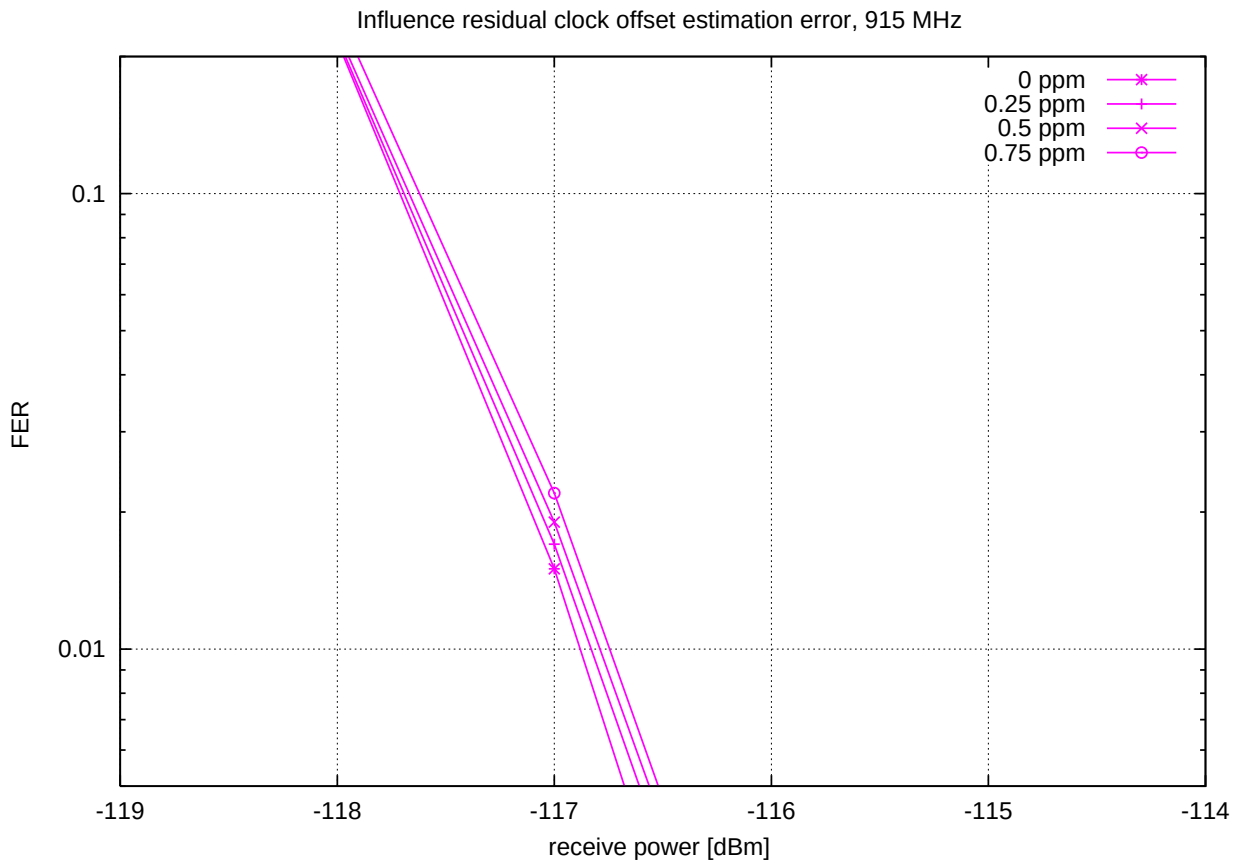
Why not considering larger spreading for 915/2450 MHz?

Option:

- chip rate: keep at 1000 kchip/s
- (SHR,PHR): increase spreading from (64,1) to (128,1)
- PSDU: decrease data rate to 15.625 kbps

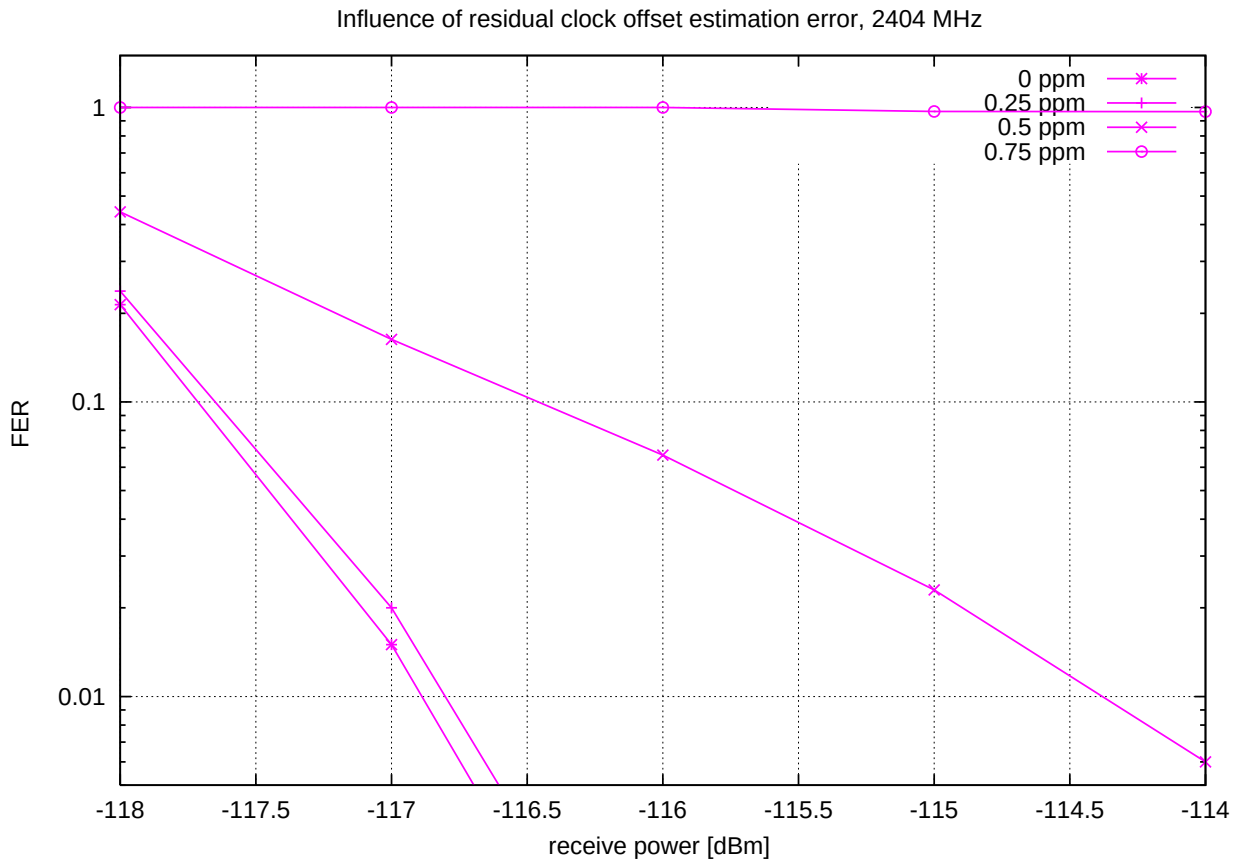
Influence of Residual Estimation Error of Clock Offset

- carrier frequency: 915 MHz
- chip rate: 1000 kchip/s
- (SHR,PHR): (128,1)
- PSDU: (32,1)-CONV-0.5 (15.625 kbps)



Influence of Residual Estimation Error of Clock Offset

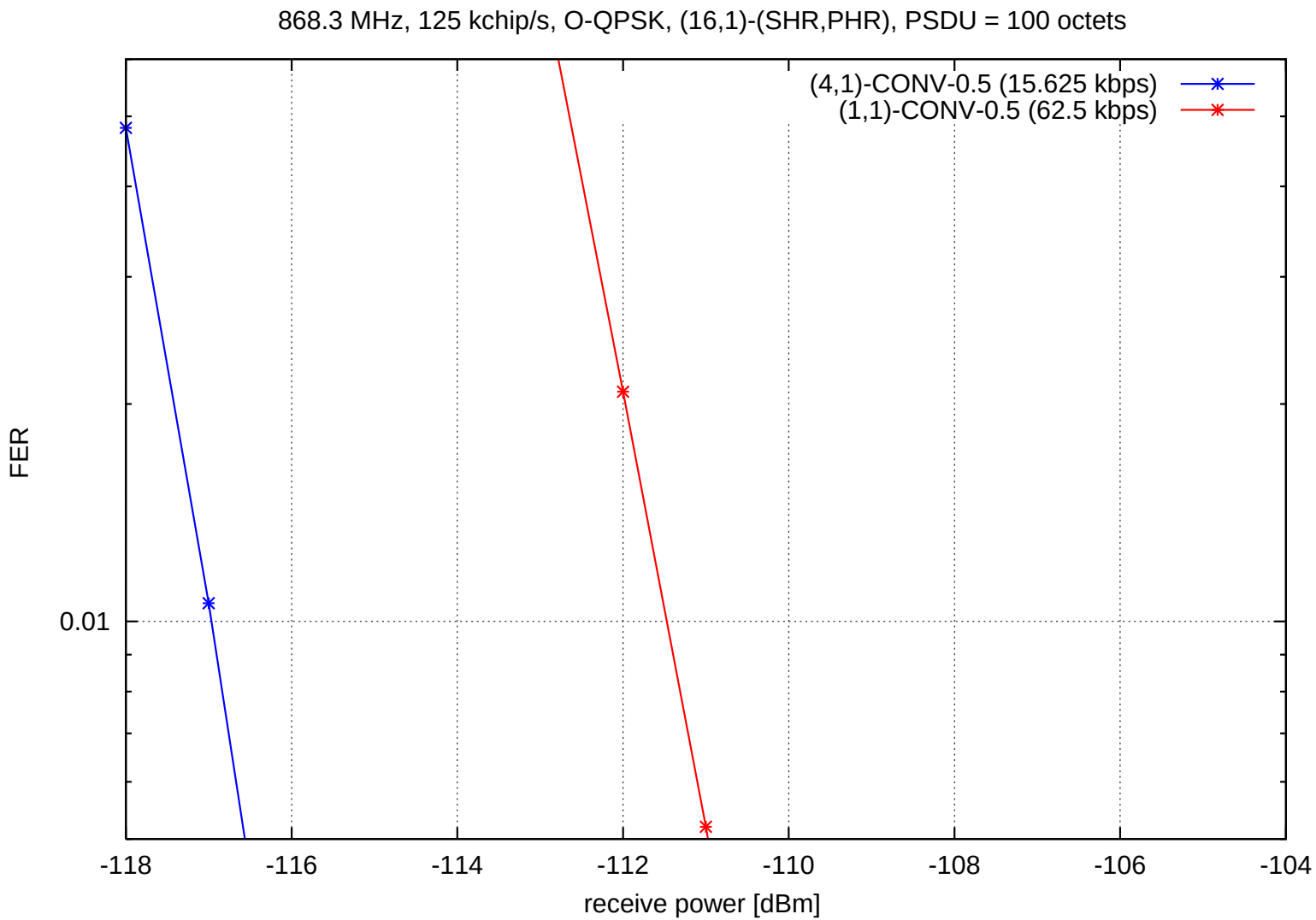
- carrier frequency: 2404 MHz
- chip rate: 1000 kchip/s
- (SHR,PHR): (128,1)
- PSDU: (32,1)-CONV-0.5 (15.625 kbps)



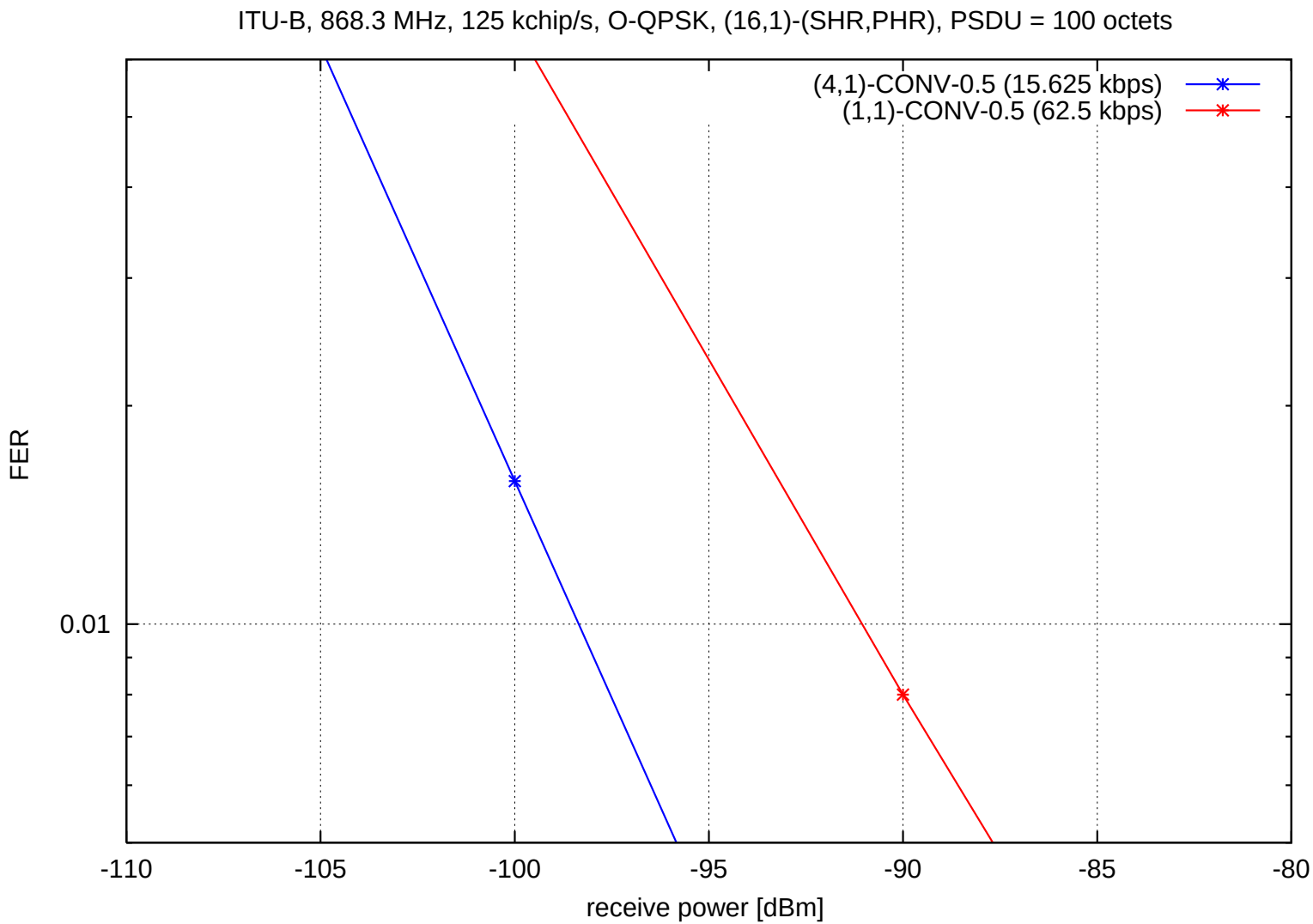
863-870 MHz Band

- chip rate 125 kchip/s in order to utilize sub-band G3 and keep the B_{99}-bandwidth below 200 kHz
- only 2 data rates: 15.625 kbps and 62.5 kbps
- additional data rate of 100 kbps (4/5 rate FEC) subject to further investigations

868.3 MHz, O-QPSK, AWGN



868.3 MHz, O-QPSK, ITU-B



To Do

- revise 0.4 MHz channel spacing
  - for 125 kchip/s: less appropriate for an IF of 0.2 MHz and clock offset (IQ images)
  - for 1000 kchip/s: find a useful upper and lower center frequency, consider IQ images

To Do

- revise 0.4 MHz channel spacing
  - for 125 kchip/s: less appropriate for an IF of 0.2 MHz and clock offset (IQ images)
  - for 1000 kchip/s: find a useful upper and lower center frequency, consider IQ images
- details on bit interleaver

To Do

- revise 0.4 MHz channel spacing
  - for 125 kchip/s: less appropriate for an IF of 0.2 MHz and clock offset (IQ images)
  - for 1000 kchip/s: find a useful upper and lower center frequency, consider IQ images
- details on bit interleaver
- optimize $(N, 1)$ codes w. r. t. signal and sync properties

Thank you!