IEEE P802.15
Wireless Personal Area Networks

Project	IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)		
Title	**Proposal for Visible Light Communication Physical Layer Specification**		
Date Submitted	October 28, 2009		
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Re:	Response to call for proposals on October 30th, 2009. Support for VLCC proposal "Introduction of VLCC Visible Light Communication Physical Layer Specification Version 1.0", IEEE 802.15.-09-0684-00-0007, September 18th, 2009		
Abstract	This specification is needed in Visible Light Communication. This proposal presents the scopes for (A) Point to Multi Point usage Model and (B) Point to Point usage Model.		
Purpose	Proposal to IEEE 802.15.7. VLC TG		
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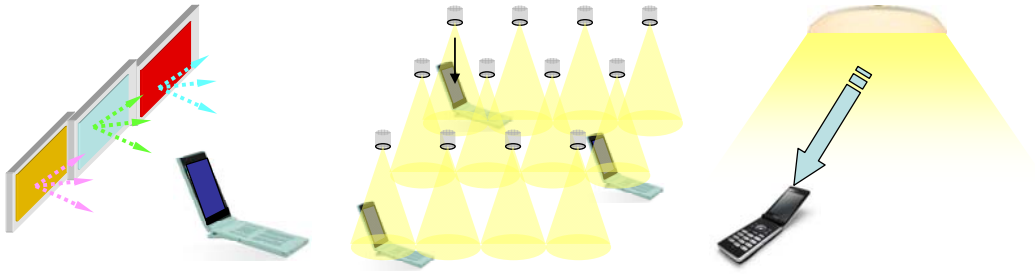
1. Introduction

1.1. History

Visible Light Communications Consortium (VLCC) has been working on standardization of visible light communication since its founding in 2003. In 2007, the VLCC team worked on the first visible light communication standards and proposed them to JEITA (Japan Electronics and Information Technology Industries Association) and developed in two visible light communication documents: CP-1221 and CP-1222. In September 2008,both VLCC which is working on research, development and the standardization of visible light communications (VLC) and the IrDA responsible for developing the Infrared communication standards to provide convenient wireless connectivity,announced a cooperative agreement between the two organizations.

1.2. Scope

(A) Point to Multipoint usage Models

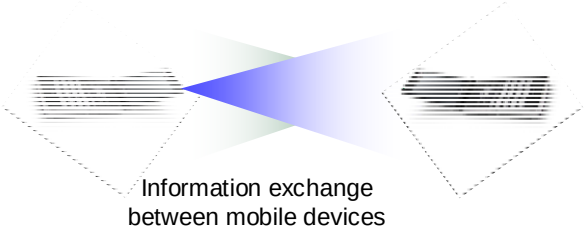


Advertising illuminations or Digital signage systems

Pinpoint information system using Down light illuminations

Information distribution in public space

(B) Point to Point usage Model



Information exchange between mobile devices

Figure 1.2 VLC typical usage models

This specification describes physical layer aspect for the free-space visible light communication from a visible light source. This document specifies the optical media interfaces, modulation and demodulation. Moreover , this specification is intended to facilitate the point-to-multipoint (broadcasting model) and point-to-point (peer to peer model) communication between light source equipments (e.g., LED lighting , Illumination signboard or other visible light sources) and mobile devices or electronic devices (e.g., cell phones and peripherals) using directed serial visible light communications (VLC) links through free space and schematic view of the optical interface geometry is shown in Figure 1. This document specifies the optical media interfaces, and 4.0 Mb/s modulation and demodulation. It contains specifications for the Active Output Interface and the Active Input Interface, and for the overall link. It also contains Appendices covering test methods and implementation examples.

1.2.1. Two modulation methods

This specification describes two modulation methods. One is an inverted-4PPM modulation method, another is a Manchester Code Data Modulation method. A 4PPM modulation method is compatible with an IrDA system. Therefore, the extension to VLCC from an IrDA system is easy (without modification of IrDA modem controller). On the other hand, the Manchester Code Data Modulation method is excellent in DC-balance characteristic. This system is a system original with VLCC. These two modulation methods can be properly used in applicable fields. Especially for the mobile device sides, support of both of systems is required (in case of Invert-4PPM, mobile devices may support receiving only).

1.3. Abbreviations & Acronyms

AGC	: Automatic Gain Control
AOC	: Automatic Offset Control
ATC	: Automatic Threshold Control
Base	: Number of pulse positions (chips) in each data symbol
BER	: Bit Error Ratio
CDF	: Cumulative Distribution Function
CDR	: Clock & Data Recovery
Chip	: One time slice in a PPM symbol
CIE	: Commission Internationale d'Eclairage
cm^2	: square centi meter
Ct	: uration of one chip
CRC	: Cyclic Redundancy Check
dB	: decibel
DRTO	: Digital Real Time Oscilloscope
DSO	: Digital Sampling Oscilloscope
DUT	: Device Under Test
IEC	: International Electrotechnical Commission
I-4PPM	: Inverted four Pulse Position Modulation
kb/s	: kilobits per second
kHz	: kilohertz
LED	: Light Emitting Diode
LVDS	: Low Voltage Differential Signaling
LVPECL	: Low Voltage Positive Emitter Coupled Logic
LVTTL	: Low Voltage TTL Level

Mb/s	: Megabits per second
MHz	: MegaHertz
mW:	: milliwatt
ms	: millisecond
nm	: nanometer
PDF	: Probability Distribution Function
PLL	: Phase Locked Loop
PPG	: Pulse Pattern Generator
PPM	: Pulse Position Modulation
SNR	: Signal Noise Ratio
TIA	: Time Interval Analysis
TIE	: Time Interval Error
UI	: Unit Interval
4PPM	: Four Pulse Position Modulation

1.4. References

The following standards either contain provisions that, through reference in this text, constitute provisions of this proposed standard, or provide background information. At the time of publication of this document, the editions and dates of the referenced documents indicated were valid. However, all standards are subject to revision, and parties to agreements based on this proposed standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

[1] IrDA (Infrared Data Association) Serial Infrared Physical Layer Link Specification, Version 1.2, November 10, 1997.

[2] IEC Standard Publication 801-3: Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 3: Radiated Electromagnetic Field Measurements.

[3] IEC 60825-1:(1993) Safety of laser products-Part 1: Equipment classification, requirements and user's guide, as amended (reported at TC 76 Meeting, Frankfurt, Germany, October 31, 1997).

[4] CIE S 009/IEC 62471 (2002), Photobiological safety of lamps and lamp systems.

2. General Description

2.1. Visible Light Communication Link Overview

The visible light communication link supports optical link uses visible light whose wavelength ranges from 400nm to 780nm. The data rate in the first version is 4 Mb/s. The visible light packet format follows the IrDA packet format defined in 5.4.2 of Infrared Data Association Serial Infrared Physical Layer Link Specification Version 1.2. [1]

2.2. Modulation Schemes

There are two modulation schemes of visible light communication of 4 Mb/s: inverted 4PPM and Manchester Code Data Modulation. Both schemes include DC offset to allow control of

illumination intensity. When a transmitter does not send any packet, idling packet which is synchronized with data packet is transmitted.

2.3 Consideration for Illumination

Visible Light Communication Physical Layer Specification must comply with requrements of illumination when visibile light source is used as an illumination device. It must consider parameters of illumination such as brightness, flickering, color rendering, etc. The physical layer specification must meet those requirements so that the data transmitter can be comfortably used as an illumination device.

2.4 Eye Safety Standards

Visible Light Communication Physical Layer Specification complies with CIE S 009/IEC 62471[4]. CIE S 009/IEC 62471 gives guidance for evaluating the photobiological safety of lamps and lamp systems including luminaries. Specifically it specifies the exposure limits, reference measurement technique and classification scheme for the evaluation and control of photobiological hazards from all electrically powered incoherent broadband sources of optical radiation, including LEDs but excluding lasers, in the wavelength range from 200 nm through 3000 nm.

3. Media Interface Description

3.1. Physical Representation

For a link operating at this specification, so-called 2R receiver should be employed to maintain proper timing margin. A block diagram of one terminal of such a link is shown in Figure 2. The Clock and Data Recovery (CDR) circuitry is placed between 1R receiver and interface [2b]. As output signal of the 1R receiver is analog but logic-level binary signal, the amplitude noises at its input are to be converted into timing jitters at its output in conjunction with all the other jitters. To suppress these jitters, it is necessary for the back-end to retime (latch) the 2R receiver's output signal by clock extracted from the output signal itself. Note that an actual "discrete CDR product" should be drawn at the right-hand side of the interface [2b] because it only outputs the retimed data and the recovered bit clock that are phase-aligned to the signal at TP3, which is associated with the other transducer-side clock domain.

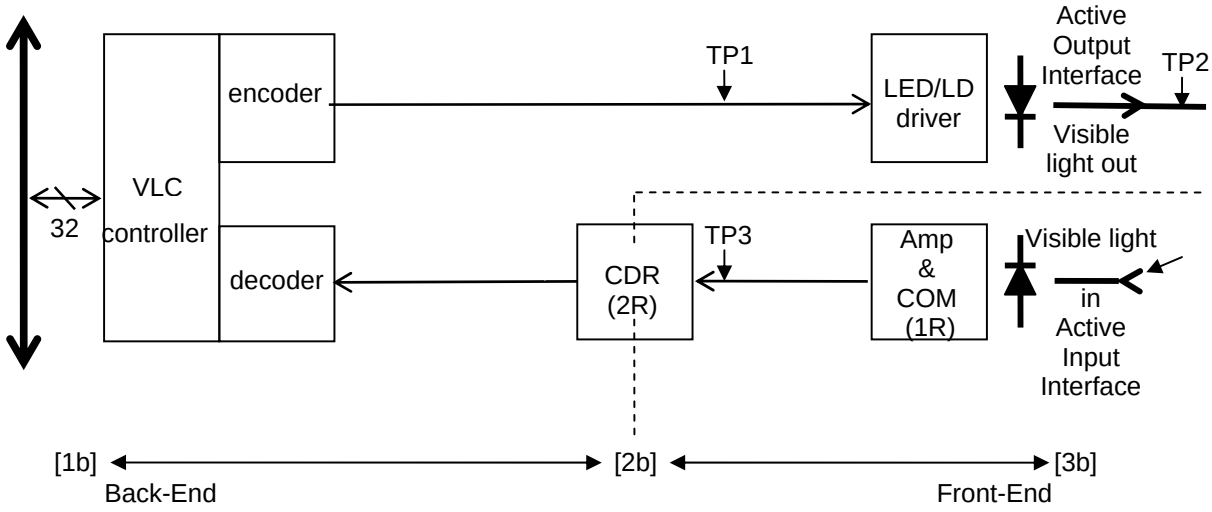


Figure 2 Visible Light Transducer Interfaces and Output/Input Test Points for 2R Receiver System including back-end example.

The most significant change in composition of the specification for 2R system is that a set of specification tables is provided. These tables individually list up the specification parameters for TP1, TP2 and TP3 in a later section. 4.4. TP2 is equivalent to Active Output Interface and TP2* is equivalent to Active Input Interface.

4. Media Interface Specifications

4.1. Overall Links

The Bit Error Ratio (BER) shall be no greater than 10^-8. The link shall operate and meet the BER specification over its range.

Signaling Rate and Pulse Duration:

Signaling rate and pulse duration specifications are shown in Table 1.

The maximum and minimum single pulse durations are the nominal 25% of the symbol duration plus and minus a tolerance of 2% of the symbol duration. For 4.0 Mb/s, minimum double pulse durations are 50% of the symbol plus and minus a tolerance of 2% of the symbol duration. Double pulses may occur whenever two adjacent chips require a pulse.

The link must meet the BER specification over the link length range and meet the optical pulse constraints.

Table 1. Signaling Rate and Pulse Duration Specifications

Signaling Rate	Modulation	Rate Tolerance % of Rate	Pulse Duration Minimum	Pulse Duration Nominal	Pulse Duration Maximum
4.0 Mb/s (single pulse) (double pulse)	Inverted 4PPM or Manchester Code Data Modulation	 +/-0.01 +/-0.01	 115.0 ns 240.0 ns	 125.0 ns 250.0 ns	 135.0 ns 260.0 ns

4.2. Active Output Interface

At the Active Output Interface, an optical signal is emitted. The specified Active Output Interface parameters appear in Table 2.

Table 2. Active Output Specifications

SPECIFICATION	Minimum	Maximum
Wavelength,, um	0.4	0.78
Signaling Rate (also called Clock Accuracy)	See Table 1	See Table 1

For a this specification , due to the introduction of Output/Input Test Points and jitter specifications, some parameters are specified in Section 4.4 (Test Point Specifications).

4.3. Active Input Interface

If a suitable optical signal impinges upon the Active Input Interface, the signal is detected, conditioned by the receiver circuitry, and output to the Receive Decoder. The specified Active Input Interface parameters appear in Table 3. This spec. is applied in the case of half angle width =30 degree.

Table 3. Active Input Specifications

SPECIFICATION	Minimum		Maximum	
	Manchester Code	I-4PPM	Manchester Code	I-4PPM
Minimum & Maximum Irradiance In Angular Range, uW/cm^2				
Wavelength 623-780nm	31.6	47.4	500000	
Wavelength 491-622nm	42.0	63.0		
Wavelength 400-490nm	63.0	94.5		
Receiver Latency Allowance, ms			10	

Note:
The maximum specification is defined for the point to point application.

There are no Active Input Interface Jitter specifications, beyond that implied in the Active Output Requirements. The link must meet the BER specification for all negotiated and allowable combinations of Active Output Interface specifications, except for non-allowed codes.

For this specification , due to the introduction of Output/Input Test Points and jitter specifications, most of the parameters are specified in Section 4.4 (Test Point Specifications). Only items that represent pure optical characteristics and/or overall link characteristics (at TP2*) are specified in Table 5. The receiver latency allowance is only appropriate for TP3 by its definition. The allowance shown in Table 5 is intended to limit 1R transceiver's overall settling time with both contributions from a transmitter (if it includes AC-coupling or power control feedback loop etc.) and a 1R receiver (typically, AGC and/or AOC/ATC consumes most of the period). See also Section 4.4.

Note:
Regarding Receiver Latency Allowance in Table 3, when 1R receiver is totally integrated with CDR as a "2R receiver", it should be enough that the BER requirements are met in the back-end under all of the TP2* specifications (i.e. Active Input Specifications).

4.4. Output / Input Test Points (TP1-TP3)

As described in section 3, the Output/Input Test Points have individual set of the parameters shown in Table 4.to 6. respectively.

4.4.1. Test Point 1 Specifications

Table 4. TP1 Specifications

SPECIFICATION	Symbol	Min	Typ	Max	Unit
Signaling Rate (clock accuracy)		7.9992 (-100ppm)	8	8.0008 (+100ppm)	MHz
Pulse Parameters: See A4.2					
Rise/Fall Time 10%-90%	Tr1/Tf1	1	-	25	ns

4.4.2. Test Point 2 Specifications

Table 5. TP2 Specifications

SPECIFICATION	Symbol	Min	Typ	Max	Unit
Signaling Rate (effective data rate)		-	4	-	Mbit/s
Eye-Mask Corner Parameters: See A4.2.					
X1	X1_2	-	15	-	%UI
X2	X2_2	-	30	-	%UI
Y1	Y1_2	-	25	-	%pp
Y2	Y2_2	-	20	-	%pp

Note:
The eye-mask corner parameters {X1,X2,Y1,Y2} are specified in a row representing “Typ” value, however, note that these parameters just set the corners in the eye-mask violation test. Do not confuse them with normal usage of the term “typical” as a lot-average or a measurement-average etc.

4.4.3. Test Point 3 Specifications

Table 6. TP3 Specifications

SPECIFICATION	Symbol	Min	Typ	Max	Unit
Signaling Rate (effective data rate)			4	-	Mbit/s
Pulse Parameters: See A4.2					
Rise/Fall Time 10%-90%	Tr3/Tf3	1	-	25	ns

5. Modulation and Demodulation

5.1. Scope

This section covers data modulation and demodulation at 4Mb/s data rates. The 4Mb/s rate uses Inverted Four pulse position modulation (PPM) and Manchester Code Data Modulation scheme. This specifies packet format, data encoding, cyclic redundancy check, and frame format for use in communications systems based on the optical interface specification.

5.2. Encoding

There are two modulation schemes of visible light communication of 4 Mb/s.

- Inverted 4PPM(I-4PPM)
- Manchester Code Data Modulation.

5.3. Packet Format Definition

5.3.1. I-4PPM

A PPM Packet format was defined for a specification of Infrared Data Association Serial Infrared Physical Layer Link Specification.
For details, refer to the Infrared Data Association Serial Infrared Physical Layer Link Specification Vertion1.2[1].(5.4.2: PPM Packet Format)

5.3.2. Manchester Code Data Modulation

5.3.2.1. Packet Overview

For Manchester Code Data Modulation packets the following packet format is defined as shown in Fig.3.

A byte order is the LSB first.

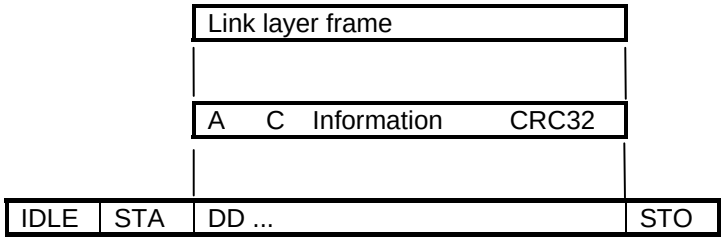


Figure 3. Packet format,

In this packet format, the payload data is encoded as described in the Manchester Code Data Modulation encoding above, and the encoded symbols reside in the DD field. Maximum packet length is negotiated by the same mechanism as for the slower rates. The Idle field is used by the receiver to establish the phase locked state. During Idle, the receiver begins to search for the start flag (STA) to establish symbol synchronization. If STA is received correctly, the receiver can begin to interpret the data symbols in the DD field. The receiver continues to receive and interpret data until the stop flag (STO) is recognized. STO indicates the end of a frame. The chip patterns and symbols for IDLE,STA, FCS field, and STO are defined below. Only complete packets that contain the entire format defined above are guaranteed to be decoded at the receiver (note that, as for the lower rates, the information field, I, may be of zero length).

The Manchester Code Data Modulation encoding described above defines only the legal encoded payload data symbols. All other 4 chip combinations are by definition illegal symbols for encoded payload data. Some of these illegal symbols are used in the definition of the idle,start flag, and stop flag fields because they are unambiguously not data.

5.3.2.2. Start Flag Definition

Start flag is constituted by the following 32-bit patterns as shown in Fig.4

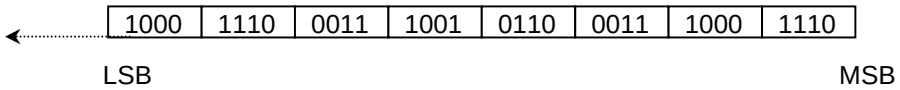


Figure 4 Start Flag

5.3.2.3. Stop Flag Definition

Stop flag is constituted by the following 32-bit patterns as shown in Fig. 5

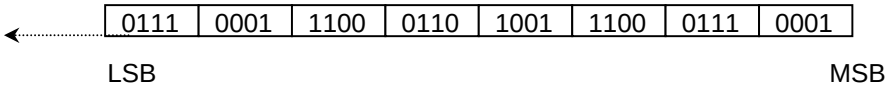


Figure 5 Stop Flag

5.3.2.4. Frame Check Sequence Field Definition

A 32-bit CRC calculation and the CRC bit order remain unchanged from which was defined for a specification of Infrared Data Association Serial Infrared Physical Layer Link Specification.

For details, refer to the Infrared Data Association Serial Infrared Physical Layer Link Specification Vertion1.2. [1] (5.3.2.5: Frame Check Sequence Field(FCS) Definition)

5.3.2.5. Back to Back Transmission Packet

Back to Back, or "brick-walled" packets are allowed, but each packet must be in a complete frame format (i.e., containing , STA, DD Frame, CRC and STO fields).

5.4. Idle

The Idle field is used by the receiver to establish the phase locked state. During Idle, the receiver begins to search for the start flag (STA) to establish symbol synchronization as shown in Fig.6

The idle signal is filled for non-packet period. The idle Signal should be consecutive by 32 bits or more.

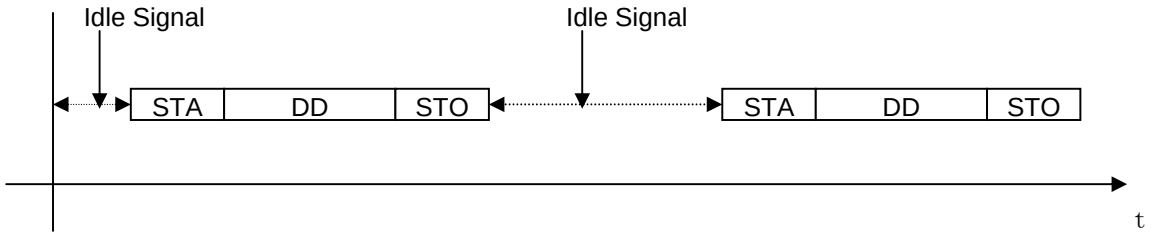


Figure 6 Idle

5.4.1. Idle Signal Definition

The idle signal consists of exactly of the repetition of four transmissions of the following stream of symbols.

5.4.1.1 I-4PPM

In the idle signal, transmission time increases from left to right so that symbols on the left are transmitted first as shown in Fig.7

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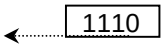

Figure 7. Idle signal format

5.4.1.2 Manchester Code Data Modulation

In the idle signal, transmission time increases from left to right so that symbols on the left are transmitted first as shown in Fig.8

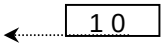

Figure 8 Idle signal format

6. Visible light connection control flags (Manchester Modulation Additional)

The first byte posisiton of payload is reserved for visible light connection control flags.
These flags defined physical characteristics and link methods of visible light connections.

6.1 Details of Visible light connection control flags (VLF)

The follwing table describes bit assignment of visible light connection capability flags.

Bit Posision	Flag Nemonic	Detiles
0	VLF_BLOADCAST	Bloadcasting data 1 / Bidirectional 0
1	VLF_ COLORED	Color channel enable 1 / Egnore color 0
2-3	VLF_OWN_COLOR	Define sender own color (See Next Table)
4-7	VLF_COLOR_CHANNEL	Used color channel (See Next Table)

6.1.1 Details of VLF_COLOR_CHANNEL

The follwing table describes bit assignment of color channel capability flags.

Bit Posision		Flag Nemonic	Detiles
2	3		
0	0	VLF_SEND_CL_CHAN_0	Sending data is used by color channel 0 (RED)
1	0	VLF_SEND_CL_CHAN_1	Sending data is used by color channel 0 (GREEN)
0	1	VLF_SEND_CL_CHAN_2	Sending data is used by color channel 0 (BLUE)
1	1	VLF_SEND_CL_CHAN_3	Reserved not use

6.1.2 Details of VLF_COLOR_CHANNEL

The follwing table describes bit assignment of color channel capability flags.

Bit Posision	Flag Nemonic	Detiles
4	VLF_CL_CHAN_0	Pure Red channel using
5	VLF_CL_CHAN_1	Pure Green channel using
6	VLF_CL_CHAN_2	Pure Blue channel using
7	VLF_CL_CHAN_3	Reserved must set 0

6.1.3 Details of color channel wave length assignments

The follwing table describes bit assignment of color channel capability flags.

Bit Posision	Flag Nemonic	Peak wavle langth
4	VLF_CL_CHAN_0	Pure Red 700.0nm
5	VLF_CL_CHAN_1	Pure Green 546.1nm
6	VLF_CL_CHAN_2	Pure Blue 435.8nm
7	VLF_CL_CHAN_3	Reserved must set 0

Appendix A. Test Methods

A.1. Active Output Specifications

A.1. 1. Peak Wavelength

The peak wavelength (Peak Wavelength, Up, um) is the wavelength of peak intensity and can be measured using an optical spectrum analyzer. The pulse shape and sequence can be the same as that used for the power measurements below and the measurement can be made on the optical axis.

A.2. Active Input Specifications

The following two specifications form a set which can be measured concurrently:
- Bit Error Ratio, (BER)
- Receiver Latency Allowance, ms

These measurements require BERs. Since the optical power source must provide the specified characteristics of the Active Output, calibration and control of this source can use the same equipment as that required to measure the intensity and timing characteristics. BER measurements require some method to determine errors in the received and decoded signal. The latency test requires exercise of the node's transmitter to condition the receiver. Definitions of the reference point, etc., are the same as for the Active Output Interface optical power measurements except that the test head is now an optical power source with the in-band characteristics (Peak Wavelength, Rise and Fall Times, Pulse Duration, Signaling Rate and Jitter) of the Active Output Interface. In addition the maximum level of light is depend on an application.therefore the maximum level of power is not defined by this Specification. It is expected that the minimum levels can be attained by appropriately spacing the optical source from the reference point.
The receiver is operated throughout the Active Output region and BER measurements are made to verify the maximum and minimum requirements. The ambient conditions of A.1 apply during BER tests; BER measurements can be done with worst case signal patterns. Unless otherwise known, the test signal pattern should include maximum length sequences of "1"s (no light) to test noise and ambient, and maximum length sequences of "0"s (light) to test for latency and other overload conditions.

Latency is tested at the Minimum Irradiance in Angular Range conditions. The receiver is conditioned by the exercise of its associated transmitter. The receiver is operated with the minimum irradiance levels and BER measurements are made after the specified latency period for this equipment to verify irradiance, half-angle, BER and latency requirements.
The test methods for these two specifications are not defined here, but separately defined for each Test Point in Output/Input.

A.3. Output/Input Test Points Specifications

A.3.1. Background

One should distinguish the following specification classes, depending on whether testing jitter or eye-opening specifications as a link component (class [I]), or testing CDR and BER performance (class [II]). These specification classes are summarized in Table 7 to show their purposes and guideline for the test methods.

Table 7 Summary of Test Point Specifications and the Test Methods.

Specification Class		Item	TP# to be tested	Test Methods	
				Test Bit Sequences (See A3)	Irradiance (See text)
[I]	Pulse Parameters and Eye Diagram	Rise/Fall Time	*TP1*	Pseudorandom Binary (Bit) Sequence	--
			TP3	PRBS2^{15}-1	--
		Eye-Mask Violation	*TP2*	$X^{15}+X^{14}+1$ ITU-T O.151	--
[II]	CDR and BER	BER (irrad.dep.)	[See A3.3.4]		@ {m} @ {T*} @ {M}

A.3.2. Eye diagram

Eye mask violation is only specified and tested at TP2. For the other test points than TP2, the signals are all electrical and they are one of the existing binary I/O logic families, e.g. LVTTL, LVPECL, LVDS etc. The measurements should be done through the same DC-coupled high-speed O/E converter. As wide-band frequency response is necessary, the O/E converter may suffer from low input SNR. Then, eye mask violation could happen due to the random noises. In this measurement, however, it is not allowed to let the oscilloscope operate in averaging mode. Further electrical amplification in O/E converter may be required.

The eye diagram should be derived by the method described in the later section A.3.3. The Test Bit Sequence should be used shown in Table 7. This test bit sequence is simple but moderately stressful to examine if DUT is ISI-dominated. The template of the Eye Mask is shown in Figure 9 Eye mask violation is declared if any trace in eye diagram invades any region defined as “Not allowed”. A set of corner parameters, {X1, X2, Y1, Y2}, is specified in Tables 7. 1UI is already specified in Table 1 as Pulse Duration. {Y1, Y2} is defined as a normalized value to the peak to peak optical amplitude that should meet Active Output specifications in Table5, if scaled properly. The rise/fall time measurement in A3.1 may be used to determine these 0% and 100% levels.

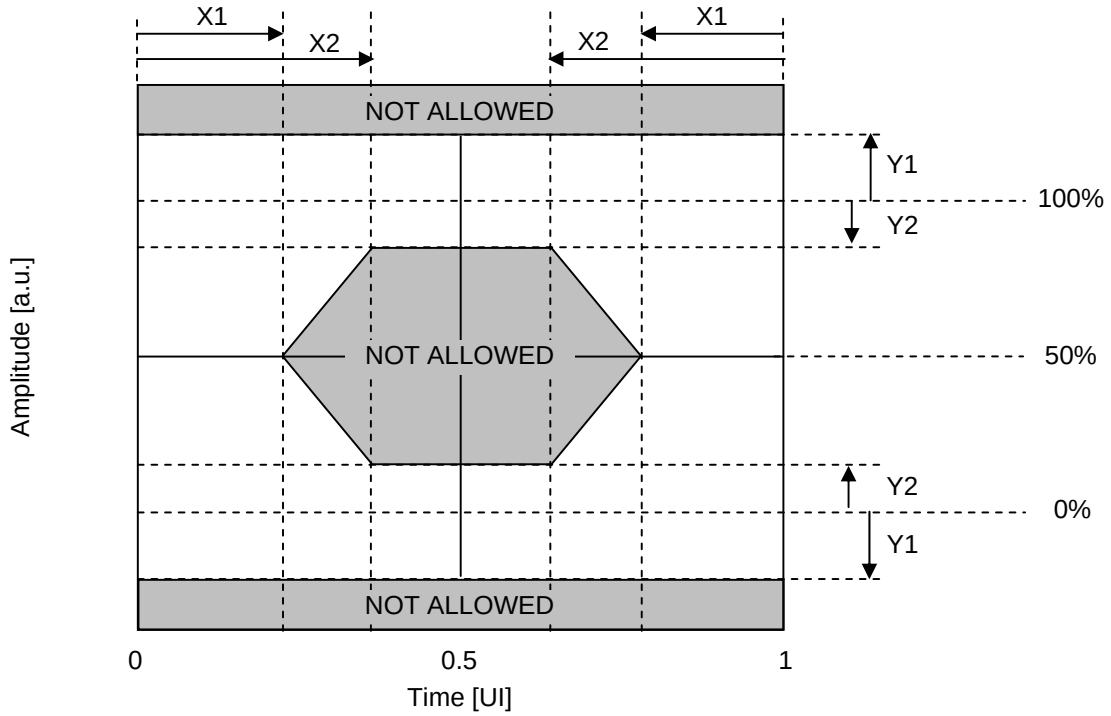

Figure 9. Eye Mask Template

Note:

The template in Figure 9 can represent various sources of jitters, noises or distortions. However, the eye mask is intended to define the limits of signal waveforms such as overshoot, undershoot, ringing and its envelope, excessive baseline wander, non-linear tailing or distortions etc, all of which are deterministic. Because combinations of these phenomena (in conjunction with duty cycle distortion) can not be revealed at a certain temporal point or amplitude, but can only be examined through the eye masks. Therefore, the eye masks are not to be used for determining compliance with the rise/fall time and the jitters.

A.3.3. Definition of Jitter Output and Eye Opening (Reference)

Jitter output and eye opening are measured at all the Test Points. It should be noted that there are two definitions for the jitter output. The term “Incremental Jitter” is referred to the jitter that is incurred by a link component such as {LED/LD+driver} or 1R receiver etc. The term “Accumulated Jitter” is referred to the jitter that is accumulated through two or more adjacent test points (or link components, equivalently), which is especially important when the link itself is under test.

It may be controversial how to exactly de-convolve the “measured” Incremental Jitter down to the individual jitter component’s contributions. And it may also be controversial when the “measured” accumulated jitters have been convolved so that one cannot find any good correlation between the associated “incremental” jitters and the “accumulated” jitter. Based on

the experiments reported at the SIG (Special Interest Group) and the following conceptual descriptions in A.3.3.1 – A.3.3.2, recommendations will be made to deal with these concerns.

The worst case “reduction”, as briefly described in A.3.1, makes it possible to define the simple jitter specifications.

A.3.3.1. TIE (Time Interval Error) Analysis

In any jitter-related tests for link components, the measurements should be based on the TIE analysis with “Edge-to-Reference” approach to avoid any confusion. The edges are to be defined at a mid-point of peak-to-peak amplitude, not at a cross-point of the eye diagram, as shown in Figure 10. When differential electrical signal is under test, jitter measurements should be done for a difference between the two complementary signals, i.e. mathematical waveform subtraction is required. It can be properly done by making use of differential active probe and then TIE analysis is done for the 0-crossing events.

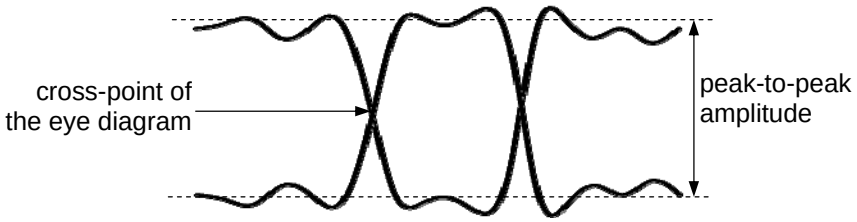

Figure 10 The definition of the waveform edges

The Edge-to-Reference approach takes account of the data edge’s deviations from the corresponding ideal reference edges, provided that such an accurate bit clock is available. There are two recommendable ways to derive such “reference edges” for arbitrary data stream:

1) To use PPG (Pulse Pattern Generator) having relatively high specifications to generate both bit clock and input test signal.
2) To apply a “find bit rate” like least-square fitting to the data stream, assuming a purely single frequency bit clock (as a Dirac delta function) has been embedded without any time-variant phase deviations throughout the data stream. Apparently, this strategy also relies upon an accurate enough PPG to make the assumption.

For both cases, the PPG should have an overall resolution/accuracy of finer than 10mUI along the whole period of test bit sequence. The accuracy and the stability of the generated bit clock and data signal crucially influence the acquired TIE trend along a long time period.

On the other hand, as for the oscilloscope to be used in the jitter measurement/analysis in this section, digital sampling oscilloscope (DSO) or digital real-time oscilloscope (DRTO) would be the most suitable choice. These apparatus provide various types of TIA (Time-Interval Analysis) with various ways to provide (ideal) clock edges internally or externally. However, all the necessary and enough functions in this section are (see also A.3.3.2):

* {Rj_effective, Dj_effective} extraction from TIE histogram
* Tj extraction for BER equal to 1E–8 from TIE histogram
* One more input channel for bit clock signal which is simultaneously generated by the same PPG to generate source data signal.
* Wide and fine skew control between the input channels to absorb low-frequency time-base fluctuations within the PPG outputs. A large skew between the bit clock signal and the data signal (by cables, amplifiers etc) involves such fluctuations in the acquired TIE trend because the two signals loose temporal correlation if far away each other.

The other functions, e.g. decomposition or extraction of various types of deterministic jitter or power spectrum analysis, are not actually needed for the specifications (but may be useful for diagnosis) because the significant or crucial jitter components/sources are already known for the “reduced” worst case conditions.

Thus, we would take the simpler methodology as briefly described in section A3.1. To this end, some important aspects should be kept in mind when one would refer to the rest of this section:

* The measurements should be done in a “single-shot” manner, including a sufficient number of transition events by using a certain TBS (Test Bit Sequence). It should be allowed to repeat the single shot measurement to increase the number of transition events. But it should not be done “periodically continuously” because transient or settling behavior of the jitter is of strong interest.
* Transition edges in the acquired data signal must be fully captured. Otherwise, statistical distribution of the TIE histogram will be very different from the original one. Therefore, regardless of the jitter amplitude in the data signal, one should always take care that there are no “extra pulses” (or logic-level glitches) and no “full-bit disappearances” in a unit test bit sequence. This kind of check is impossible just by looking at the acquired eye diagram, and is somehow possible by carefully looking at the TIE trend. It will be nice to make use of the original data source for such wrong event mapping.
* When TIE histogram is acquired over hundreds of microseconds or more, one should take care of another risk. In poor test environment, local thermal fluctuation and/or electrical noises etc. may disturb a source (internal) oscillator and its associated PLL that stabilize and guarantee the “time base” of PPG and DRTO. In principle, relative deviation of the “time base” between PPG and DRTO is directly convolved into the TIE trend if it is faster than PLL response in DRTO. To examine this issue, consider a TIE trend for data and bit clock that are simultaneously generated by PPG is acquired by “independently running” DRTO. After a sufficient period of warm-up has been done, if any long term fluctuation or drift is observed, one should try to synchronize source oscillators in the PPG and the DRTO each other. These apparatuses are usually equipped with input and output ports for "external reference clock". They can be synchronized easily if both of the frequencies are in common.

* Finally, in the jitter-related measurements, it should be avoided to use any types of PLL for the purpose of cleaning up clock (triggering) jitters or recovering bit clock from data signal. If PLL is used, the resultant incremental jitters for components having different design strategies would be very much dependent on the setups, even though frequency response of the PLL is strictly specified and matched in every testing. This is because, especially for TP3, the origins or nature (distribution) of the jitter output may strongly depend on the individual DUT's. Such details are absolutely unknown prior to the actual measurements even if typical and/or worst-case characteristics are well-described in their datasheet. Therefore, in this document, the jitter-related specifications/measurements are all intended to reveal the "raw jitter characteristics" of the DUT (front-end device) by avoiding use of PLL in TIE analysis.

A.3.3.2. Total Jitter Output (Eye-Opening)

Once TIE histogram is derived from the data stream under test, the most basic analysis is to extrapolate the both extremes of the distribution. If some mathematical models can be used to describe the extremes (or tails), the analysis yields a probability distribution function (PDF) of the measured jitters as a continuous function of time in Unit Interval (UI), but only valid around the tails. By consistently scaling both the tail PDF's and the TIE histogram along a common set of bins, one can estimate a cumulative distribution function (CDF) of the original TIE histogram as normalized integral from both sides to the center of the estimated (tail-fitted) PDF. By arranging the plot for UI-axis, it is also called a "bathtub curve". Then, one can estimate "confidence limits" in which any edge-transition will never occur beyond a specific probability (as a BER). The full width of the confidence limits is total jitter, Tj, at that specified BER.

The most popular and realistic tail model is a Gaussian distribution. So-called "effective" method is one of the simplest ways to decompose the jitter histogram into either "random" or "deterministic" component. It is already included in the above-mentioned process. That is, the TIE histogram is least-square-fitted by two Gaussian distributions around the both tails with an assumption that the two Gaussians are separated

by Dj_effective. Rj_effective is derived from a sum of the standard deviations of each Gaussian. By definition, Tj = Rj_effective + Dj_effecvtive at the specified BER. Note that a small letter "j" is used to express "elementary" jitter component derived in each TIE analysis. On the other hand, a capital letter "J" is used for the Jitter value that should meet the specifications in this document such as: Random Jitter RJ, Deterministic Jitter DJ and Total Jitter TJ. For example, at test point k, TPk, after some measurements done under various conditions, the worst case value among the resultant set of {Dj_eff} is reported as a DJ. And if it is "incremental" or "accumulated", it is denoted as iDJ_k or aDJ_k, respectively.

Although the extraction of Rj_effective, Dj_effective and Tj is a necessary and enough TIA function as described in A3.3.1, the other decomposition methodologies can be complementally used. As long as the measured tails are well-described by Gaussian, resultant Tj's won't depend on the methodologies at the same BER, however, the worst value among the elementary jitter components should be reported. The Total Jitter, TJ to be reported is defined as the sum of RJ and DJ, analogous to the elementary jitters, but in this case the RJ and the DJ are derived from individual measurements as described above. The Total Jitter, TJ is basically the most useful parameter applicable to any situation where various jitters are convolved in the TIE histogram. The eye-opening is defined as {1–TJ} in [UI] at the specified BER.

A.3.3.3. Consistency between Eye-opening and BER

In this sub-section, it is described how to maintain consistency between the eye-opening (tested by transceiver suppliers before shipping) and the BER (tested by controller suppliers, set makers or test labs. after a board implementation).

As described in A.3.3.1, frequency spectrum of the jitter is not explicitly specified, but it is implicitly embedded in the test bit sequences. Besides, in actual measurements, no PLL is assumed to be in the signal path such that one can capture all frequency components of the raw jitter output from DUT. This methodology leads to simpler interoperability test, but may be rather conservative and severe for the analog components from a view point that all the low frequency jitter components should be suppressed to less than a unique, frequency-independent value of the Total Jitter Allowance. However, by setting it moderately conservatively, these PHY specifications guarantee that a link meets the BER specification

without executing BERT measurements for any combination of the worst case link components. (Instead, the Total Jitter Allowance and the Jitter Tolerance would never predict the BER for individual links.) It should also be noted that the most significant merit of this methodology appears in ensuring this PHY specification supporting 32kB-long packet (~2ms long) or any multiple-window frames without any ambiguity as long as the system clock accuracy of Tx-side and Rx-side both stays within its specification.

Finally, this PHY specification does not specify the output characteristics of CDR but the input characteristics only. As a result, the Jitter Tolerance of CDR is to be specified as an input characteristics of the controller IC's. This is because, to examine BER of a link, some gluing function between different clock domains, i.e. CDR and the following back-end logic, is necessary. It is supposed that these elements be all integrated in a PHY (controller) chip. Therefore, by taking account of the jitter transfer/generation characteristics of the CDR, and by using actual controller chips, the controller suppliers (or set makers if CDR is implemented as a discrete component in their own design) should be responsible for examining if the specified Total Jitter Allowance, i.e. the specified Jitter Tolerance is enough to meet the BER specification of 10^{-8}.