Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: NICT Phy Solution: Part 1: Chirp Pulse Based IR-UWB Physical Layer
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Abstract: Chirp Pulse Based UWB Physical Layer Proposal for Body Area Networks

Purpose: Response to "TG6 Call for Proposals" (IEEE P802.15-08-0811-02-0006)

NICT Phy Solution: Part 1: Chirp Pulse Based IR-UWB Physical Layer

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Outline

- Motivation
- System principles
- Choosing system parameters
- System performance
- Conclusions

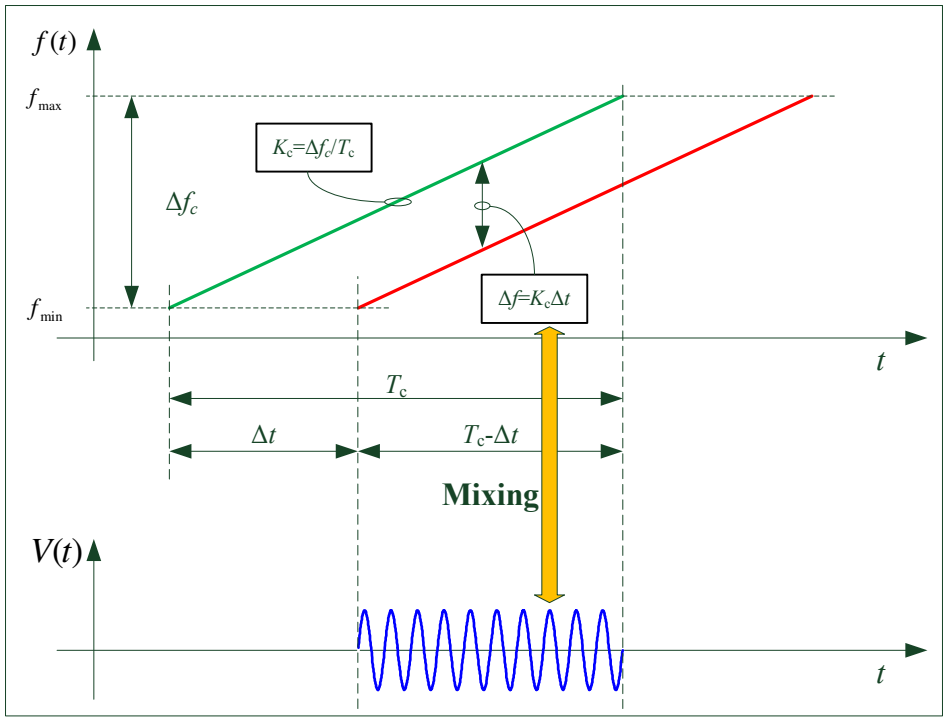
Motivation

- IR-UWB is a (strong) candidate for wearable BAN.
- Low power non-coherent IR-UWB systems are sensitive to MAI, NBI and interference from other IR-UWB.
- Systems that are aspiring to be low power (differentially) coherent IR-UWB are still emerging and make significant compromise between system performance and power consumption.
- Is it possible to design a system that is coherent, performs close to the full Rake receiver and is low complexity and low power?

SYSTEM PRINCIPLES

Why is linear chirp pulse signal like no other?

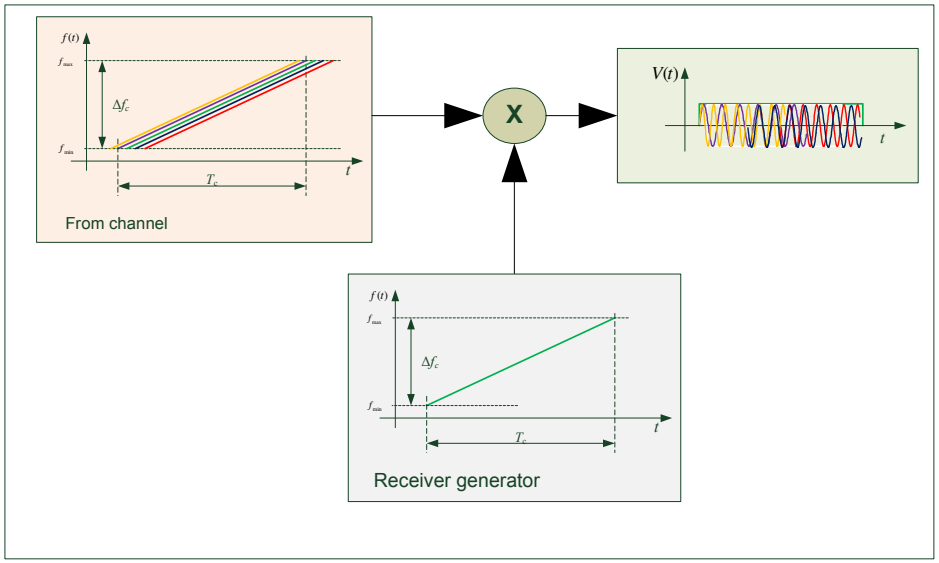
Mixing two linear chirp pulses:

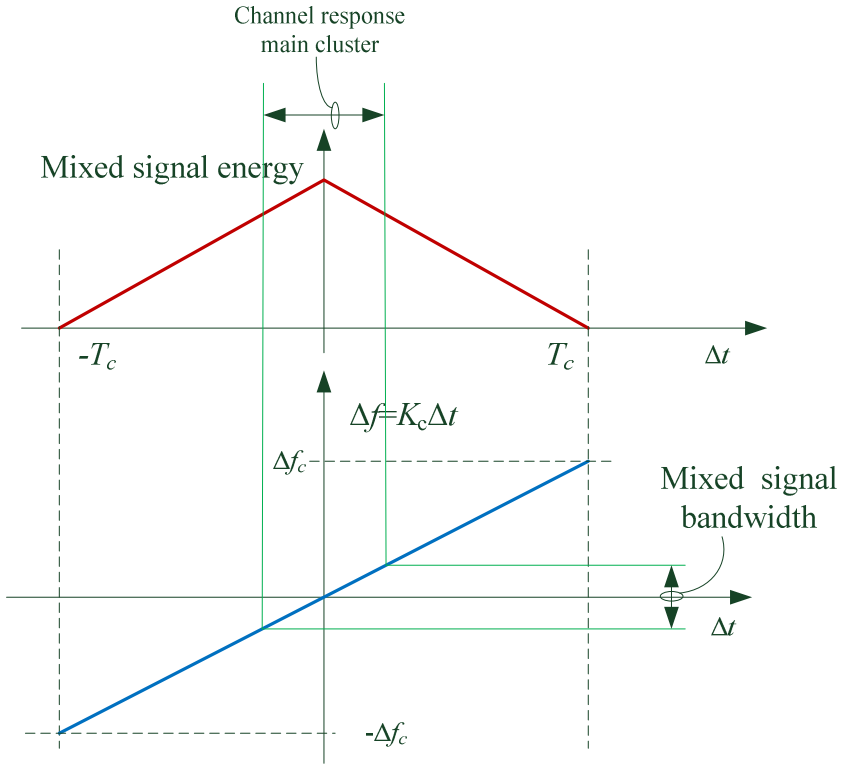


- **It de-spreads the chirp in frequency without de-spreading it in time.**
- Timing does not to be matched well in order to get low-pass signal that contains most of the energy.

Why is linear chirp pulse signal like no other? (cont.)

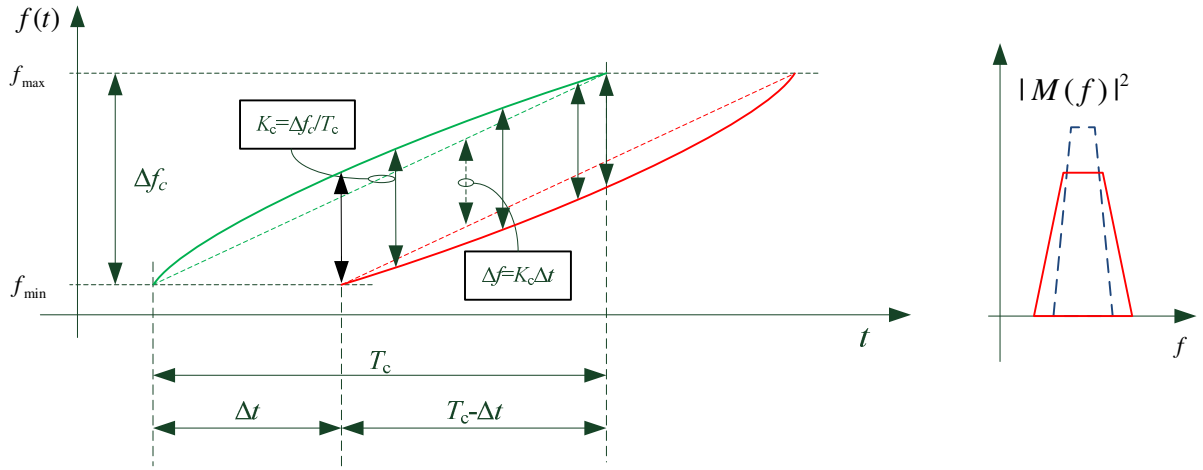
Effects on multipath:





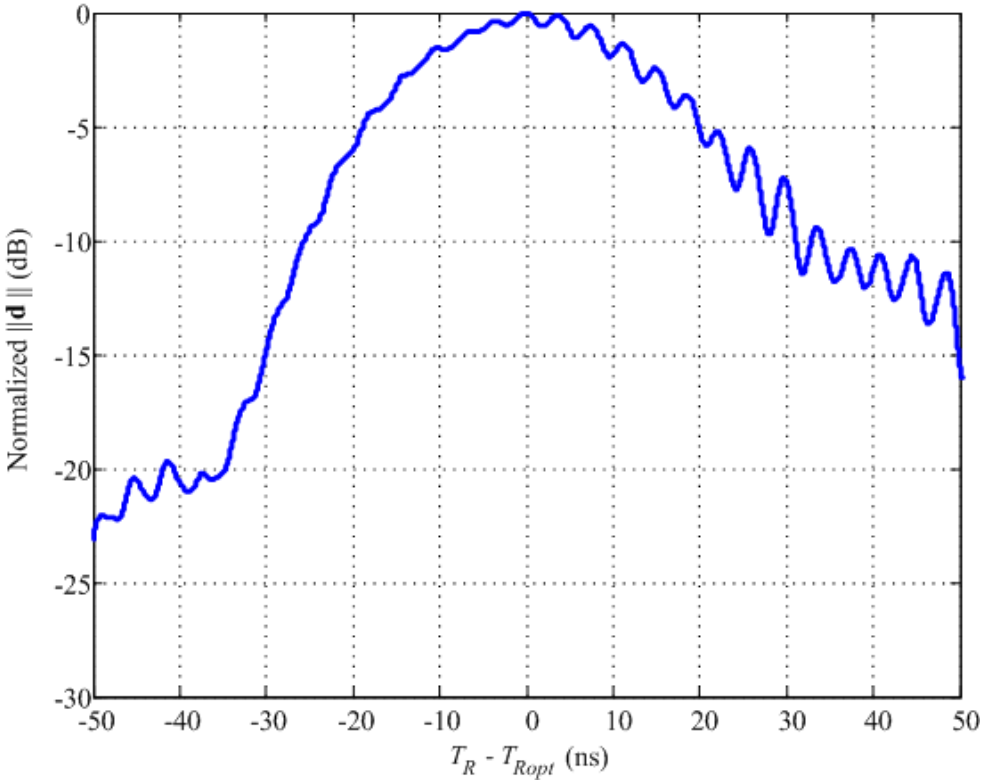
With proper choice of chirp parameters, for a given channel and optimum timing, energy of the multipath signal will be mostly preserved after mixing and concentrated in low frequencies where it ca be conveniently sampled.

Chirp pulse generation non-idealities robustness rationale



- Non-idealities in chirp generation:
  - Non-linearity and offset in chirp slope (Kc), carrier frequency offset, as well as phase and amplitude modulations encountered in the channel widen the spectra of tones after mixing.
  - There is no need to have very good match in carrier frequency in order to achieve phase coherence.

Timing resolution relaxation rationale

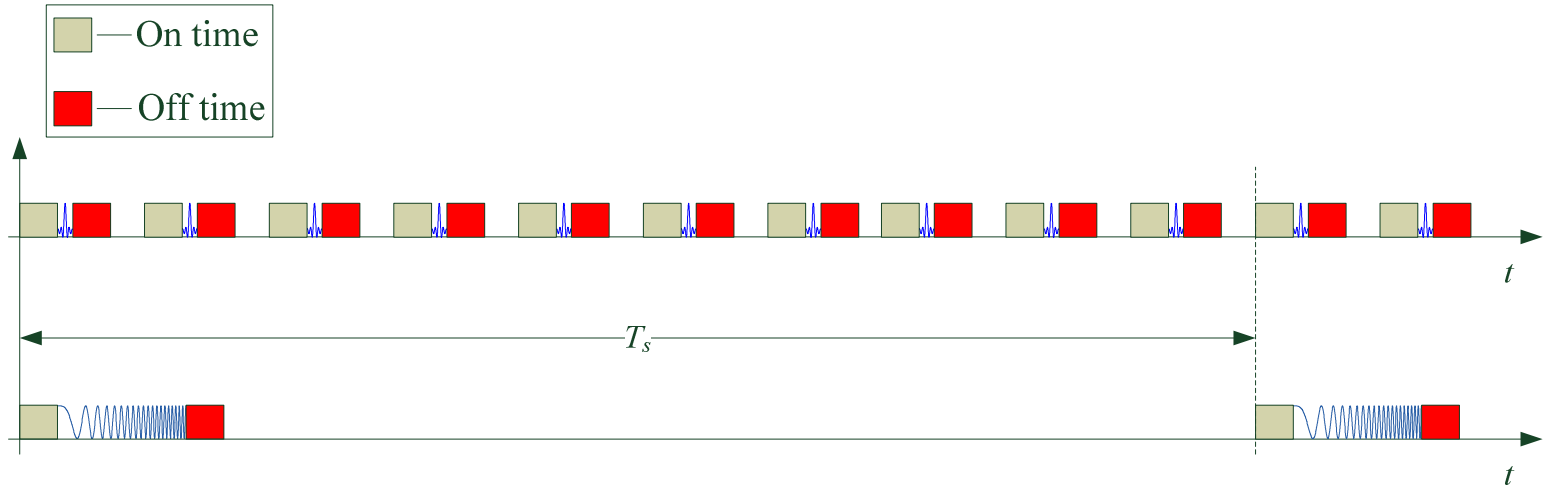


In the worst case scenario (single path), power in the digital portion of the system varies $\sim \Delta T_R / T_c$

In equivalent differentially coherent IR-UWB system with short pulses power would vary $\sim \Delta f_c \Delta T_R$

Timing resolution necessary is relaxed TB product of the used chirp pulse times.

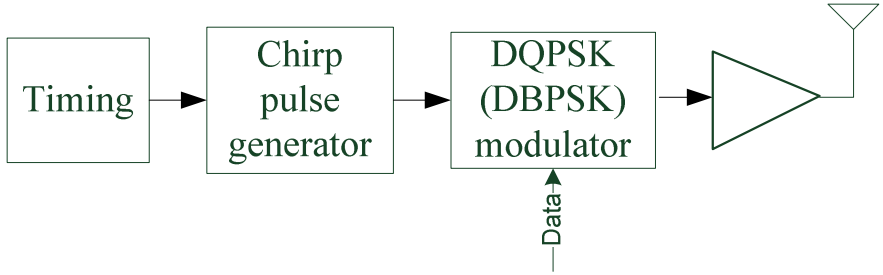
Duty cycling (power saving) rationale



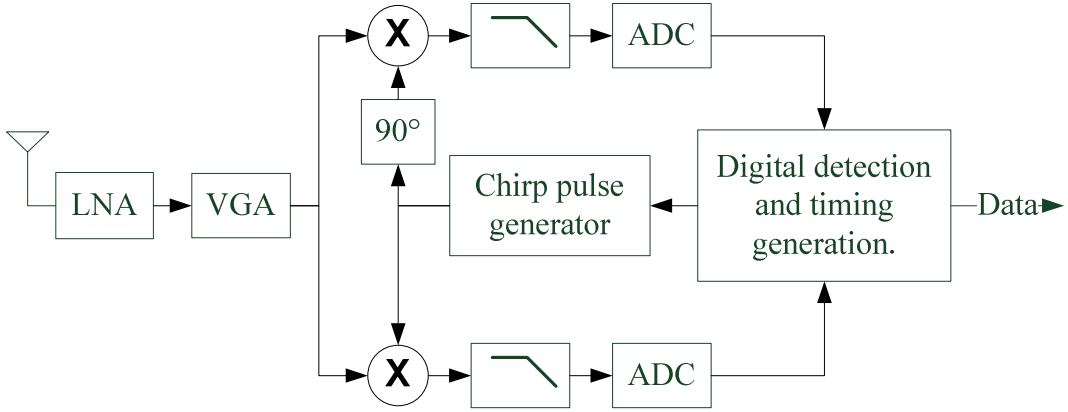
- Duty-cycling is facilitated, both in Tx and Rx, through emitting symbols that consist of single long packet of energy instead of series of isolated short pulses.
- Chirp pulse generator (founded both in Tx and Rx) is inherently duty cycled since it works in pulse regime.
- System is not peak-power limited but RMS power limited, which allows higher EIRP.

System block diagram

- Tx:



- Rx:



Notes on the system architecture

- System uses differentially phase modulated linear chirp pulses with relatively high TB product as symbols. Each pulse represents one symbol (symbol = 1 chip), except for lowest data rates when symbol consists of 2-4 chips.
- Receiver is Quadrature Analog Correlating (QAC) receiver (in specific configuration) found in both non-coherent and coherent IR-UWB solutions.
- Chirp generator is basically VCO with relatively linear tuning curve that works in pulse regime with linear ramp excitation (This technique of generation of chirp pulses is based on mature UWB VCO technology).

Digital detection methods

- There are two symbol detection methods that are considered.

1. **Ordinary DPSK detection**. i.e. “Symbol-wise DPSK”.
2. **“Digitally Differential Phase Shift Keying (DDPSK)”** i.e. “Sample-wise DPSK”. (Suboptimal, but does not require any channel vector estimation.)

Ordinary DPSK detection

- Symbols samples are, first, approximately match filtered:

$$b_k = \hat{\mathbf{d}}^H(T_R)\mathbf{s}_k(T_R)$$

- Then, transmitted symbol is estimated in the following manner:

$$\hat{\beta}_k = \angle\left(b_{k-1}^* b_k\right) - \hat{\varphi}_d .$$

- This technique also requires estimation of the channel vector $\hat{\mathbf{d}}(T_R)$

- Timing drift complicates channel estimation, since it causes continuous change of the channel vector itself.
- Ideally, this technique yields performance that is equal to theoretical one for DPSK.

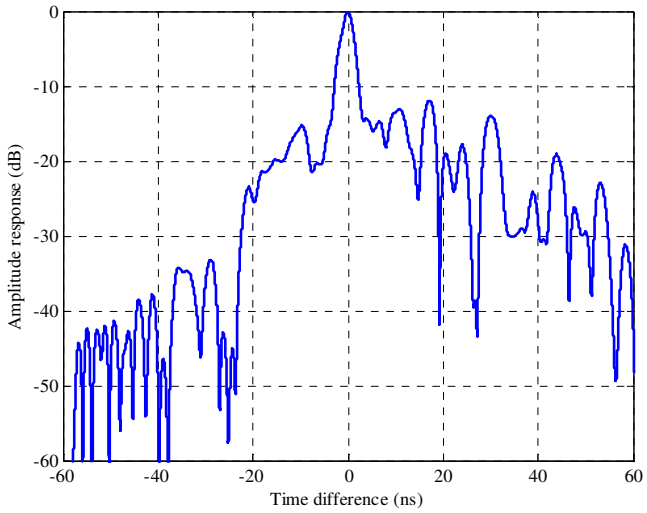
"Digitally Differential Phase Shift Keying (DDPSK)"

- Two consecutive symbols are correlated in the digital domain to produce phase difference estimate: $\hat{\beta}_k = \angle\left(\mathbf{s}_{k-1}^H(T_R)\mathbf{s}_k(T_R)\right) - \hat{\varphi}_d$

- DDPSK does not require any channel vector estimation.
- DDPSK is suboptimal compared to the DPSK.

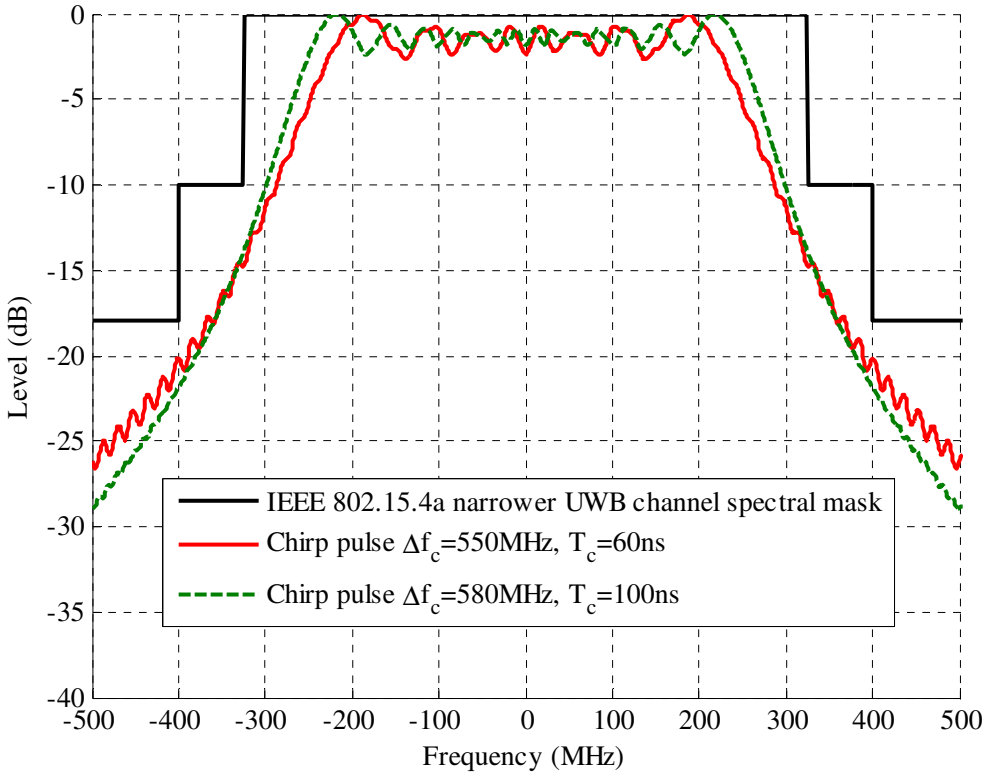
Time hopping

- During synchronization process there is no time hopping.
- During PSDU, system uses first half of time slots to avoid ISI.



CHOOSING BASIC SYSTEM PARAMETERS

System bandwidth



• The system uses chirp sweep of 550 MHz in order to fit with high efficiency to narrower IEEE 802.15.4a spectrum mask of about 600 MHz.

• Band plan is to use all narrower IEEE 802.15.4a channels.

Pulse duration (T_c).

- It is a tradeoff between low duty cycle and system multipath performance.
- Extensive simulation on IEEE 802.15.6 channels and IEEE 802.15.4a channel showed:
  - Chirp pulse duration higher than about 60ns does not significantly improve multipath performance.
  - Depending on the channel investigated, system with around 60ns pulse is able to coherently gather 0.5 – 3 dB short of all multipath energy (full Rake receiver).
- Decided to use IEEE 802.15.4a time frames as chirp pulse durations (same crystal resonator is planed):

T_c	Multipath performance
64 ns	0.5 – 3 dB under full Rake receiver.
32 ns	.5 – 1.5 dB under 64ns pulse.
16 ns	.5 – 1.5 dB under 32 ns.
12 ns	.3 dB under 16 ns.

Rx sample rate and resolution.

- We propose using receiver with 2 bits, 8-12 samples per pulse, since:
  - More than about 8-12 samples per pulse does not improve performance significantly.
  - 3 bits sampling performs near to ideal sampling, 2 bits sampling performs about 2 dB below, while 1 bit sampling is 4-6 dB below to 2 bit.

Chirp pulse generation tolerances.

- Chirp slope error of 30% is acceptable
- Central frequency error of 100 MHz is still acceptable.
- 30% Non-linearity still acceptable.

Proposed data rates

Raw data rate (Mbps)	Pulse duration (ns)	Modulation type	Number of chips per symbol	Chip rate (Mcps)
0.245	64	DBPSK	4	.98
0.49	64	DBPSK	2	.98
.98	64	DBPSK	1	.98
1.96	64	DQPSK	1	.98
1.96	32	DBPSK	1	1.96
3.92	32	DQPSK	1	1.96
7.80	16	DQPSK	1	3.90
10.40	12	DQPSK	1	5.20

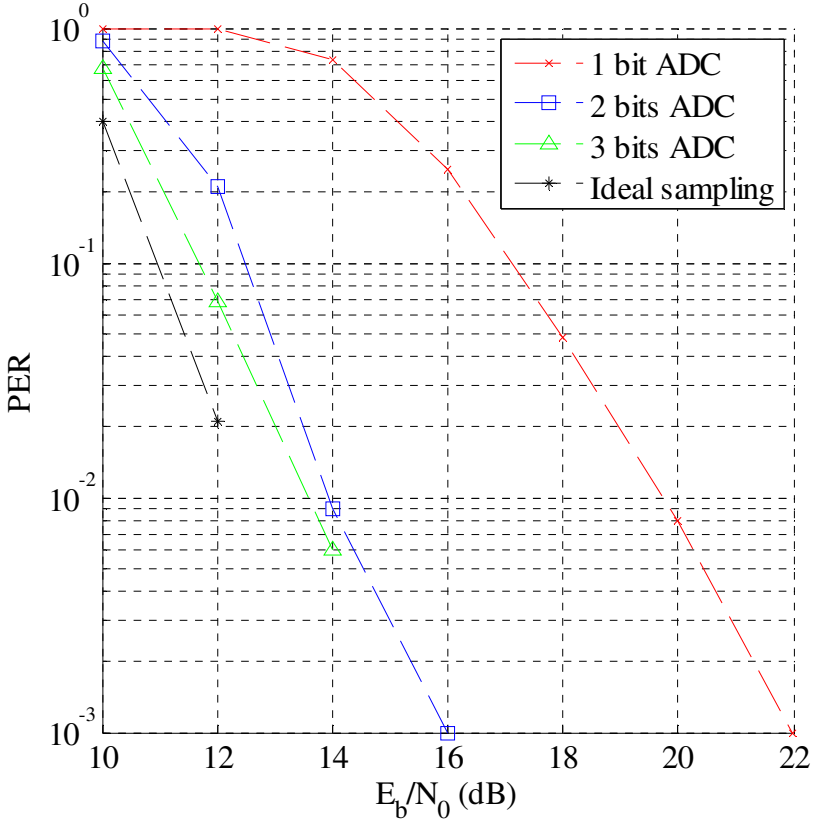
It is considered practical for the system to have constant duty cycle in order to have constant Tx PA pulse power; duty cycle is chosen to be 6.2% which is close to current technology limit of about 4% with 1V power supply.

Synchronization

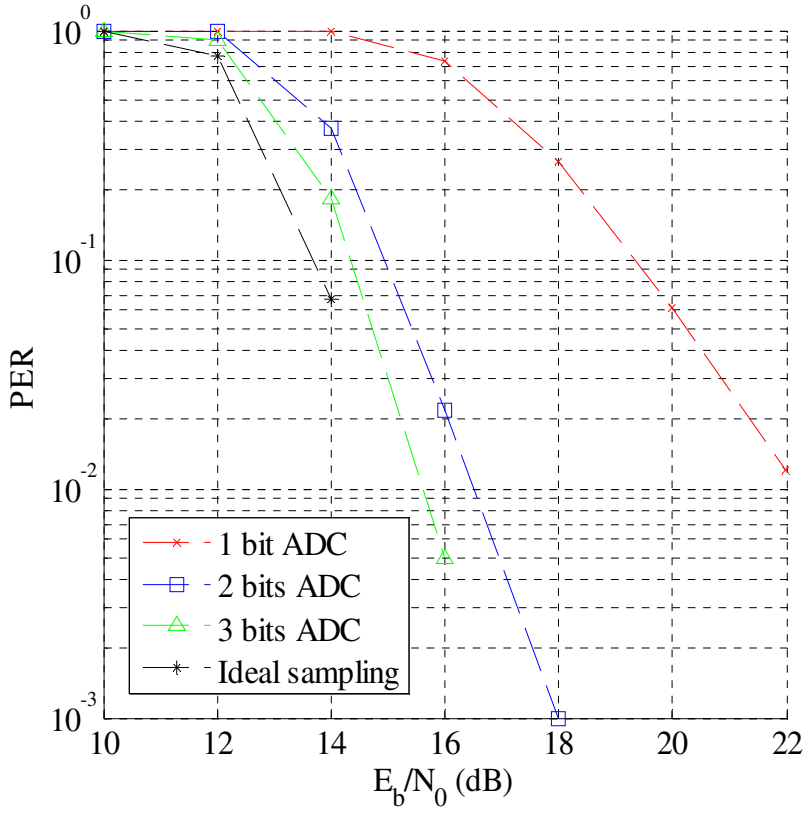
- Symbol rate of 1 Mbps with 9 x DBPSK length 7 Barker sequence is used as preamble. This is enough for AGC, maximum (low pass) signal power finding and estimation of the phase drift coupled with timing drift.
- SFD length 11 DBPSK Barker sequence is used. SFD is detected with DDBPSK. DBSK/DQPSK receiver can use SFD for channel vector estimation.

SYSTEM PERFORMANCE

Packet error rate on CM3 (256 octets PSDU)

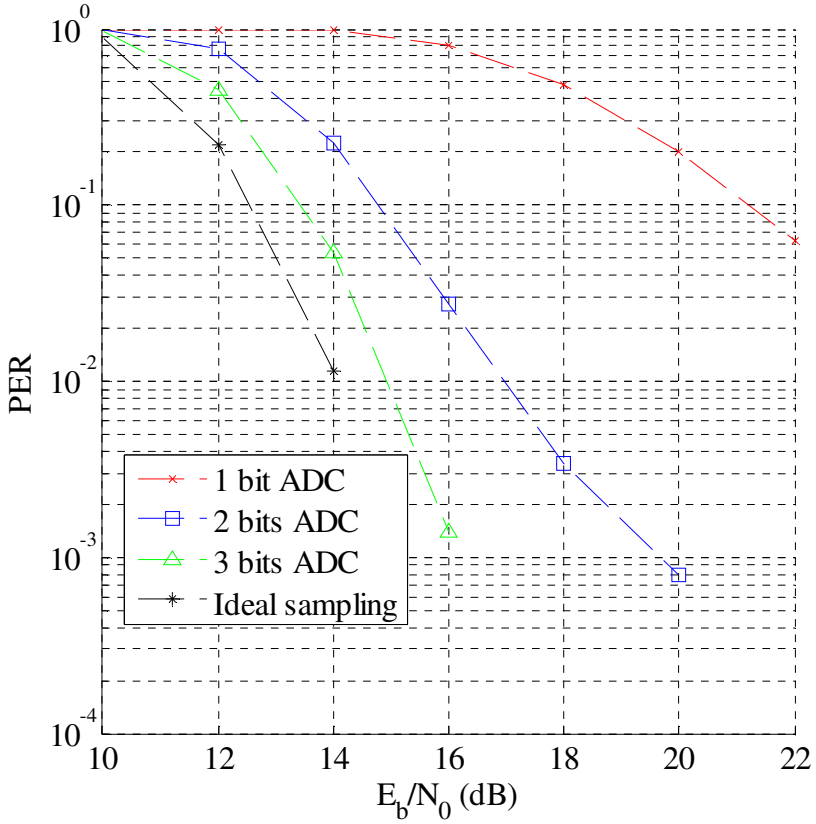


0.98 Mbps uncoded DBPSK.

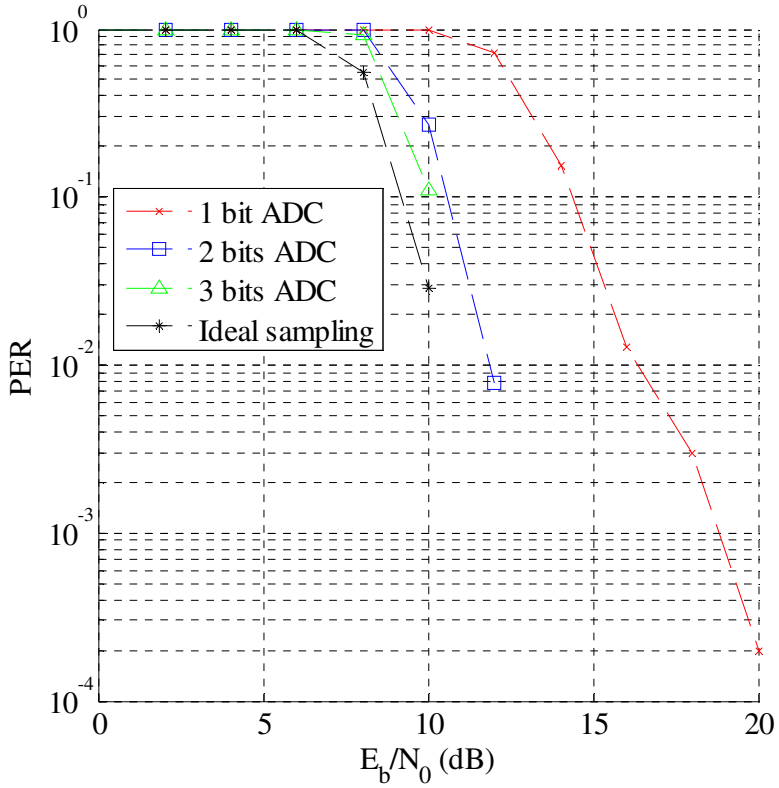


0.98 Mbps uncoded DDBPSK.

Packet error rate on CM3 (256 octets PSDU) cont.

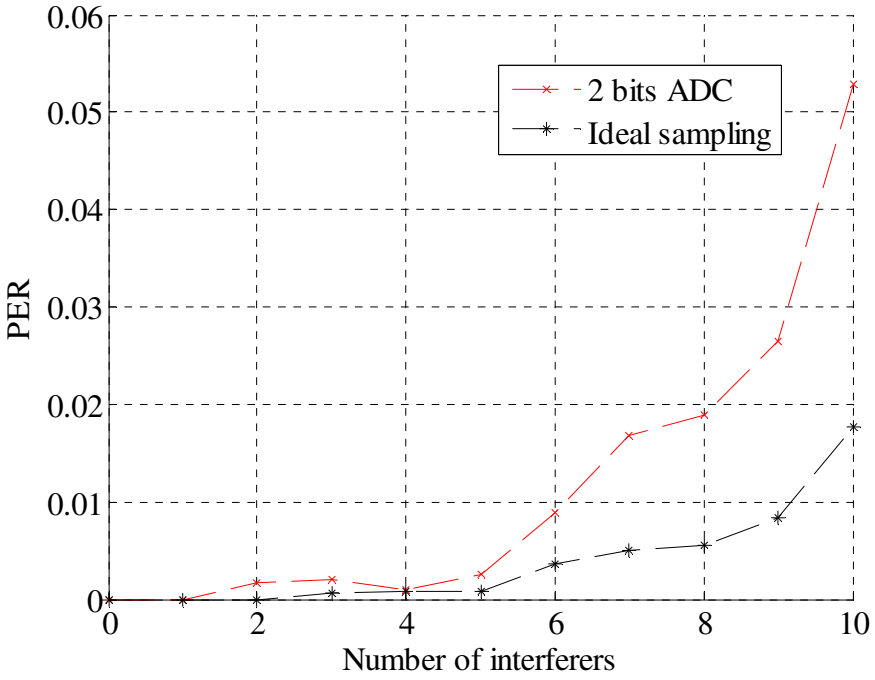


3.92 Mbps uncoded DQPSK.



0.98 Mbps coded DDBPSK with $RS_8(72, 64)$

Multiple Access Interference (MAI) resistance of the system

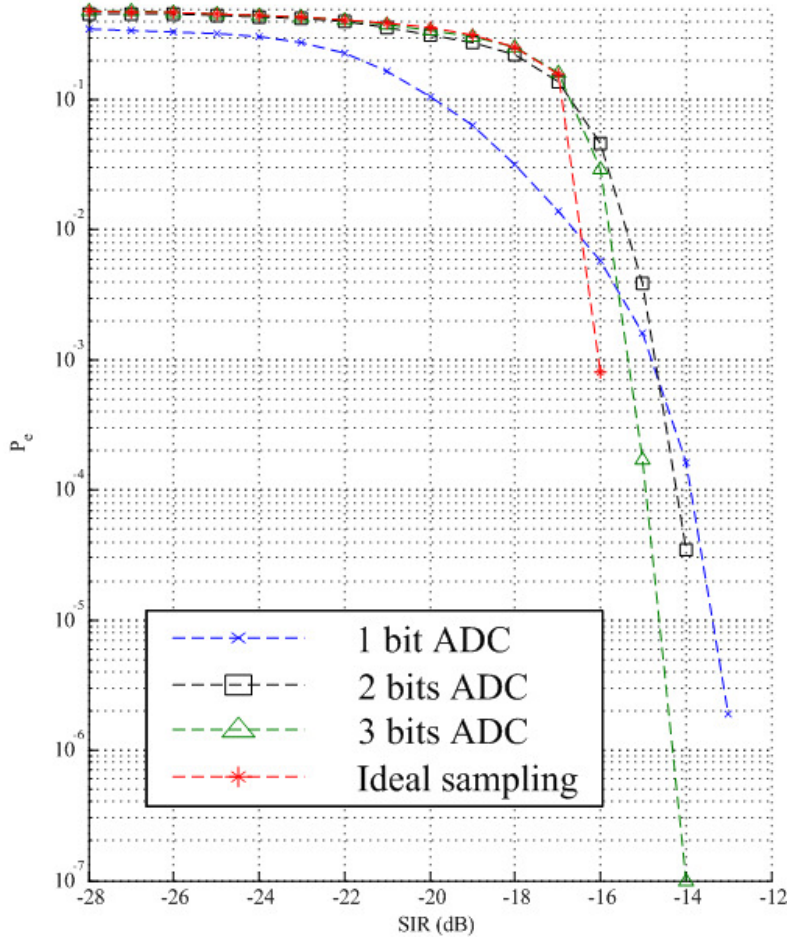


0.98 Mbps uncoded DDBPSK.

Interferers are located on the same IEEE 802.15.4a frequency channel. All interferers have equal power at the receiver to the one of user of interest.

DDBPSK without coding still meets criteria of 10 co-located piconets on the same channel + there is FDMA to increase capacity even more.

NBI resistivity of the system regarding sampling resolution.



Eb/N0=30 dB, 0.98 Msps (Processing gain 27 dB), DDBPSK

•The system fully utilizes processing gain in NBI resistance.

•The system does not have a problem of saturation of low-resolution ADCs with NBI, like some others do, 2 bits are more than enough here.

•Most of processing gain effect to NBI, both in TDMA and CDMA (spreading in frequency and low-pass filtering) is already achieved before ADC.

Link budget

Factor	Symbol (unit)	Value
Tx power	P_Tx (dBm)	-14
Path Gain 1m (3m)	Pg (dB)	-58 (-63)
Tx antenna gain	G_Tx (dBi)	0
Rx antenna gain	G_Rx (dBi)	0
Noise figure	Nf (dB)	7
Noise density	N0 (dBm)	-174
Implementation loss	L_i (dB)	3
Effective power at detection 1m (3m)	P_det (dBm)	-75 (-80)
Bit rate	R_b (Mbps)	0.98
Eb/N0 1m (3m)	Eb/N0 (dB)	32 (27)
Eb/N0 for PER=1e-3	Eb/N0 _req (dB)	16
Receiver sensitivity	S_Rx (dBm)	-91
Link margin	Lm (dB)	16 (11)

- For Pe calculation DDBPSK with 2 bit ADC and 10 samples per symbol is used.

- For the same sampling characteristics other modulation/detection methods have +/- 2 dB variation in the link margin.

Power consumption

- Tx – most power is analog, timing generation power consumption is relatively low:
  - Peak power 15 mW.
  - Standby power 0.1 mW.
  - Duty cycled to 6.2% with duty cycling (on/off) overhead that varies between 1-5 mW depending on the signaling speed.
  - Total power: 2 mW for 0.98 Mcps and 6 mW for 5.20 Mcps.
- Rx – power is divided between analog front-end and digital back-end.
  - Analog front-end – peak power 30 mW.
    - Standby power: 0.1 mW.
    - Duty cycled to 6.2% with duty cycling (on/off) overhead that varies between 2-10 mW depending on the signaling speed (2 mW for 0.98 Mcps and 10 mW for 5.20 Mcps.
    - Total power: 4 mW for 0.98 Mcps and 12 mW for 5.20 Mcps.
  - Digital back-end - peak power about 15 mW – during chip reception/processing @ 0.98 Mcps. (Mean power will be about 1 mW.) It scales nearly linearly with chip rate, to become 4 mW @ 3.92 Mcps and 5 mW @ 5.20 Mcps.
- Total power budget (Tx+Rx):
  - 7 mW @ 0.98 Mcps (245 kbps – 1.96 Mbps)
  - 23 mW @ 5.20 Mcps (10.4 Mbps)

CONCLUSIONS

Conclusions

- The system uses chirp pulses with specific Rx configuration to divide UWB signal de-spreading (signal processing) between analog and digital part of the receiver, which:
  - Lowers burden on digital signal processing with very small complexity increase in analog part of the system.
  - Protects digital part of the receiver from saturation by NBI through doing good part of signal de-spreading before digitalization.

Conclusions (cont.)

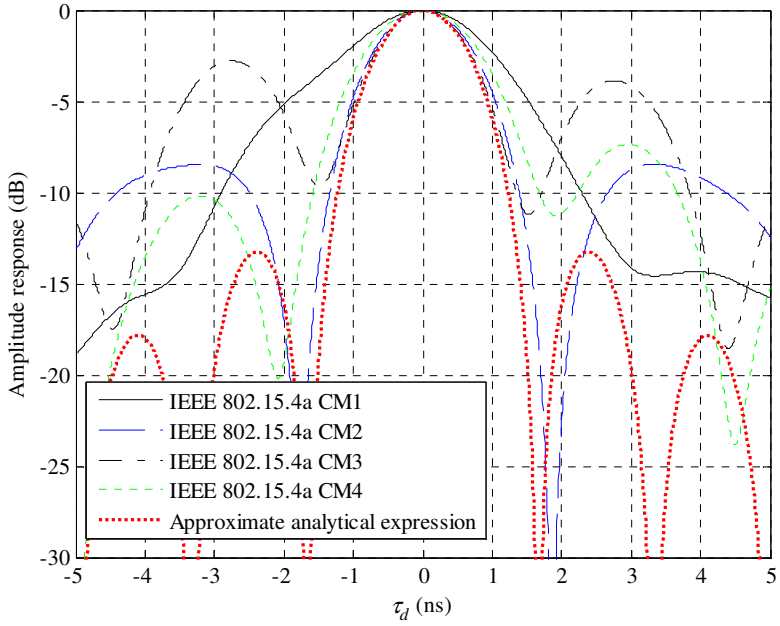
- The system main advantages are:
  - Multipath performance that is about 1-3 dB lower than one of full Rake receiver.
  - Coherent operation with timing resolution requirement that is close to non-coherent short pulse IR-UWB (can be same as sampling period).
  - Low sampling resolution necessary (2 bits are enough).
  - Low sampling rate (about 10 times symbol rate.)
  - Inherent robustness to error in chirp generation.
- The system is full-blown coherent IR-UWB with:
  - high NBI resistance.
  - high MAI resistance.
- The system, especially receiver can be easily reconfigured to be used in other IR-UWB schemes.

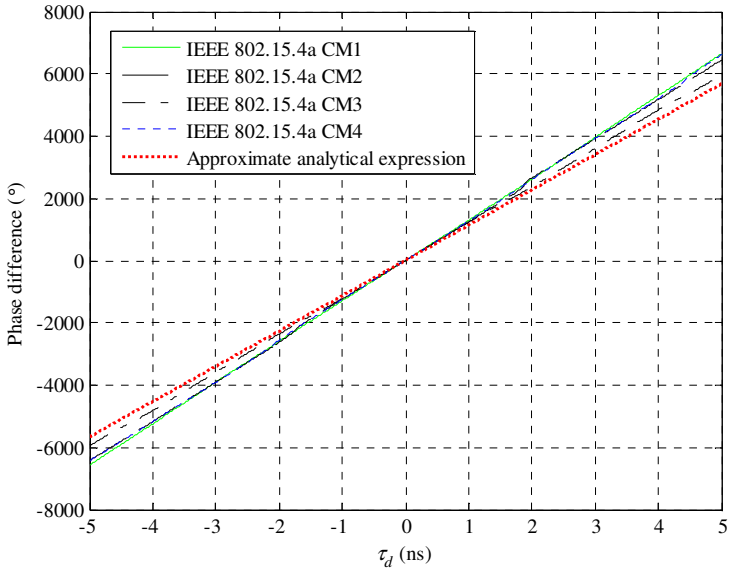
Comparison criteria

- **Regulatory** +
- **Raw PHY data rate (node to node)** +
- **Transmission distance between two nodes** +
- **Packet error rate (PER)** +
- **Link budget** +
- **Power emission level** +
- **Interference and coexistence** +
- **Reliability** +
- **Scalability** +
- **Power Efficiency** +
- **Bonus point** +
  - Proposal is founded upon novel concept of Rx design, however, with known building blocks.

ADDITIONAL SLIDES

Timing drift effects illustration





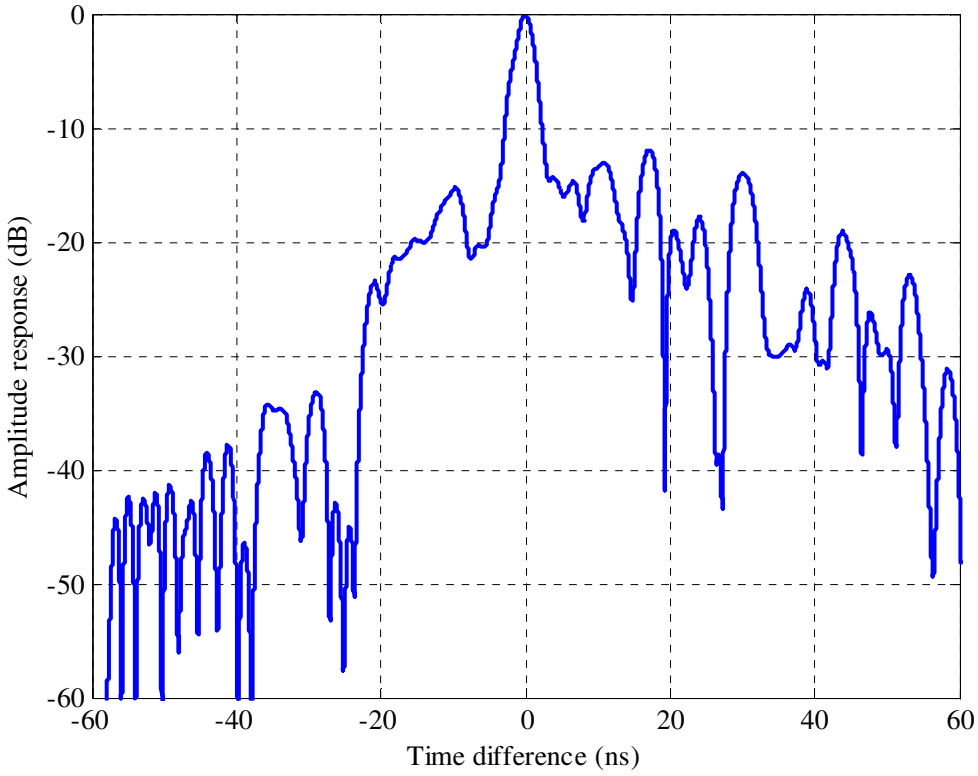
Timing drift effects

- For understanding digital detection mechanisms, understanding timing drift effects is necessary.
- Timing drift effects output digital signal with following approximate expression:

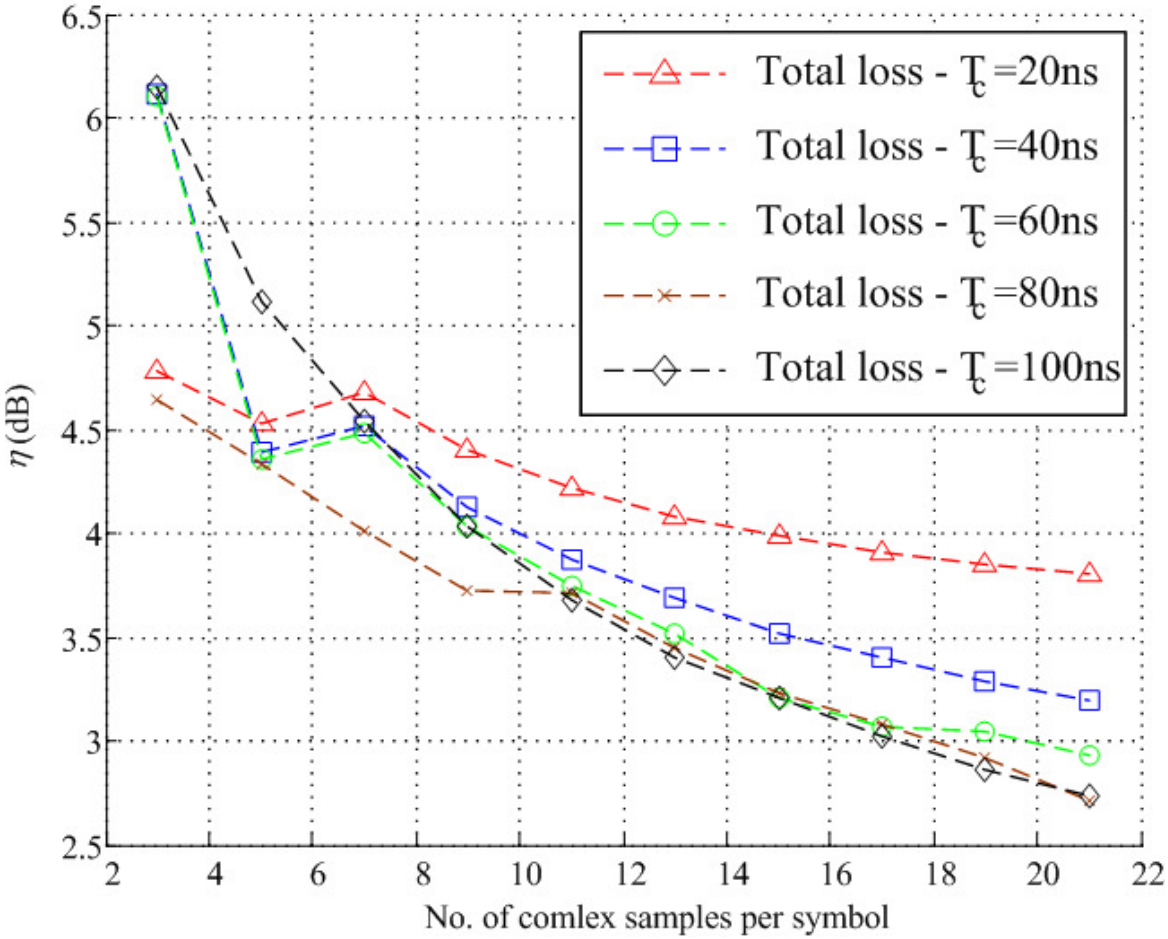
$$\frac{b_k(\tau_d, T_{Ropt})}{b_k(0, T_{Ropt})} \approx \exp\left[j2\pi(f_0 - \Delta f_c / 2)\tau_d \right] \mathrm{sinc}(\pi \Delta f_c \tau_d)$$

- For realistic timing drift value of 20ppm, phase drift on lowest symbol rate of 0.98 Mbps is about 23 and 45 degrees on lower and higher UWB bands respectively while power loss is negligible. Therefore, phase drift estimation ($\hat{\varphi}_d$) and compensation in the digital domain is necessary (via all digital PLL, usually).

System ISI considerations

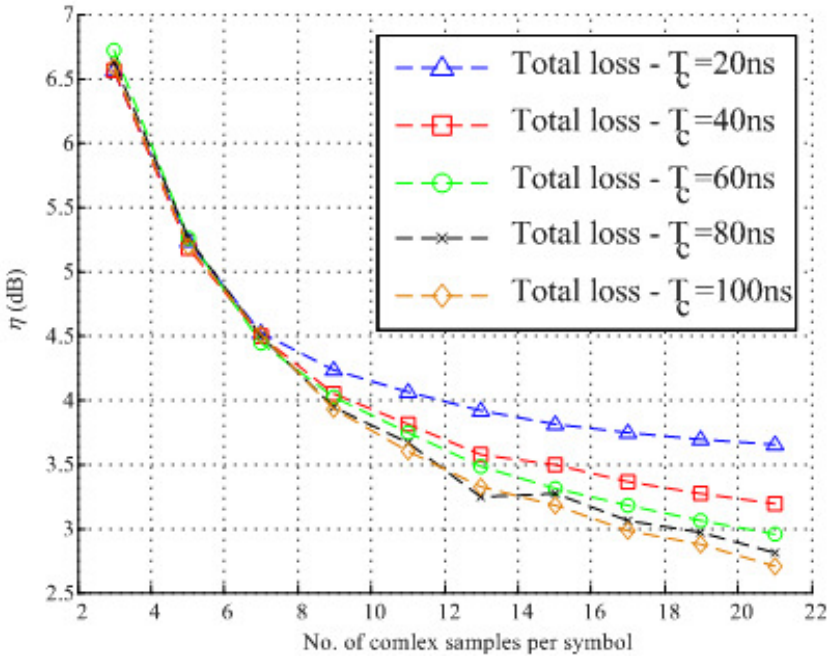


System multipath performance IEEE 802.15.6 CM3

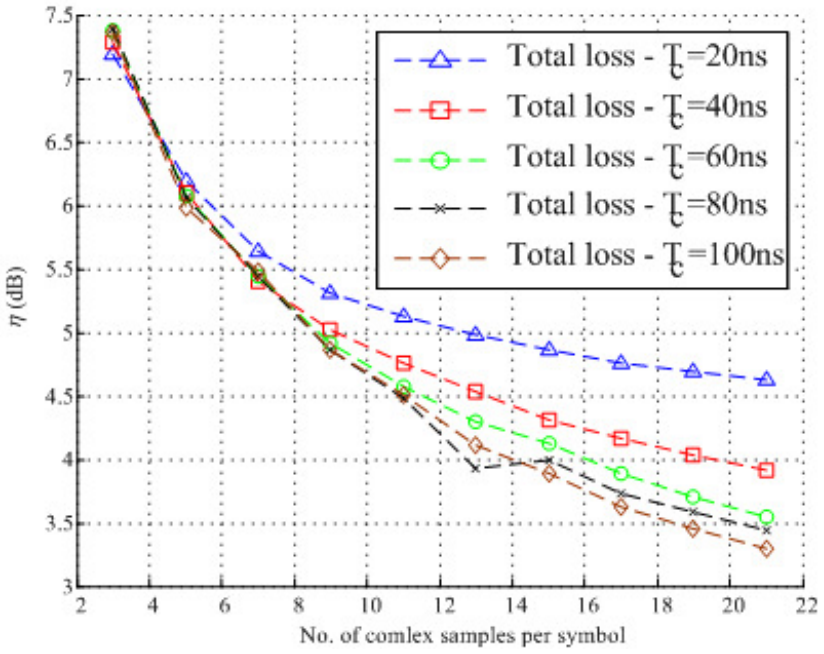


η represents loss of energy compared to ideal (i.e. "full Rake") receiver that collects all multipath energy.

System multipath performance. (cont.)
IEEE 802.15.6 CM4

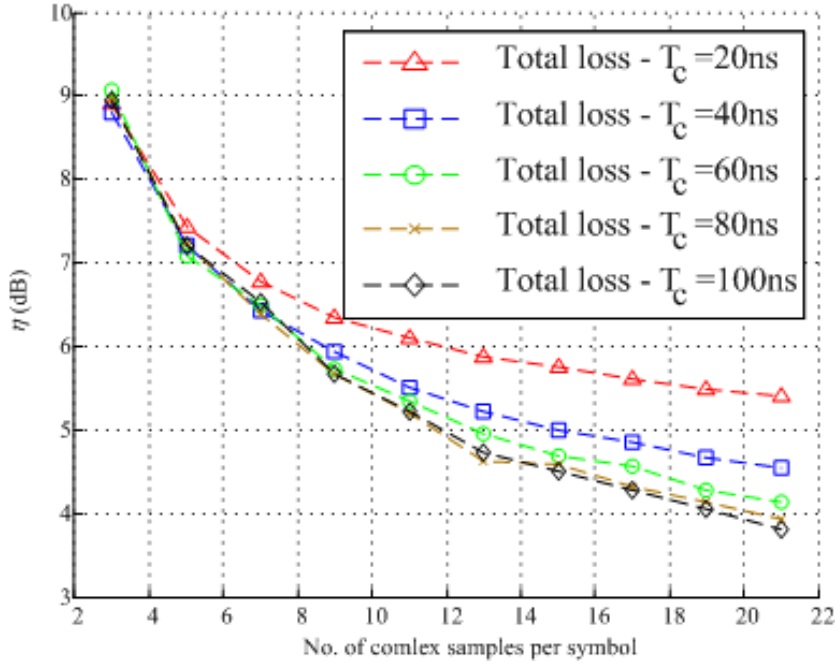


TG6 CM4-1

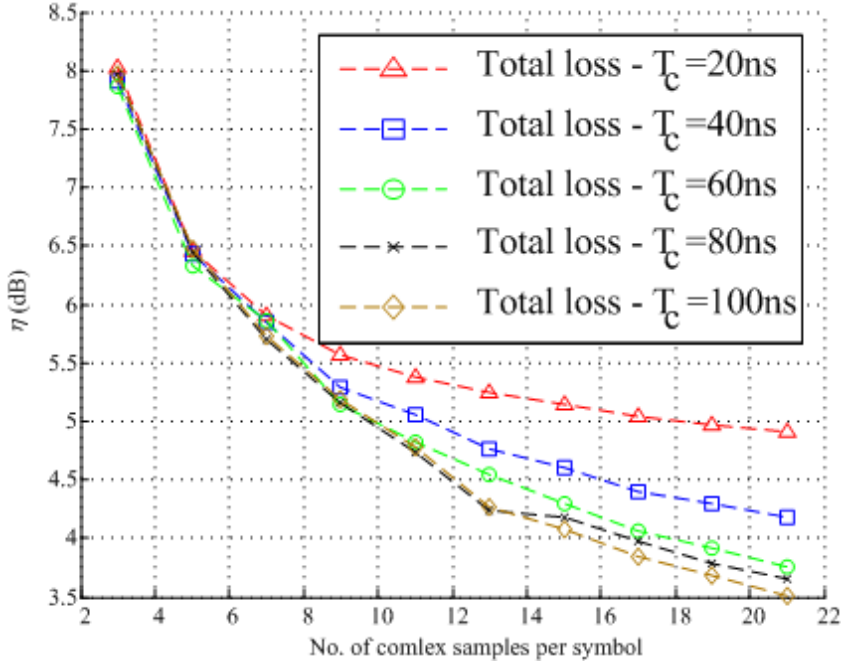


TG6 CM4-2

System multipath performance. (cont.)
IEEE 802.15.6 CM4 (cont.)

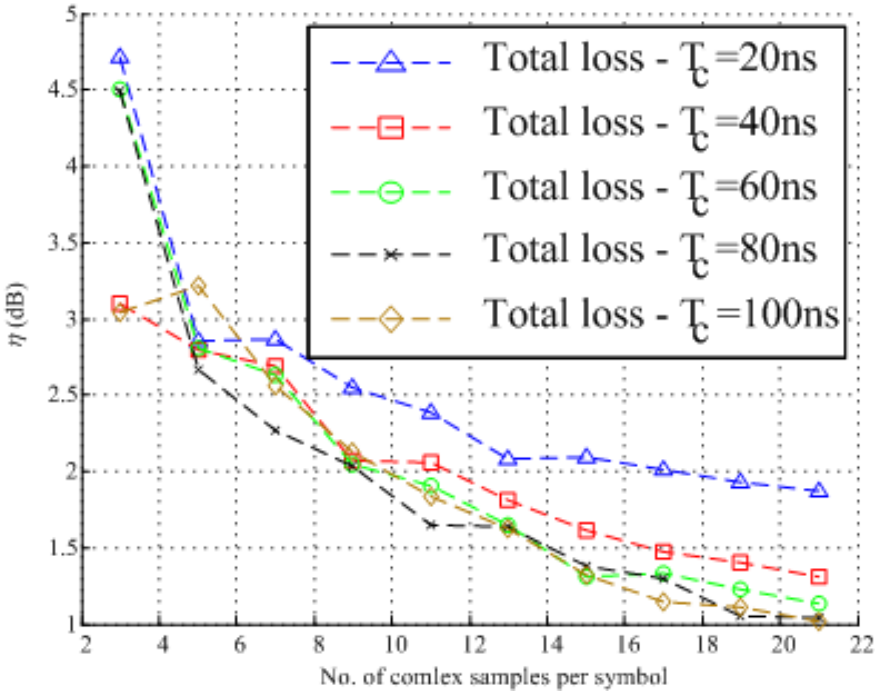


TG6 CM4-3

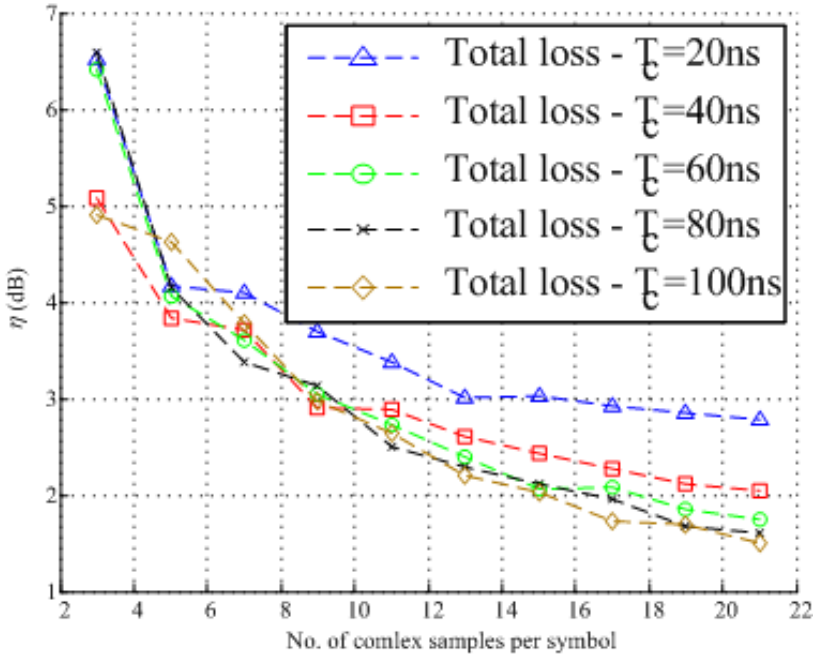


TG6 CM4-4

System multipath performance (cont.)
IEEE 802.15.4a Channel Models

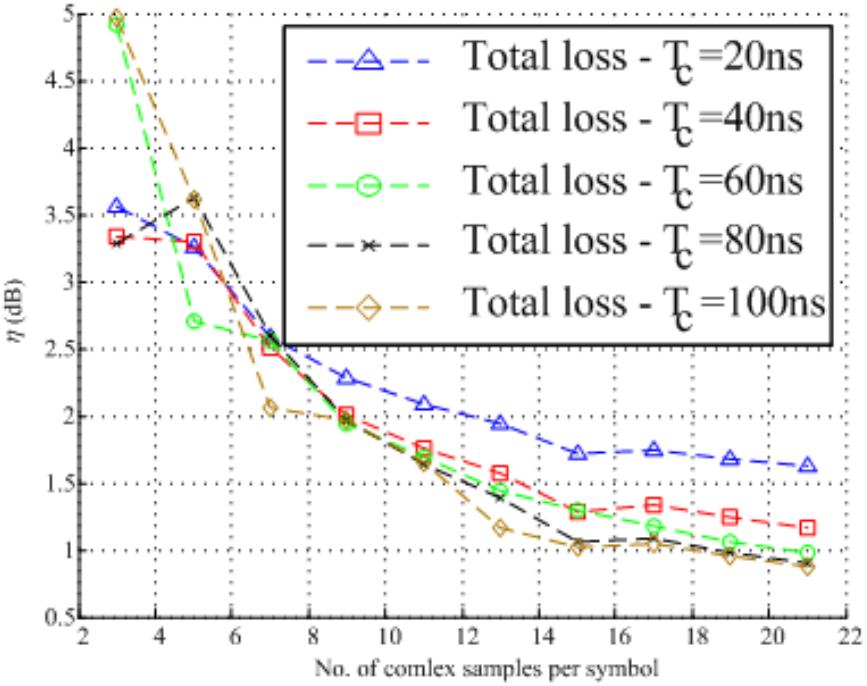


4a CM1

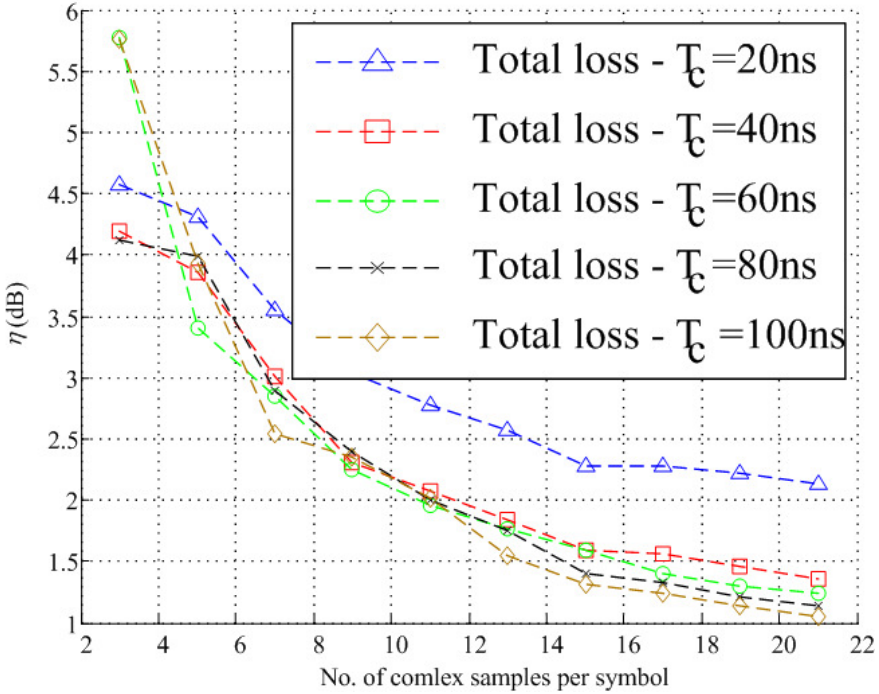


4a CM2

System multipath performance (cont.)
IEEE 802.15.4a Channel Models (cont.)



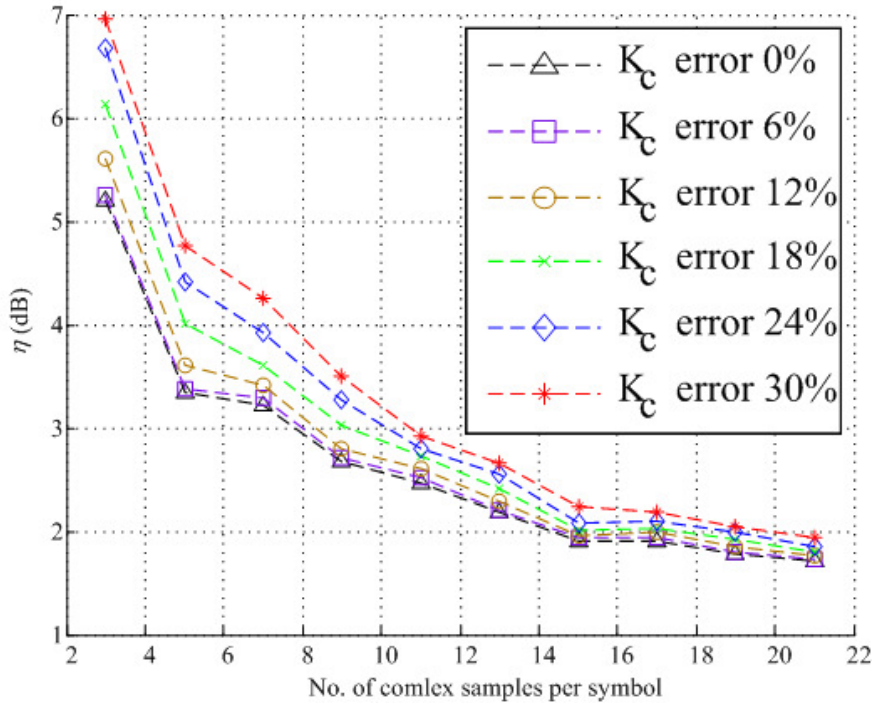
4a CM3



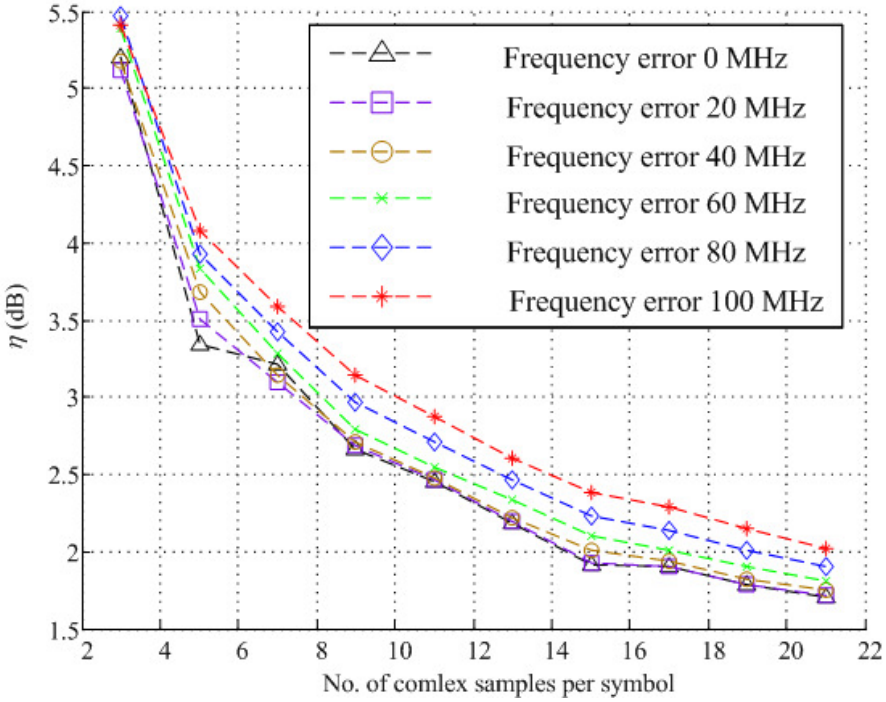
4a CM4

System robustness to chirp errors

Chirp slope (K_c) error



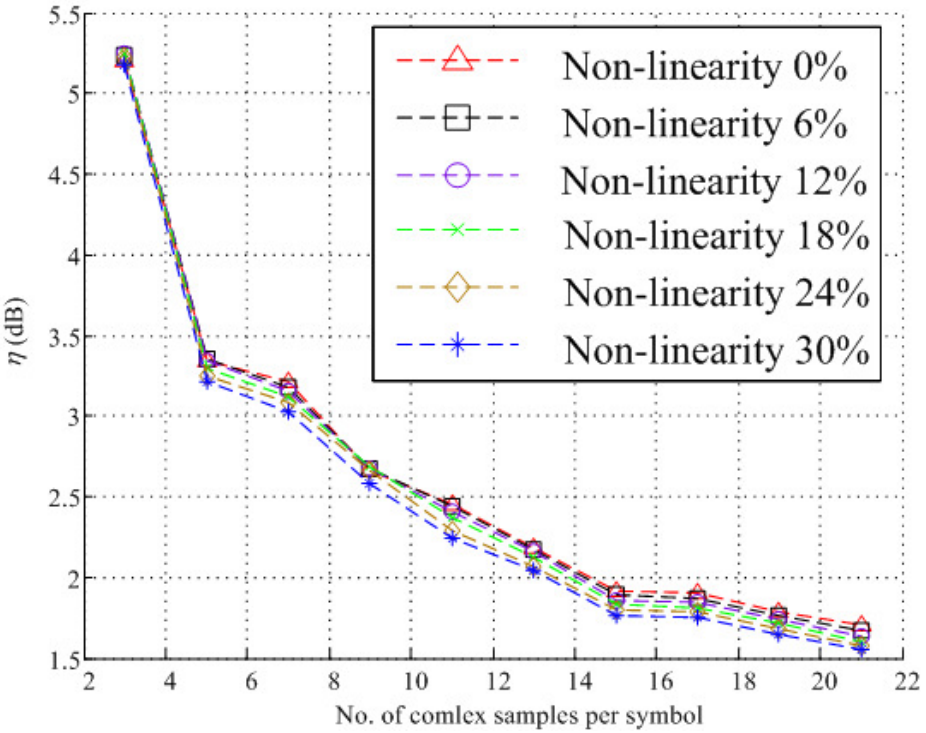
Carrier frequency error



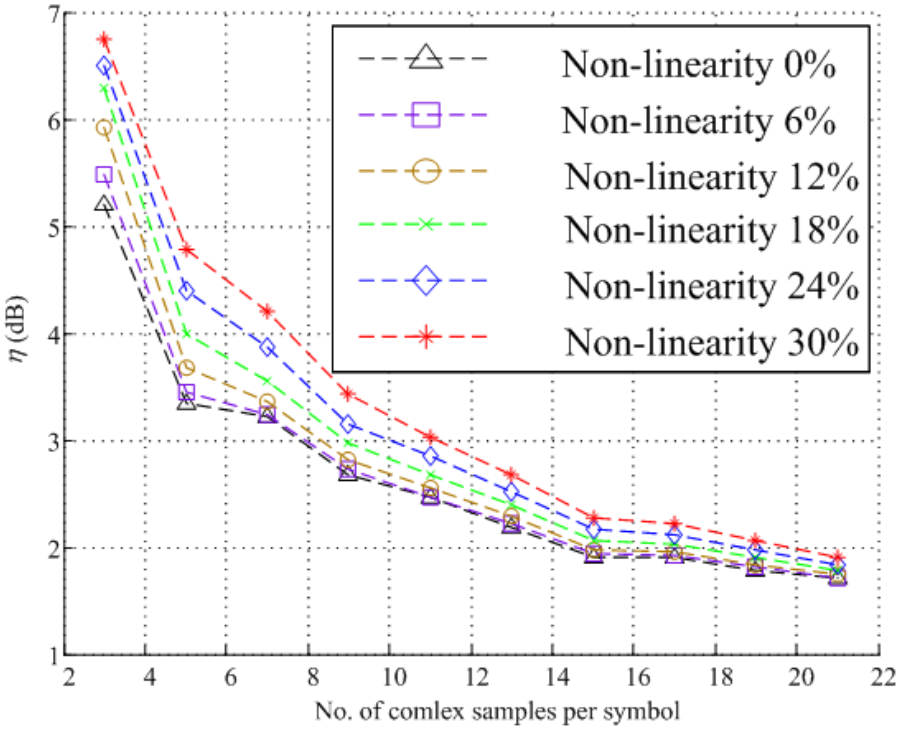
- Chirp slope error of 30% is acceptable
- Central frequency error of 100 MHz is still acceptable.

System robustness to chirp errors (cont.)

K_c non-linearity, same in TX and

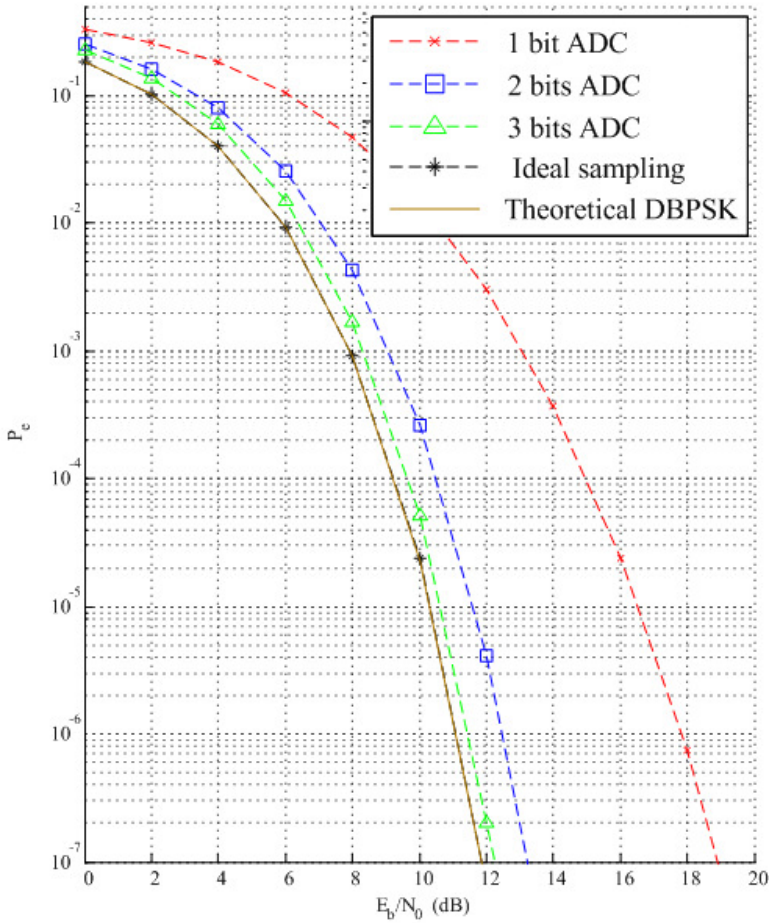


K_c non-linearity, different sign in TX and Rx

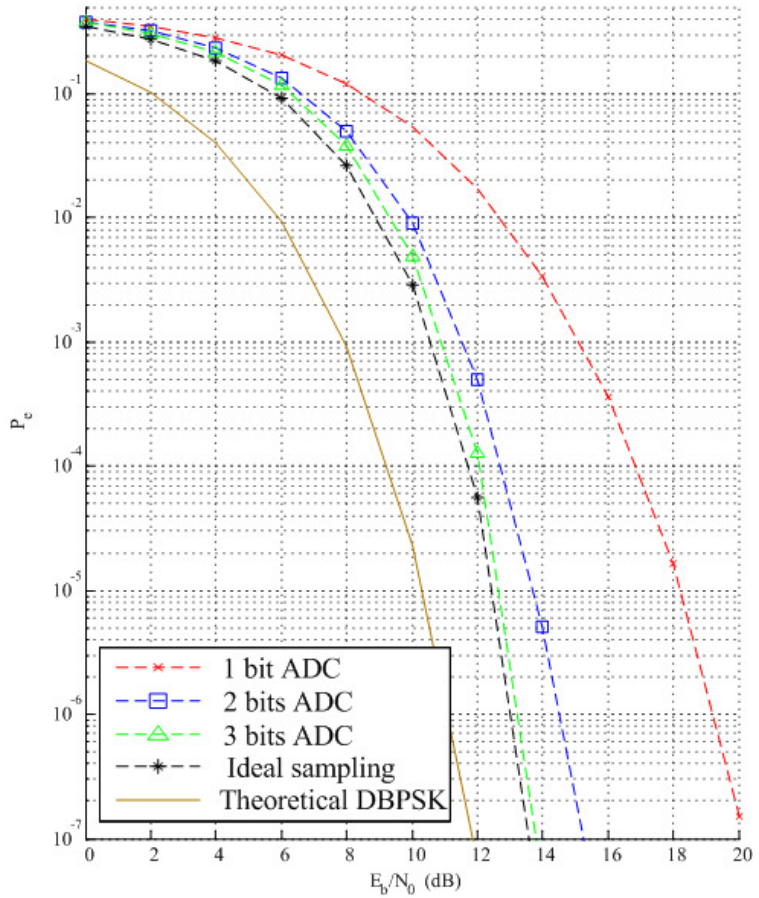


- Non linearity is modeled as 3rd order polynomial.
- 30% Non-linearity is acceptable.

Ordinary DBPSK detection versus DDBPSK with 10 samples per symbol

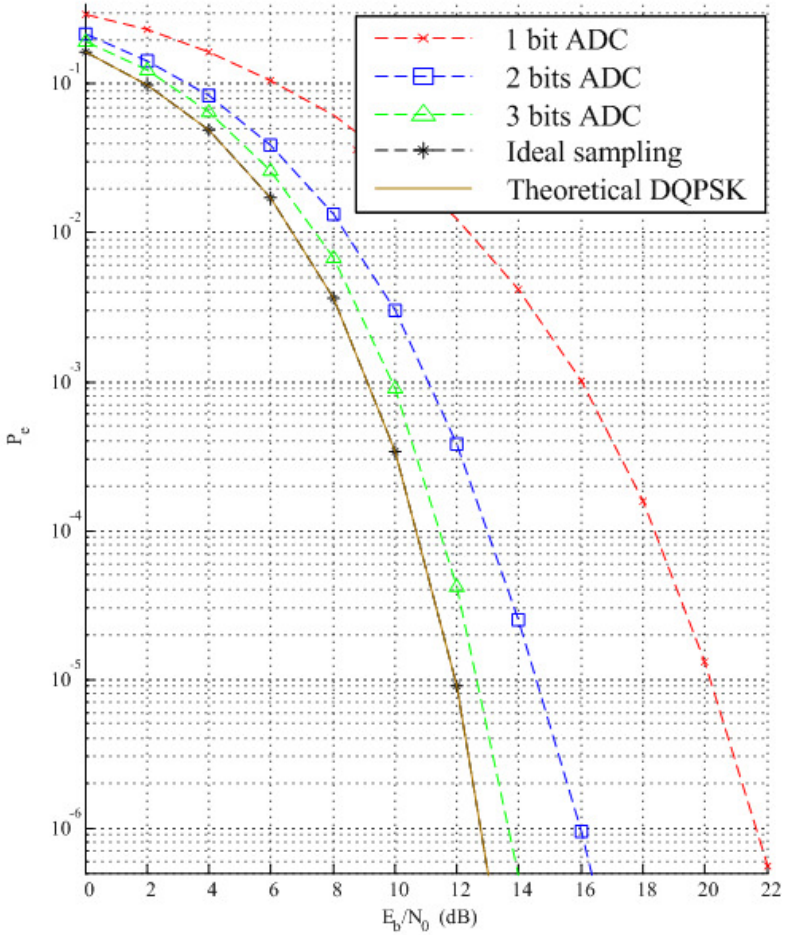


DBPSK

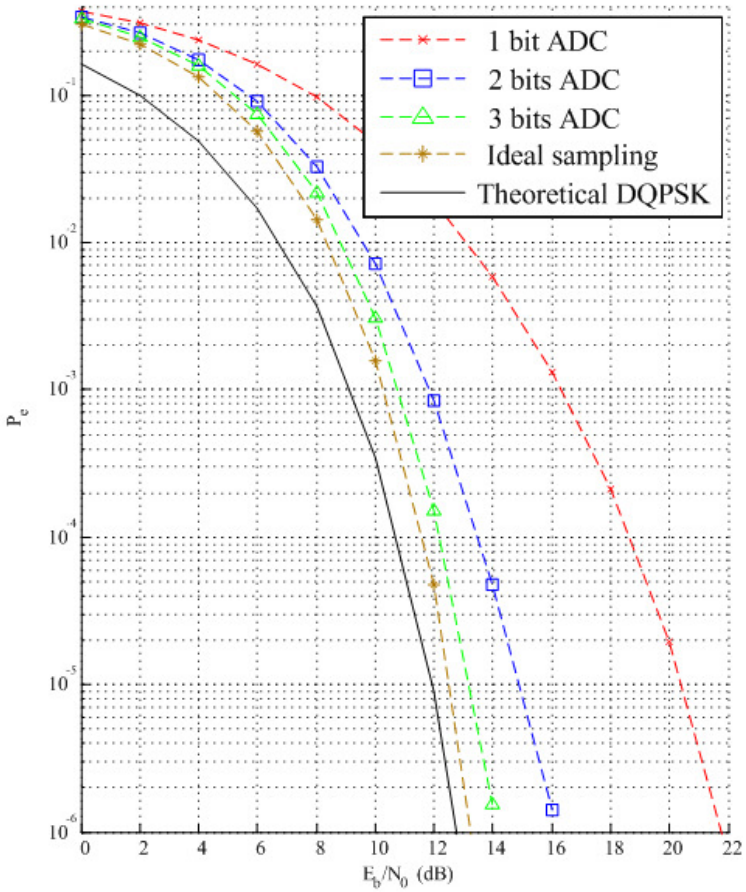


DDBPSK

Ordinary DQPSK detection versus DDQPSK with 10 samples per symbol



DQPSK



DDQPSK