

## **Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)**

**Submission Title:** [IMEC UWB PHY Proposal]

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**Source:** Dries Neirynck, Olivier Rousseaux (Stichting IMEC Nederland)

Address: High Tech Campus 31, 5656AE Eindhoven, Netherlands

Voice: +31 40 277 40 51, E-Mail: [olivier.rousseaux@imec-nl.nl](mailto:olivier.rousseaux@imec-nl.nl)

**Abstract:** This document proposed an impulse radio ultra-wideband physical layer. The basic mode uses burst position modulation in order to enable non-coherent energy detection. The enhanced mode uses concatenated burst modulation to achieve extremely power efficient communications, up to 27.2 Mbps with less than 10 mW. The preamble design enables low power synchronization, in the order of tens of microwatts.

**Purpose:** Proposal to be considered for adoption by TG6

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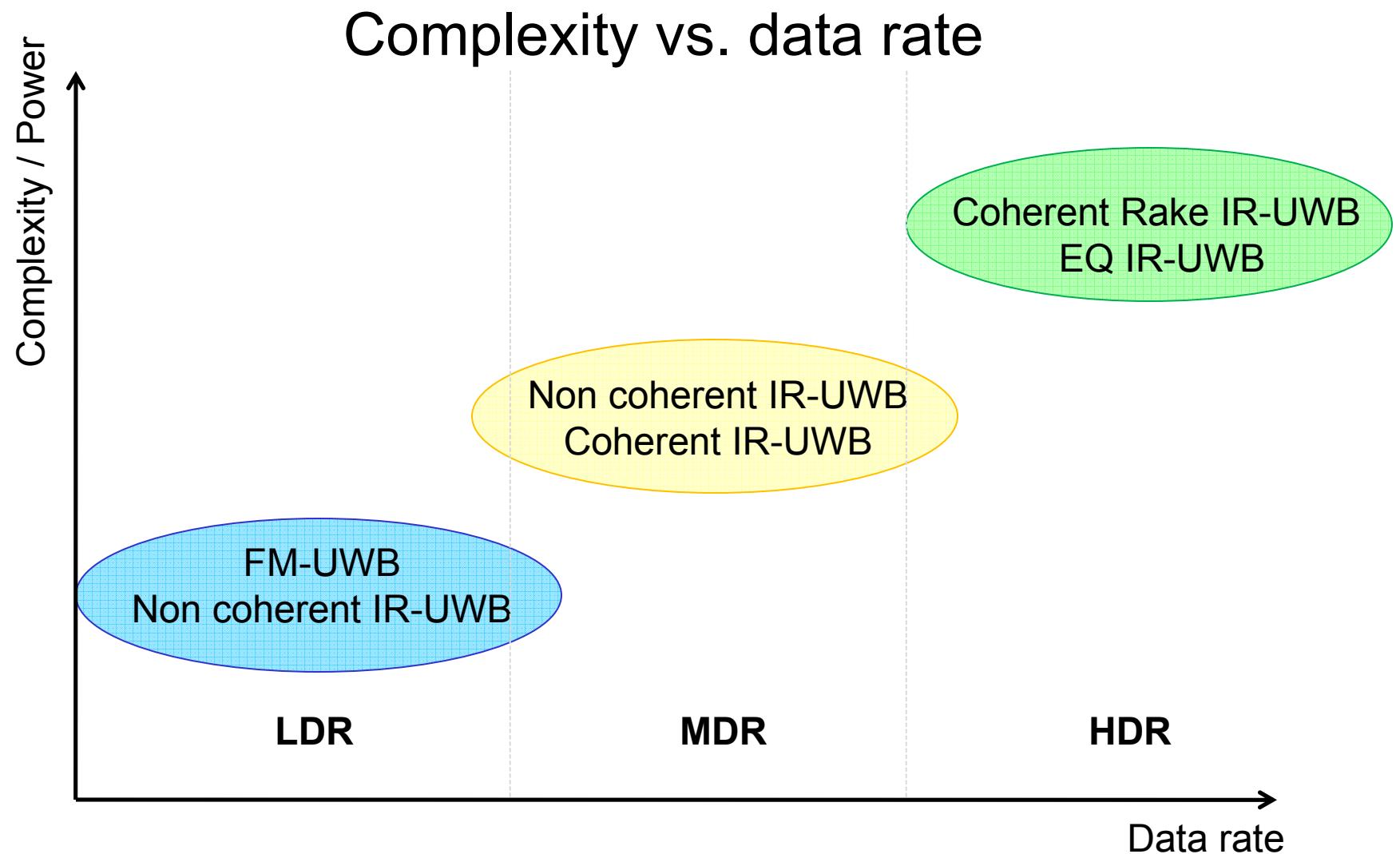
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# Overview

- Motivation IR-UWB
- Proposal
  - Burst position modulation
  - Concatenated burst modulation
- The PHY proposal outlined in this presentation is a part of IMEC's UWB PHY/MAC proposal. The complete proposal is made of this PHY used in combination with the UWB MAC presented in doc: 802.15-15-09-0332-00-0006.

# Advantages of UWB

- **Low radiated power**
  - Low PSD, low interference, low SAR
  - High co-existence with existing 802.x standards
  - Real potential for low power consumption
- **Large bandwidth worldwide**
  - Spectrum is worldwide available
  - Robust to multipath and fast varying channels
- **Flexible, scalable (e.g. data rates, users)**
- **Low complexity HW/SW solutions in advanced development**



# IR-UWB suits BAN

- License-free operation
- Scarce usage of air interface
  - Supports low power operation by duty cycling
  - Favours multi-user operation and high node density
- Low spectral emission (-41.3 dBm/MHz):
  - Avoids interference to other systems
  - Minimizes user exposure to radiation
- Robust to interference
  - Spectrum from 3-10 GHz available
- Flexible data rate – range trade-off by adapting spreading code length

# Proven technology

- Isolated pulse based systems
- Burst based systems, including 15.4a:
  - Reduced starting-up/shutting down overhead when duty-cycling
  - Larger separation between bursts increases multipath robustness.
- Hence, proposal is inspired by 15.4a

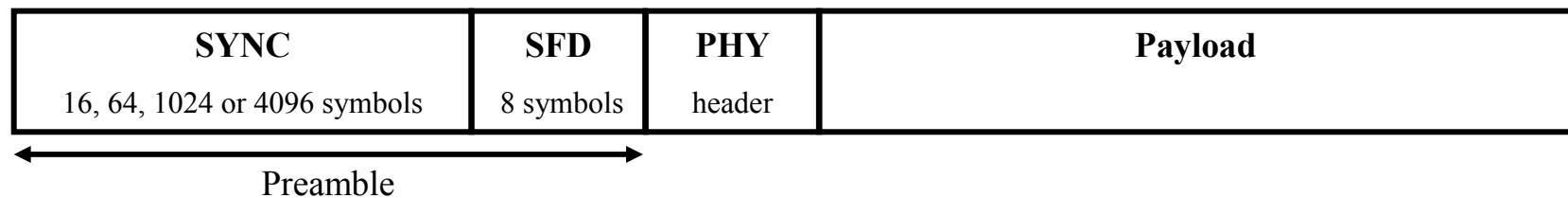
## 15.4a weaknesses to be avoided

- At low data rates, long gap between bursts leads to extremely difficult timing accuracy requirements in order to be able to detect burst phase
- At high data rates, guard interval between bursts shortens, leading to inter-symbol interference
- Power consumption quickly increases with higher data rate because of start-up overhead

# Proposed solution

- Basic mode: burst position modulation
  - 15.4a minus burst phase shift keying
  - Allows non-coherent reception
- Enhanced mode: concatenated burst modulation
  - Ensures long guard interval to avoid interference between strings
  - Constant start-up overhead: efficient duty cycling even at high data rates

# Basic packet structure



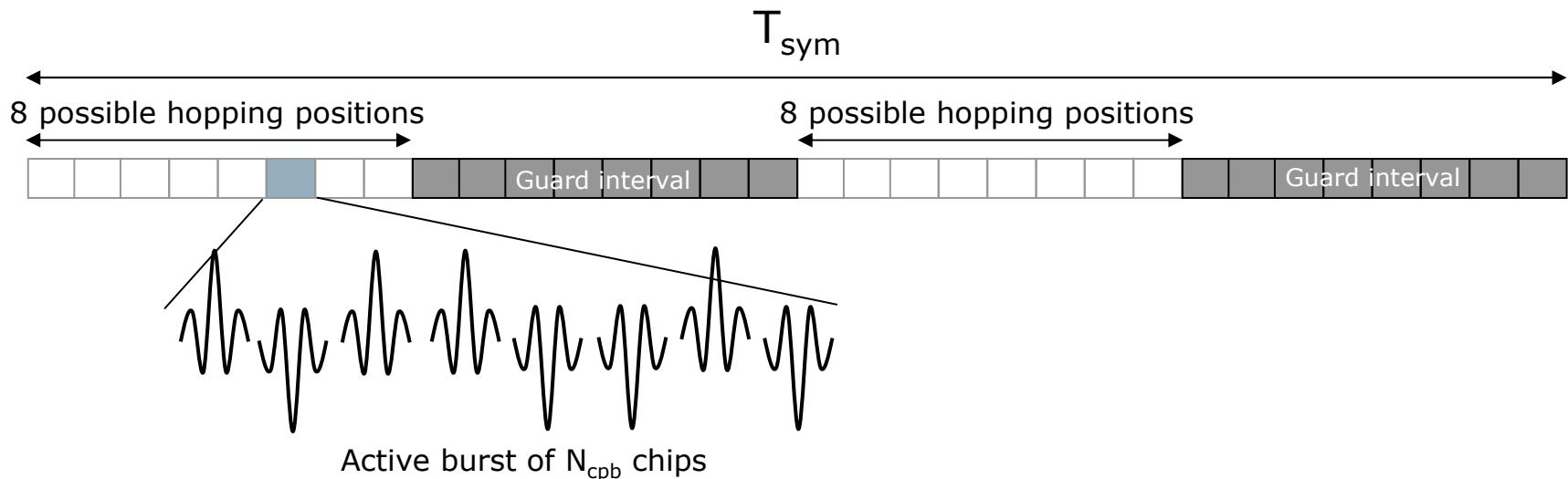
- 15.4a inspired:
  - Preamble: regularly spaced isolated pulses
  - PHY Header: burst position modulation
  - Payload:
    - burst position modulation, or
    - concatenated burst modulation

# Burst Position Modulation

- Simple version of 15.4a, supporting non-coherent energy detectors:
- 15.6 MHz mean pulse repetition freq. only.
- No burst phase modulation
- RS<sub>6</sub>(63,55) from 15.4a is kept

# BPM Symbol structure

- Each burst contains  $N_{cpb}$  active chips
- Each symbol consists of 4 sets of 8 burst durations
  - The active burst will be located in sets 1 or 3, depending on whether a '0' or '1' is being transmitted
  - Sets 2 and 4 act as guard intervals to reduce inter-symbol interference



# Basic mode - Data rates

Mode	Mean PRF	$N_{\text{hop}} / N_{\text{burst}}$	$N_{\text{cpb}}$	Data rate
1.1	15.6 MHz	8 / 32	128	0.11 Mbps
1.2			16	0.85 Mbps
1.3			8	1.70 Mbps
1.4			4	3.40 Mbps
1.5			2	6.81 Mbps
1.6			1	13.6 Mbps

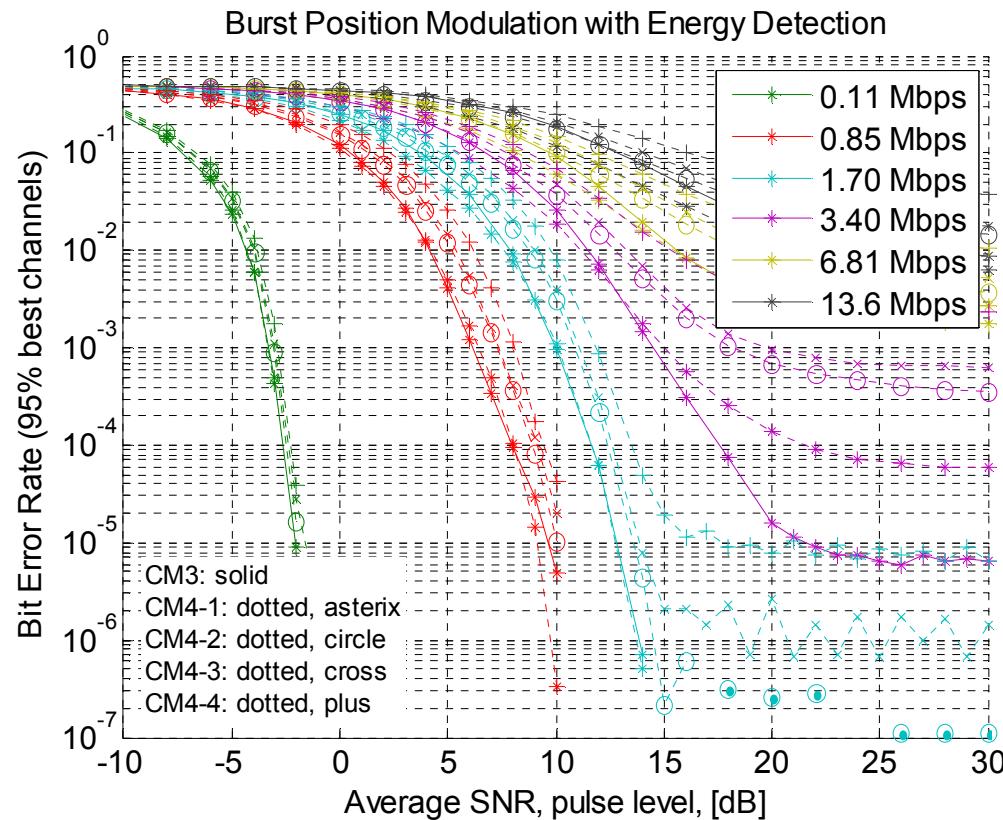
- 15.4 terminology:
  - Mean PRF: mean pulse repetition frequency
  - $N_{\text{hop}}$ : number of possible burst positions per slot
  - $N_{\text{burst}}$ : symbol length relative to burst length
  - $N_{\text{cpb}}$ : number of chips per burst

# Basic Mode - Power consumption estimates

- Assumptions:
  - Start-up TX and RX: 50 and 100 ns respectively
  - Power consumption TX and RX: 50 mW during on time
- Duty cycling supports low power at low data rates,
- Rapidly increasing power consumption at higher data rates:

Mode	$N_{cpb}$	Data rate	Avg. TX Power	Avg. RX Power
1.1	128	0.11 Mbps	2.0 mW	4.6 mW
1.2	16	0.85 Mbps	4.3 mW	13.3 mW
1.3	8	1.70 Mbps	7.0 mW	23.0 mW
1.4	4	3.40 Mbps	12.1 mW	41.5 mW
1.5	2	6.81 Mbps	21.1 mW	47.6 mW
1.6	1	13.6 Mbps	35.7 mW	45.9 mW

# BER BPM with Energy Detector



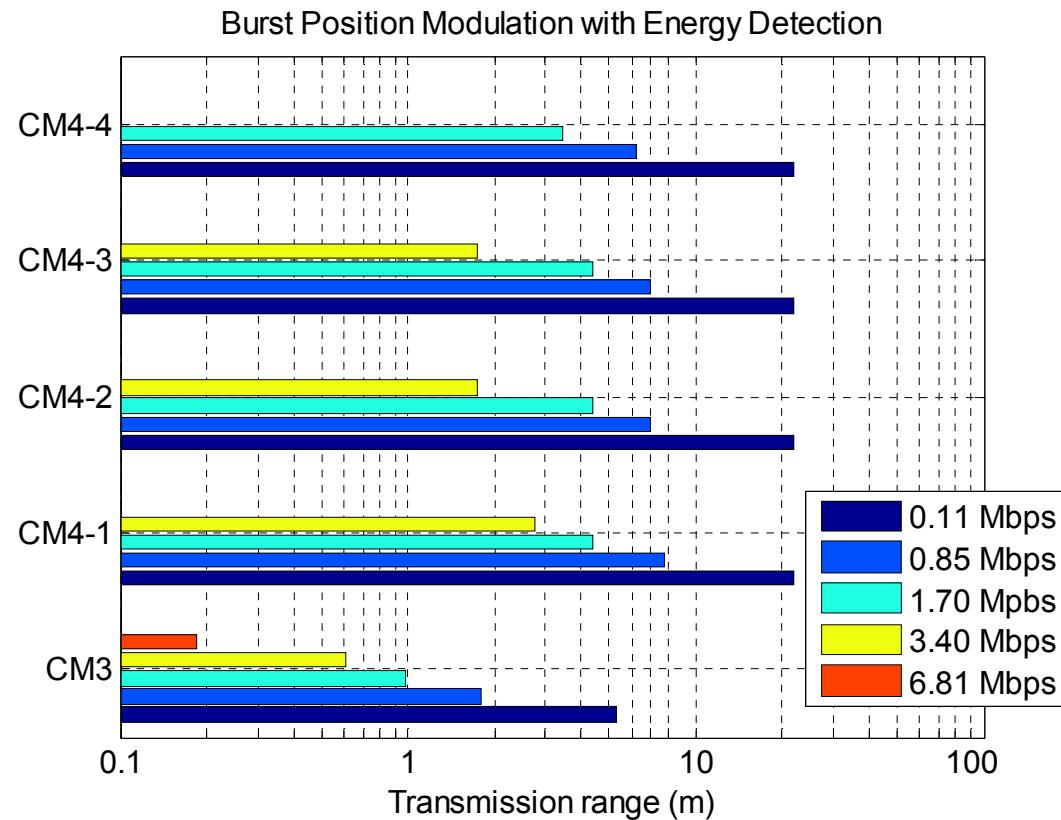
# Link budget

Transmitter	Transmit power	0 dBm	Vpeak = 316 mV, 50 Ohm load
Channel	Antenna Gains	0 dB	
	Path loss & fading		CM3/CM4 models
Receiver	Thermal noise	-86 dBm	500 MHz, 30°C
	Noise figure	12 dB	
	Implementation loss	2 dB	

## Path loss

- According to channel model document  
08-0780-06-0006
- CM3:
  - PL [dB] =  $19.2 * \log_{10}(d [\text{mm}]) + 3.38$
- CM4:
  - Free space path loss
  - Centre frequency: 6 GHz

# Range BPM with Energy Detector

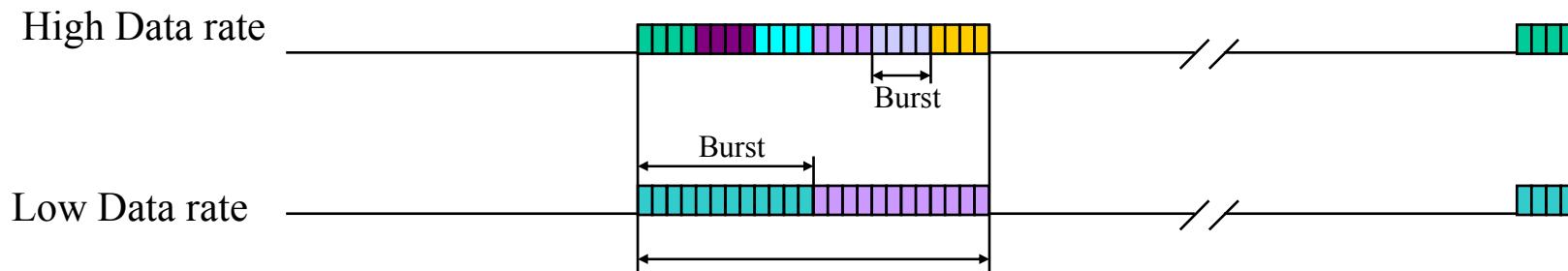


# Burst position modulation conclusion

- Higher data rates achieved by shortening symbols and guard periods. Start-up times remain constant
- Duty cycling ratio and ISI worsen as data rate increases
- Enhanced mode using concatenated modulation can solve these shortcomings.

# Enhanced mode: Concatenated Burst Modulation

- Concatenate bursts into continuous strings
  - Higher data rates are achieved by decreasing burst length, i.e. more bursts per string
  - Maintains duty cycling ratio at high data rates



# Concatenation needs ISI mitigation

- Lower data rates have longer burst lengths, hence rake receivers may work
- Frequency domain equalisation is efficient way of removing ISI:
  - Silence periods around strings provide cyclic prefix
  - Channel matrix is then circulant:
  - Equalisation reduces to FFT, one-tap equalisation (i.e. multiplication), IFFT

# FFT complexity estimate

- Assumptions:
  - 200MHz digital clock
  - FFT size 512
  - CMOS 90nm
  - Bit width 8 bits
- It requires 8 clocks do to do the computation and digital is turned off for the rest of the time.
- 4608 additions @ 8.5  $\mu\text{W}$  each
- 4608 multiplications @ 140  $\mu\text{W}$  each
- 4608 register files @

# Enhanced mode power estimate

- Same assumptions as before:
  - Start-up TX and RX: 50 and 100 ns respectively
  - Power consumption TX and RX: 50 mW during on time
- Assume frequency domain equalisation is to combat ISI:
  - 5 mW for FFT size 512 (ref: 09-0181-03)
  - FFT power consumption scales as  $N \cdot \log(N)$

String length	Avg. TX power	Avg. RX power	FFT size	FFT power	Total Avg. RX Power
64	2.0 mW	4.6 mW	128	0.42 mW	5.0 mW
128	2.3 mW	5.7 mW	256	0.97 mW	6.7 mW

# Enhanced mode - modulation

- On-off keying and differential burst shift keying have been considered
  - DBPSK encodes data in phase difference between bursts.  
First burst of each string is a reference burst.
  - OOK encodes data in presence or absence of the burst.
- On-off keying is only active half the time:
  - data rate can be doubled using same  $m_{PRF}$
- But DBPSK preferred:
  - Offers more robust performance for similar throughput
  - Avoids problem of choosing threshold for OOK
- Only highest data rate uses OOK

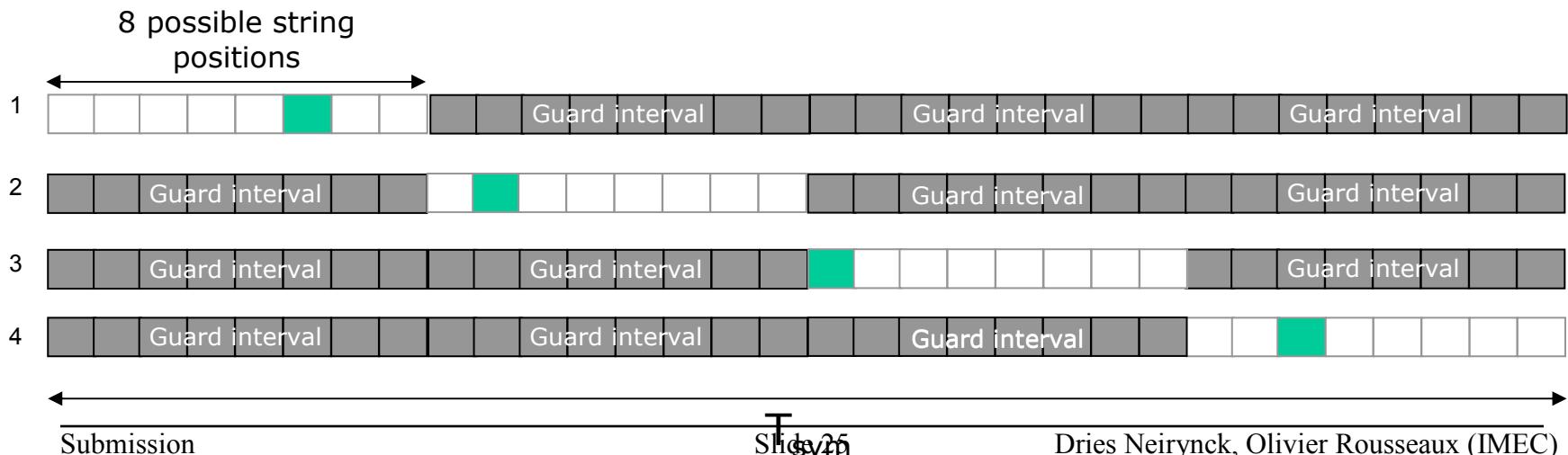
# Enhanced mode – data rates

Mode	Mean PRF	$N_{cpb} / N_{cps}$	Modulation	Data rate
2.1	15.6 MHz	16 / 64	DBPSK	0.64 Mbps
2.2		8 / 64	DBPSK	1.5 Mbps
2.3		4 / 64	DBPSK	3.2 Mbps
2.4		2 / 64	DBPSK	6.6 Mbps
2.5		1 / 64	DBPSK	13.4 Mbps
2.6		1 / 128	OOK	27.2 Mbps

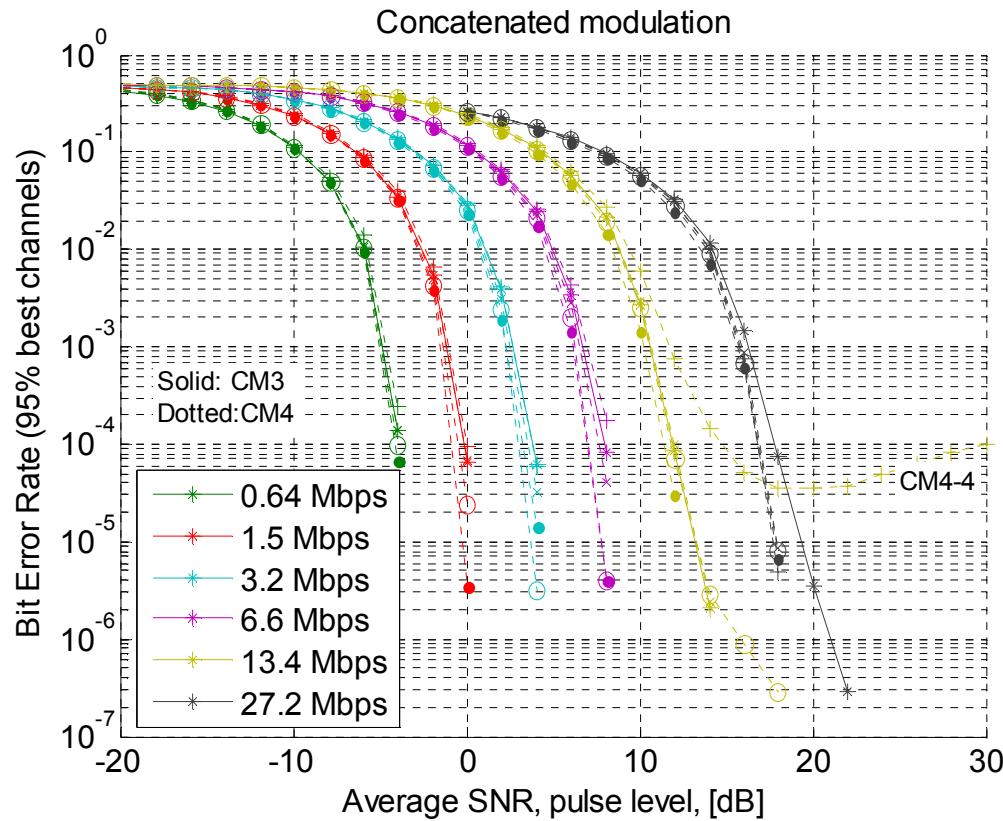
- Basic mode requires roughly 100 mW to support 13.6 Mbps,
- Enhanced mode supports up to 27.2 Mbps with less than 10 mW!

## Enhanced mode symbol structure

- Rotate through four sets of 8 possible string durations such that gap between them is maximised to four guard intervals
- Each string contains 64 chips, consisting of bursts up to 16 chips



# BER Concatenated Modulation

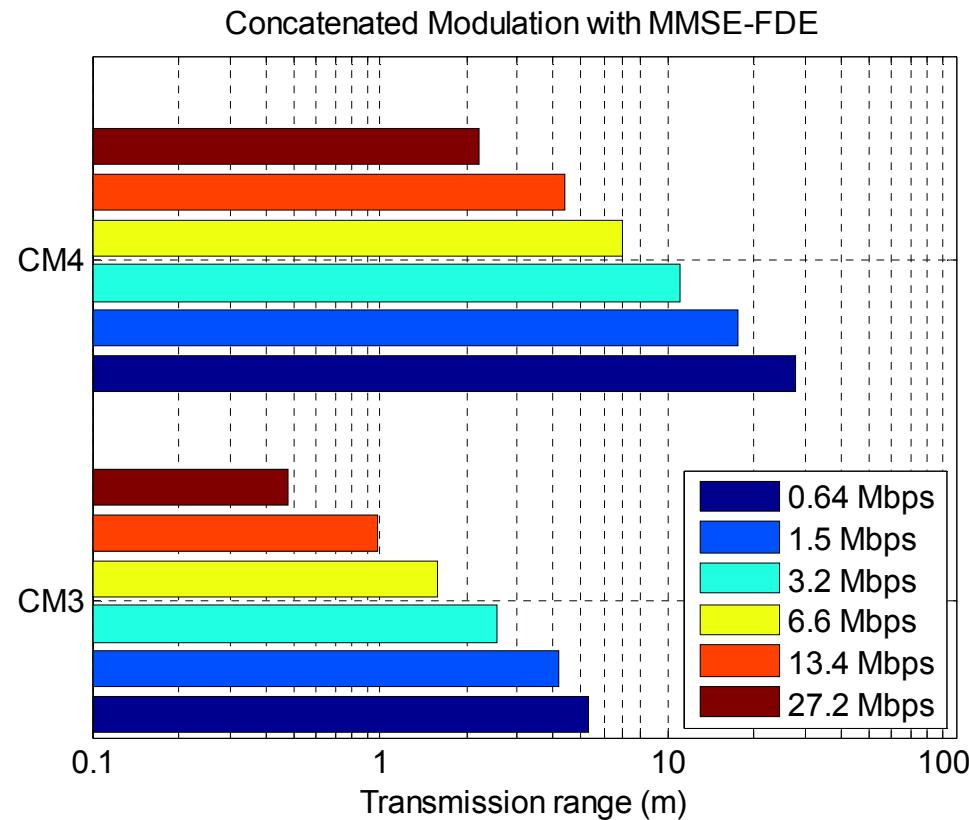


# Link budget & path loss as before

Transmitter	Transmit power	0 dBm
Channel	Antenna Gains	0 dB
	Path loss & fading	CM3/CM4 models
Receiver	Thermal noise	-86 dBm
	Noise figure	12 dB
	Implementation loss	2 dB

- Path loss according to channel model document (08-0780-06)
- CM3:  
$$PL [dB] = 19.2 * \log_{10}(d [\text{mm}]) + 3.38$$
- CM4:
  - Free space path loss
  - Centre frequency: 6 GHz

# Range Concatenated Modulation



# Preamble

- Based on 15.4a preamble:
  - Isolated pulses with regular spacing allow to acquire timing as quickly as possible so that duty cycling can start
  - Length 31 ternary preamble code
  - Synchronisation field consisting of 16, 64, 1024, 4096 symbols
  - Start of Frame Delimiter consisting of 8 symbols

# Preamble

Changes compared to  
15.4a:

All codes allowed in all  
channels to support  
more users

Only SFD length 8  
supported

## Preamble codes

```
-0000+0-0+++0+-000+-++00-+0-00
0+0+-0+0+000-++0-+-00+00++000
-+0++000-++0++0+00-0000-0+0-
0000+-00-00-++++0+-+000+0-0++0-
-0+-00+++-+000-+0++0-0+0000-00
++00+00---+0++-000+0+0-+0+0000
+0000+-0+0+00+000+0+---0-+00-
0+00-0-0++0000--+00-+0++-++0+00
```

# Synchronisation power estimate

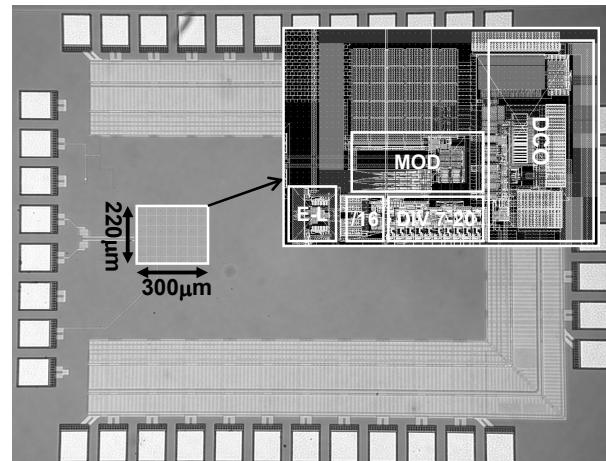
- Assumptions:
  - Length 4096 used as beacon.
  - RX requires 4 preamble symbols to complete synchronisation
  - RX power consumption 50 mW when on
- Duration preamble symbol:
  - $31 \times 16 \times 2 \text{ ns} = 992 \text{ ns} \sim 1 \mu\text{s}$
  - i.e. RX on: 4  $\mu\text{s}$
- Duration preamble:
  - $4096 \times 31 \times 16 \times 2 \text{ ns} = 4.06 \text{ ms} \sim 4 \text{ ms}$
- When seeking a beacon for the first time, the receiver needs to switch on for 4  $\mu\text{s}$  every 4 ms:
  - Duty cycle ratio 1/1000:
  - Average power consumption 50  $\mu\text{W}$

## PHY Header

- Contains parameters of the rest of the packet:
  - Modulation & rate: 12 options: 4 bits
  - Payload size: 0 .. 256 bytes: 9 bits
- Together 13 bits, protect with SECDED Hamming code used in 15.4a
- Results in 19 bits PHR
- Transmitted at 0.85 Mbps, except for 0.11 Mbps mode

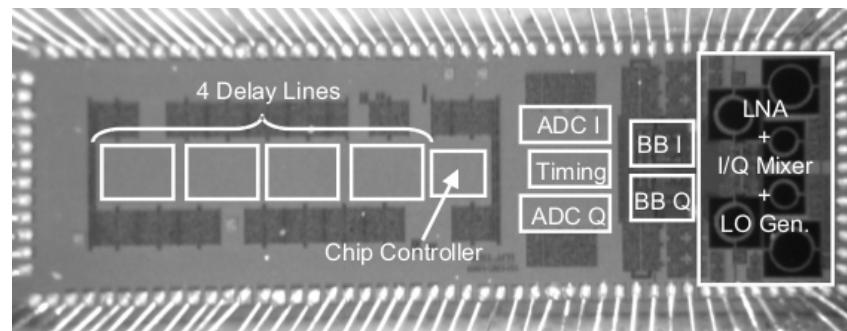
# Evidence of practical feasibility

- ICs in our labs - Published Material
- Full Transmitter in C90 CMOS
  - Fully Duty Cycled
  - 1 mW Power consumption (P mean)
- ISSCC 2007

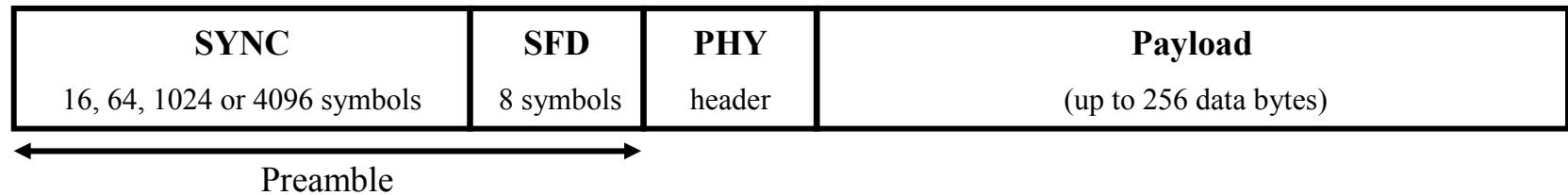


# Evidence of practical feasibility

- 180 nm CMOS UWB Receiver successfully demodulates UWB signal @ Low Power
  - 3.1 – 5 GHz (UWB lower band)
  - 30 mW Power Consumption
  - No Signal Duty Cycling
- ISSCC 2006



# Final overview



- **Preamble**
  - low cost synchronisation, below  $100 \mu\text{W}$
- **Burst position modulation:**
  - Low complexity non-coherent reception at low data rates
  - < 20 mW average @ 850 kbps
- **Concatenated burst modulation:**
  - extremely power efficient communication
  - < 10 mW average, up to 27.2 Mbps
- To be combined with the MAC proposal from doc: 15-09-0332-00-006.