Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: [IL Comments Resolution]

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Re: []

Abstract: [This document proposed resolutions to comments on DF02]

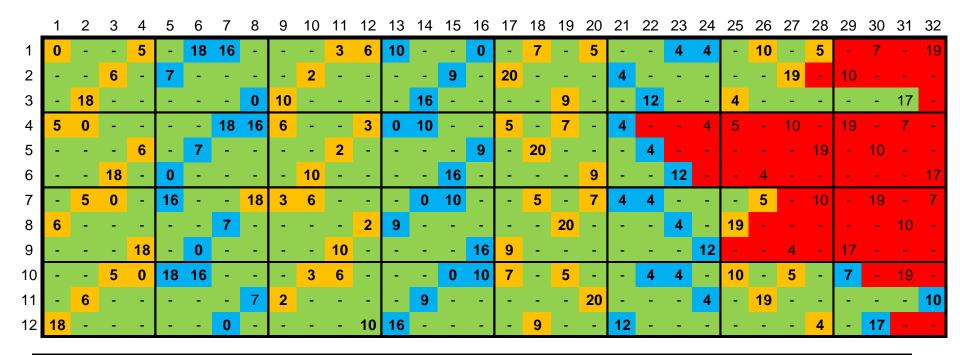
Purpose: [For consideration and discussion by IEEE 802.15 TG3C.]

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- Comment 103: There is no code rate between 1/2 and 3/4.
 This causes large jumps in the available rates.
- Suggested Resolution: Add the following LDPC rate 5/8 parity check matrix to both SC and HSI-OFDM

Rate 5/8 Parity Check Matrix



- Comment 158: how many total of beams and how it is encoded? (13.1.4, P.156, L26)
- Suggested Resolution: The current test read as follows:
 "Bits c1c0 shall encode the total number of beams in the horizontal direction (excluding the center beam)."

Replace with

"Bits c1c0 shall encode the total number of beams in the horizontal direction (excluding the center beam). The maximum number of beams (excluding the center beam) shall be 3 which corresponds to the setting c1c0=11."

 Comment 183: What does "Omni-directional antenna (no beam forming capability)" mean? Link budget for omnidirectional antenna? (7.4.11, P33, L23)

Suggested Resolution: Replace

"0 -> Omni-directional antenna (no beam forming capability)"

with

"0 -> Omni-directional antenna (no beam forming capability), i.e. and antenna covering the region of space of interest"

Comment 226: The receiver may require a large size of memory to buffer the payload before demodulation if LDPC encoding is used for the header because of LDPC decoding delay.

Suggested Resolution:

Assuming a master clock of 1728/8 = 216 MHz, an LDPC block code can be decoded in 48 iterations ~ 48/216e6 ~ 220 ns.

Using a higher master clock or lower number of iterations will decrease the decoding delay.

 Comment 234, 246, 238, 241, 243, 246, 249,251: Remove subclause 12.2.2.4 (Pad Bits) or remove from Table 106

Suggested Resolution:

- 12.2.5 Data field
 - The data field is the last component of the frame, and is constructed as shown in Figure 144. The data field shall be constructed as follows:
 - a) compute the FCS over frame payload,
 - b) form the data field by appending the 4-octet FCS to the frame payload,
 - c) scramble the resulting combination according to 12.2.5.1,
 - d) encode the scrambled data field into NFEC codewords as specified in 12.2.2.2. The number of FEC codewords is calculated as follows:

$$N_{FEC} = \left\lceil \frac{LENGTH \times 8}{L_{FEC} \times R_{FEC}} \right\rceil$$

where L_{FEC} is the FEC codeword length, LENGTH is the length of the frame payload defined in the header field (in octets), and R_{FEC} is the code rate. The FEC codeword length, L_{FEC} , is 2040 for the Reed Solomon FEC specified in 12.2.2.2.1, 672 for the irregular LDPC specified in 12.2.2.2.2, and 1440 for the rate 14/15 irregular LDPC specified in 12.2.2.3.

e) the encoded data field shall be concatenated with N_{PAD} pad bits in order to ensure that the resulting data field is aligned on the sub-block symbol boundary. The pad bits shall be set to zero and than scrambled using the continuation of the scrambler sequence that scrambled the frame payload and FCS in step a). The number of pad bits, N_{PAD} , shall be computed as follow. The number of encoded bits in the data field is given by:

$$N_{EBITS} = 8 \times (LENGTH + 4) + N_{FEC} \times (1 - R_{FEC})$$

The number of symbol sub-blocks, N_{SBLKS} , and the number of pad bits, NPAD, are calculated as follows:

$$\begin{split} N_{SBLKS} = & \lceil N_{EBITS} / N_{CBPS} \rceil \\ N = & N_{SBLKS} \times N_{CBPS} - N_{EBITS} \end{split}$$

where N_{CBPS} is the number of coded bits per symbol sub-block as specified in **Table 102p**.

- f) spread the encoded and scrambled data field using the appropriate spreading sequence as detailed in 12.2.2.3,
- g) map the resulting data field onto the appropriate constellation as specified in 12.2.2.1,
- h) build symbol sub-blocks from the spread data field according to 12.2.5.5.1,
- i) insert the PCES periodically as described in 12.2.5.5.2,
- j) apply a chip level $\pi/2$ -continous rotation to the resulting data field as described in 12.2.2.1.

12.3.2 Data field

The data field is the last component of the frame, and is constructed as shown in Figure 155.

The data field shall be constructed as follows:

- a) compute the FCS over frame payload,
- b) form the data field by appending the 4-octet FCS to the frame payload,
- c) scramble the resulting combination according to 12.3.2.2,
- d) encode the scrambled data field into NFEC codewords and interleave the result as specified in 12.3.2.3. The number of FEC codewords is calculated as follows:

$$N_{FEC} = \left\lceil \frac{LENGTH \times 8}{L_{FEC} \times R_{FEC}} \right\rceil$$

where L_{FEC} = 672 is the LDPC codeword length, *LENGTH* is the length of the frame payload defined in the header field (in octets), and R_{FEC} is the code rate.

e) the resulting data field shall be concatenated with N_{PAD} pad bits in order to ensure that the resulting data field is aligned on the OFDM symbol boundary. The pad bits shall be set to zero and than scrambled using the continuation of the scrambler sequence that scrambled the frame payload and FCS in step a). The number of pad bits, N_{PAD} , shall be computed as follow. The number of encoded bits in the data field is given by:

$$N_{EBITS} = 8 \times (LENGTH + 4) + N_{FEC} \times (1 - R_{FEC})$$

The number of OFDM symbols, N_{SBLKS} , and the number of pad bits, N_{PAD} , are calculated as follows:

$$N_{SBLKS} = \lceil N_{EBITS} / N_{CBPS} \rceil$$

$$N = N_{SBLKS} \times N_{CBPS} - N_{EBITS}$$

where N_{CRPS} is the number of coded bits per symbol sub-block as specified in Table 126.

- f) map the resulting data field onto the appropriate constellation as specified in 12.3.2.4,
- g) spread the QPSK and QAM modulated signal as described in Table 12.3.2.5
- h) interleave the data with the tone interleaver as described in 12.3.2.6,
- i) modulate the resulting complex values with the OFDM modulator described in 12.3.2.7, and
- j) insert PCES periodically as described in 12.3.2.8.

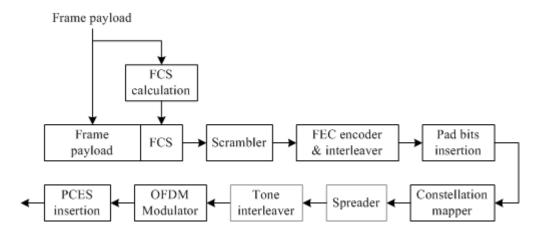


Fig 155. Data field construction process

- Comment 235: Simplify SC CES structure and sequences in the preamble (12.2.3, P.92)
- Suggested Resolution: (see next slide)

CMS preamble:

CES/SFD	SYNC
-b ₁₂₈ \mathbf{u}_{512} (repeated 6 times) - \mathbf{u}_{512} \mathbf{u}_{512}	a ₁₂₈ (repeated 64 times)

Long preamble:

Header with spreading 2

CES/SFD	SYNC
$\mathbf{-b}_{128}\mathbf{u}_{512}\mathbf{u}_{512}$	a ₁₂₈ (repeated 32 times)

Header with spreading 8

CES/SFD	SYNC
$+\mathbf{b}_{128}\mathbf{v}_{512}\mathbf{v}_{512}$	\mathbf{a}_{128} (repeated 32 times)

Short preamble

CES/SFD	SYNC
$-\mathbf{b}_{128}\mathbf{u}_{512}$	a ₁₂₈ (repeated 8 times)

Transmission direction

•
$$\mathbf{u}_{512} = [+\mathbf{a}_{256} + \mathbf{b}_{256}], \, \mathbf{v}_{512} = [-\mathbf{a}_{256} + \mathbf{b}_{256}],$$

•
$$\mathbf{b}_{256} = [-\mathbf{a}_{128} - \mathbf{b}_{128}], \, \mathbf{a}_{256} = [\mathbf{a}_{128} - \mathbf{b}_{128}], \, \text{PCES} = [\text{CES/SFD } \mathbf{a}_{128}]$$

- Comment 236, 247, 248: Simplify OFDM CES structure and sequences (12.2.2.4), Is there a need for short and long CES?
- Suggested Resolution:

Long preamble:

CES/SFD	SYNC
$-\mathbf{b}_{128} \mathbf{u}_{512}$ (repeated 10 times) $-\mathbf{u}_{512} \mathbf{u}_{512}$	a ₁₂₈ (repeated 128 times)

Short preamble:

CES/SFD	SYNC
$-\mathbf{b}_{128}\mathbf{u}_{512}\mathbf{u}_{512}$	a ₁₂₈ (repeated 16 times)

PCES: [CES/SFD a₁₂₈]

 Comment 239: Restrict usage of long preamble to common mode only, same for base header (12.2.4.1)

Suggested Resolution:

Long preamble renamed CMS preamble.

Base header rate of 12.3 Mbps is used only with CMS.

- Comment 256: Is SAS needed? If not remove from beamforming
- Suggested Resolution:

Yes it is needed. No change.