Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: [TensorCom Physical Layer Proposal]
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Re: [This submission is in response to the TG3C call for Proposals (IEEE P802.15-07-0586-02-003c)]

Abstract: [This document describes the Tensorcom physical layer proposal for IEEE 802.15 TG3C.]

Purpose: [For considereation and discussion by IEEE 802.15 TG3C.]

TensorCom Physical Layer Proposal Dual-Mode Single Carrier / OFDM

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Outline

- PHY key features
- Channelization
- Common Preamble
- Unified Frame format
- Single Carrier Mode
- OFDM Mode
- Selected responses to the selection criteria
- Summary

PHY Key Features

- Dual-mode SC (Single Carrier) / OFDM for different classes of devices and different applications;
- Low-complexity interoperability common mode for interoperability between different devices/networks;
- Unified common frame format enabling a single HW supporting SC / OFDM;
- Link Adaptation & Unequal Error Protection via low – complexity Structured Turbo LDPC / RS;
- Balanced Channelization with multiple XTAL support.

Channelization

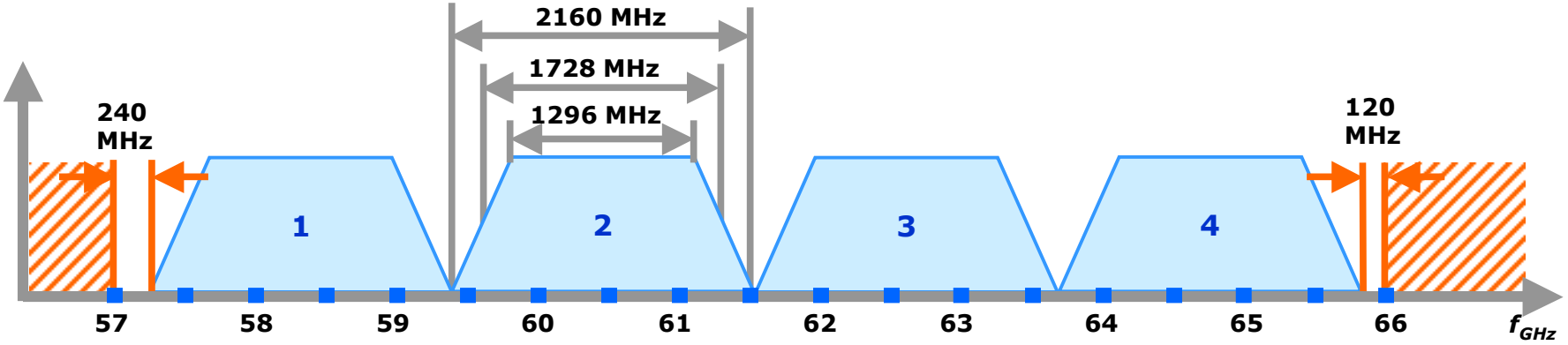
- Desired Features
- Band Plan
- Direct conversion PLL Reference Diagram
- Heterodyne PLL Reference Diagram: Variable IF
- Heterodyne PLL Reference Diagram: Fixed IF

Channelization Desired Features

- Use “free spectrums” of Japan, USA, Korea & EU
- Support for 4 channels in the available spectrum
- Channel Separation in the order of 2 GHz
- Single/Dual integer PLL that generates all necessary frequencies using direct synthesis
- Support of multiple PLL architectures (Direct conversion, double conversion)
- High Frequency Dividers should be in power of 2 : low-frequency dividers can be programmable
- Support of multiple crystals including at least one cell crystal & one high frequency crystal

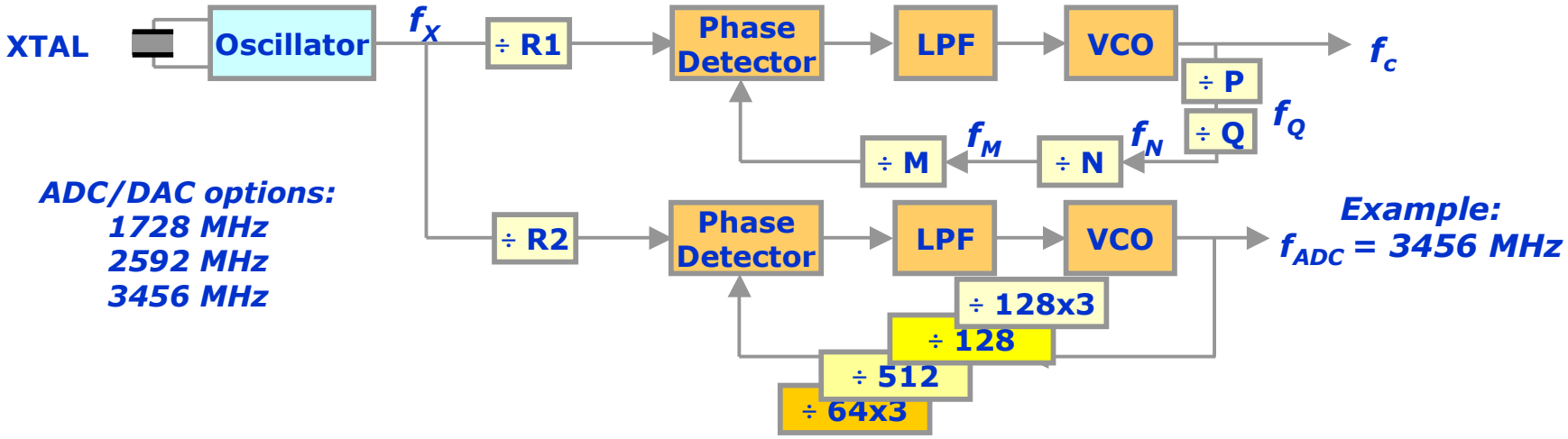
Channelization

Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	3 dB BW (MHz)	Roll-Off Factor
1	57.240	58.320	59.400	1728	0.25
2	59.400	60.480	61.560	1728	0.25
3	61.560	62.640	63.720	1728	0.25
4	63.720	64.800	65.880	1728	0.25



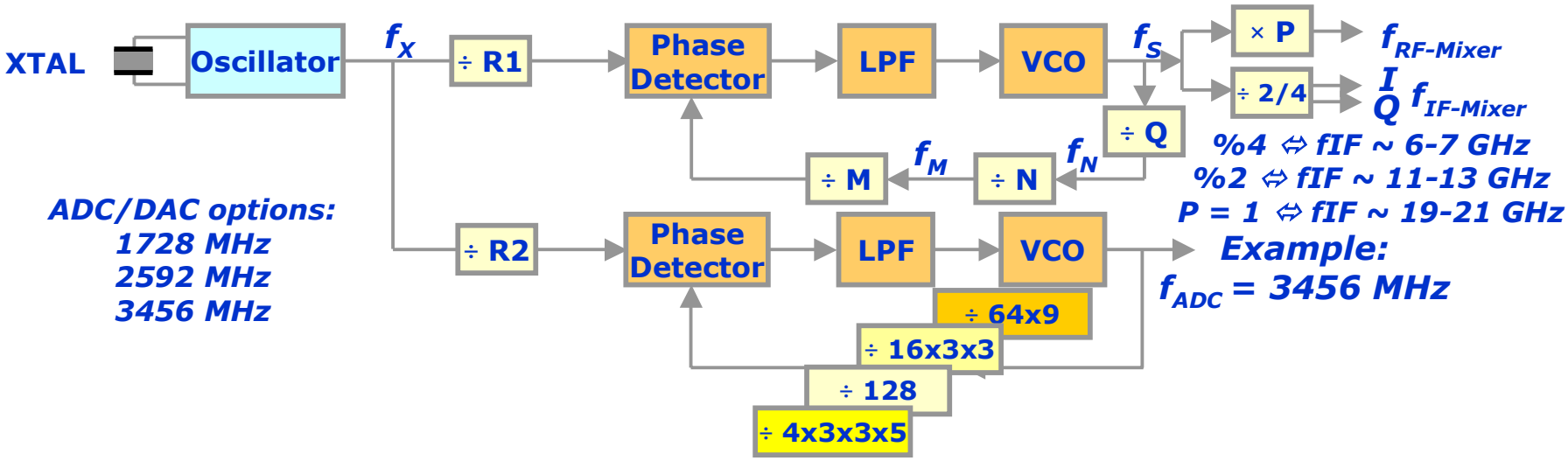
- Support Cell phone XTAL: **15 MHz**, **18 MHz**, **19.2 MHz & 24 MHz** & Other High frequency XTALs: 22.5, 27, 30, 33.75, 36, 45, 54MHz, …
- Balanced margins to 57/66 GHz & Good roll-off factor
- Supports Multiple PLL Architectures even with the Cell phone XTAL
- Dual PLL: High frequency PLL that generates carrier frequencies
- Low frequency PLL that generates the ADC/DAC & ASIC frequencies

Direct Conversion PLL Reference Diagram



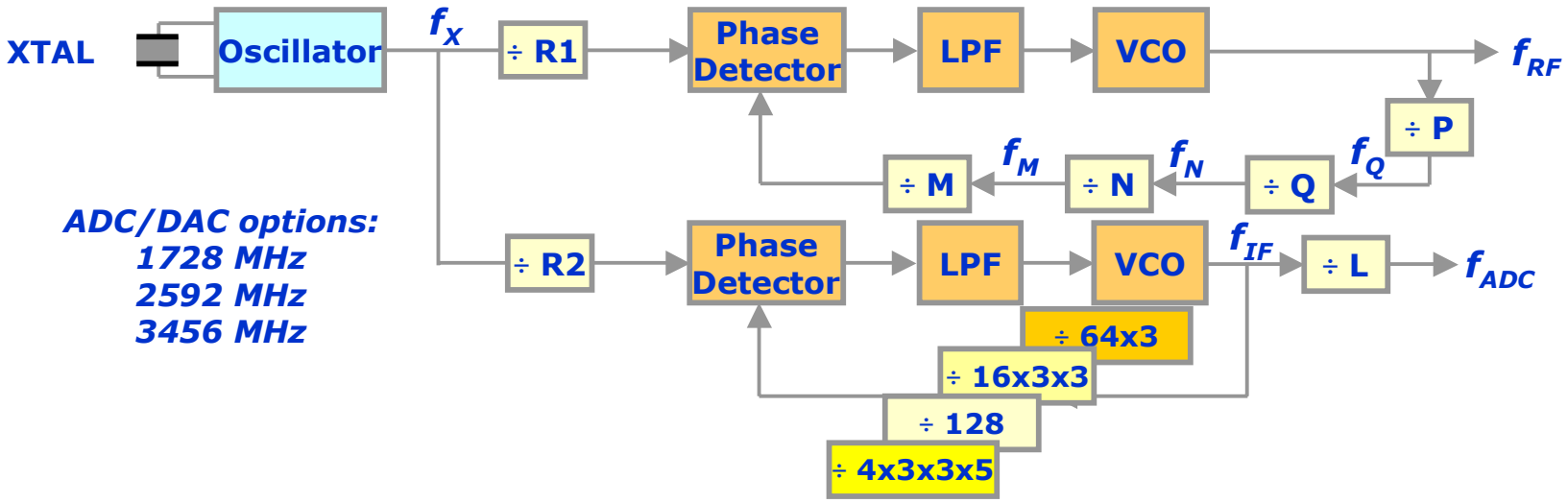
f_c (GHz)	f_X (MHz)	f_Q(GHz)	f_N (MHz)	f_M (MHz)	R1	P	Q	N	M	R2
58.320	15	3.645	1215	405	1	16	3	3	3×3 ×3	5
60.480	15	3.780	1260	420	1	16	3	3	2×2 ×7	5
62.640	15	3.915	1305	435	1	16	3	3	29	5
64.800	15	4.050	1350	450	1	16	3	3	2×3 ×5	5
58.320	18	7.290	2430	486	1	8	3	5	3×3×3	1
60.480	18	7.560	2520	504	1	8	3	5	2×2×7	1
62.640	18	7.830	2610	522	1	8	3	5	29	1
64.800	18	8.100	2700	540	1	8	3	5	2×3×5	1
58.320	22.5	1.82250	607.50	607.50	1	32	3	1	3×3×3	5
60.480	22.5	1.89000	630.00	630.00	1	32	3	1	2×2×7	5
62.640	22.5	1.95750	652.50	652.50	1	32	3	1	29	5
64.800	22.5	2.02500	675.00	675.00	1	32	3	1	2×3×5	5
58.320	27	3.645	729	729	1	16	5	1	3×3×3	1
60.480	27	3.780	756	756	1	16	5	1	2×2×7	1
62.640	27	3.915	783	783	1	16	5	1	29	1
64.800	27	4.050	810	810	1	16	5	1	2×3×5	1

Heterodyne PLL Reference Diagram: Variable IF



f_C (GHz)	f_X(MHz)	f_S (GHz)	f_{IF} (GHz)	f_N (MHz)	f_M(MHz)	R1	P	Q	N	M	R2
58.320	15	25.920	6.480	405	405	1	2	64	1	3x3x3	5
60.480	15	26.880	6.720	420	420	1	2	64	1	2x2x7	5
62.640	15	27.840	6.960	435	435	1	2	64	1	29	5
64.800	15	28.800	7.200	450	450	1	2	64	1	2x3x5	5
58.320	18	23.328	11.664	1458	486	1	2	16	3	3x3x3	1
60.480	18	24.192	12.096	1512	504	1	2	16	3	2x2x7	1
62.640	18	25.056	12.528	1566	522	1	2	16	3	29	1
64.800	18	25.920	12.960	1620	540	1	2	16	3	2x3x5	1
58.320	22.5	38.880	19.440	607.50	607.50	1	1	64	1	3x3 x3	5
60.480	22.5	40.320	20.160	630.00	630.00	1	1	64	1	2x2 x7	5
62.640	22.5	41.760	20.880	652.50	652.50	1	1	64	1	29	5
64.800	22.5	43.200	21.600	675.00	675.00	1	1	64	1	2x3 x5	5
58.320	27	23.328	11.664	729	729	1	2	32	1	3x3x3	1
60.480	27	24.192	12.096	756	756	1	2	32	1	2x2x7	1
62.640	27	25.056	12.528	783	783	1	2	32	1	29	1
64.800	27	25.920	12.960	810	810	1	2	32	1	2x3x5	1

Heterodyne PLL Reference Diagram: Fixed IF



f_c (GHz)	f_X(MHz)	f_{RF} (GHz)	f_{IF} (GHz)	f_Q (MHz)	f_N(MHz)	f_M(MHz)	R1	P	Q	N	M	L	R2
58.320	15	49.680	8.640	3105	1035	1035	1	16	3	3	23	5	1
60.480	15	51.840	8.640	3240	1080	1080	1	16	3	3	2x2x2x3	5	1
62.640	15	54.000	8.640	3375	1125	1125	1	16	3	3	5x5	5	1
64.800	15	56.160	8.640	3510	1170	1170	1	16	3	3	2x13	5	1
58.320	18	51.408	6.912	6426	2142	306	1	8	3	7	17	4	1
60.480	18	53.568	6.912	6696	2232	558	1	8	3	4	31	4	1
62.640	18	55.728	6.912	6966	2322	774	1	8	3	3	43	4	1
64.800	18	57.888	6.912	7236	2412	1206	1	8	3	2	67	4	1
58.320	22.5	49.680	8.640	1552.50	517.50	517.50	1	32	3	1	23	5	1
60.480	22.5	51.840	8.640	1620.00	202.50	67.50	1	32	8	3	3	5	1
62.640	22.5	54.000	8.640	1687.50	562.50	112.50	1	32	3	5	5	5	1
64.800	22.5	56.160	8.640	1755.00	877.50	292.50	1	32	2	3	13	5	1
58.320	27	51.408	6.912	3213	459	459	1	16	7	1	17	4	1
60.480	27	53.568	6.912	3348	837	837	1	16	4	1	31	4	1
62.640	27	55.728	6.912	3483	1161	1161	1	16	3	1	43	4	1
64.800	27	57.888	6.912	3618	1809	1809	1	16	2	1	67	4	1

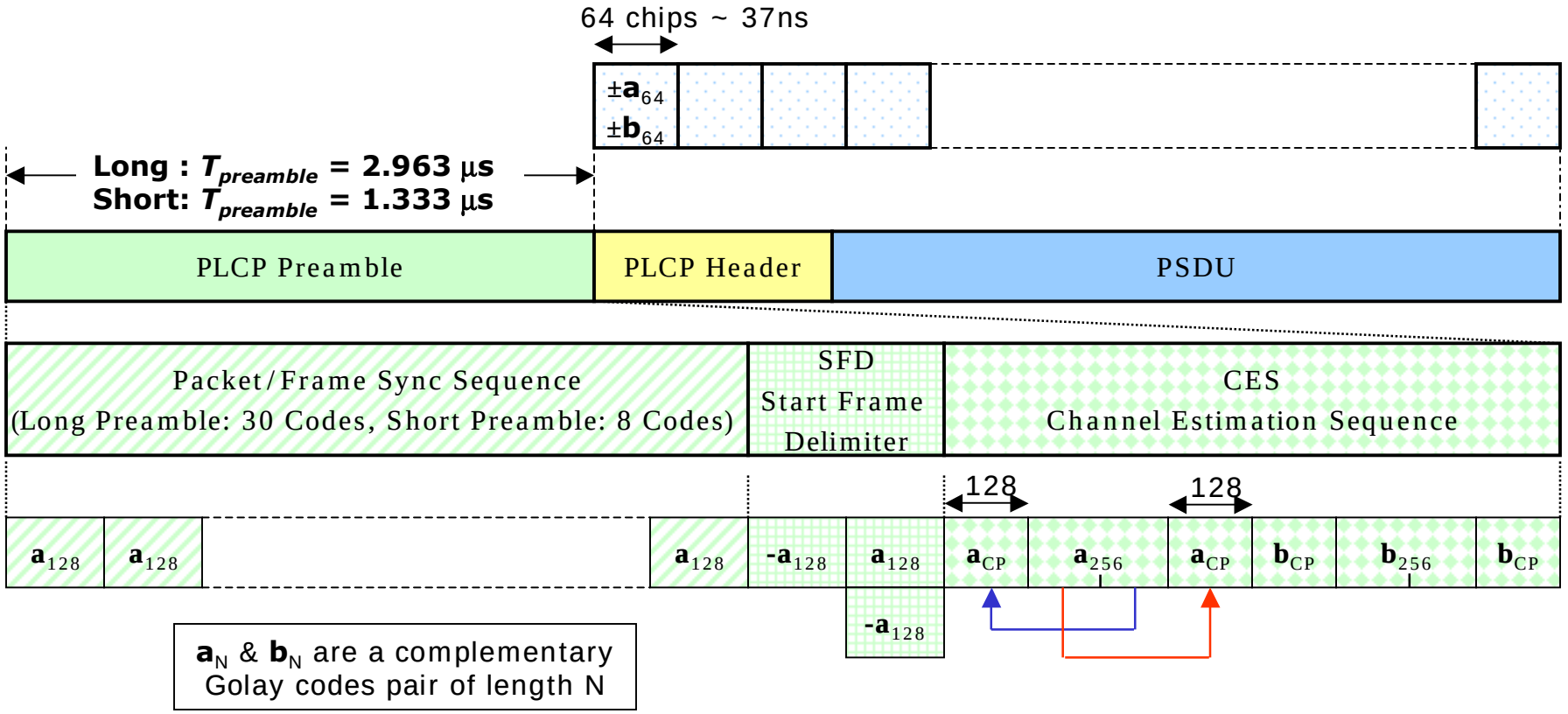
Common Mode

- Common Mode Highlights
- Preamble Structure & Frame Format
- Rate, Timing & Frame Related Parameters
- Transmitter Reference Diagram
- Spreading Codes & Properties
- The Modulator & Mapper
- The Reed Solomon FEC
- The Scrambler
- The Frame & Header Check Sequences
- The Pulse Shaper

Common Mode Highlights

- Definition: Common Mode (CM) is a Base Rate (BR) Mode that is mandatory for all devices
- Usage: CM is used for beaconing, signaling and for BR data packets
- Common mode: necessary for interoperability between different devices & different networks
- Modulation: Golay symbols with chip level $\pi/2$-DBPSK
- Pulse Shaping: left to the implementer
  - Example 1: GMSK or Linearized GMSK pulse with BT=0.5 (recommended);
  - Example 2: Square-root raised cosine with roll-off=0.25 with clipping /lifting;
  - Example 3: Square-root raised cosine with roll-off=0.25 without clipping
- Coding: Shortened Reed-Solomon from RS(255,239)
- Spreading Codes:
  - length 128 codes ($\mathbf{a}_{128}$ & $\mathbf{b}_{128}$) used for SYNC & SFD fields
  - length 256 codes ($\mathbf{a}_{256}$ & $\mathbf{b}_{256}$) used for CES
  - length 064 codes ($\mathbf{a}_{064}$ & $\mathbf{b}_{064}$) used for Header and data

Preamble Structure & Frame Format



- Long preamble is the default preamble;
- PNC switch from long preamble to short preamble upon Device request (implicit or explicit)
- Header & PSDU are spread using Golay codes $\mathbf{a}_{64}$ & $\mathbf{b}_{64}$. Each symbol carries 2 bits of information

PSDU Rate & Timing Parameters

Common Mode: PSDU Rate-Dependent Parameters							
Chip Rate Rchip : **MHz**	**Modulation Scheme**	**Spreading Length: L**	**FEC Rate**	**Base Rate MSps**	**Bits per Symbol**	**Base Date Rate Mbps**	**Manatory or Optional**
1728	π/2-BPSK/GMSK	64	0.933	27	2	50.400	**Mandatory**

- MSps = Mega Symbols per second
- Mbps = Mega bits per second
- FEC = RS(240,224), Rate = 224/240 = 0.933

Common Mode: Timing-Related Parameters

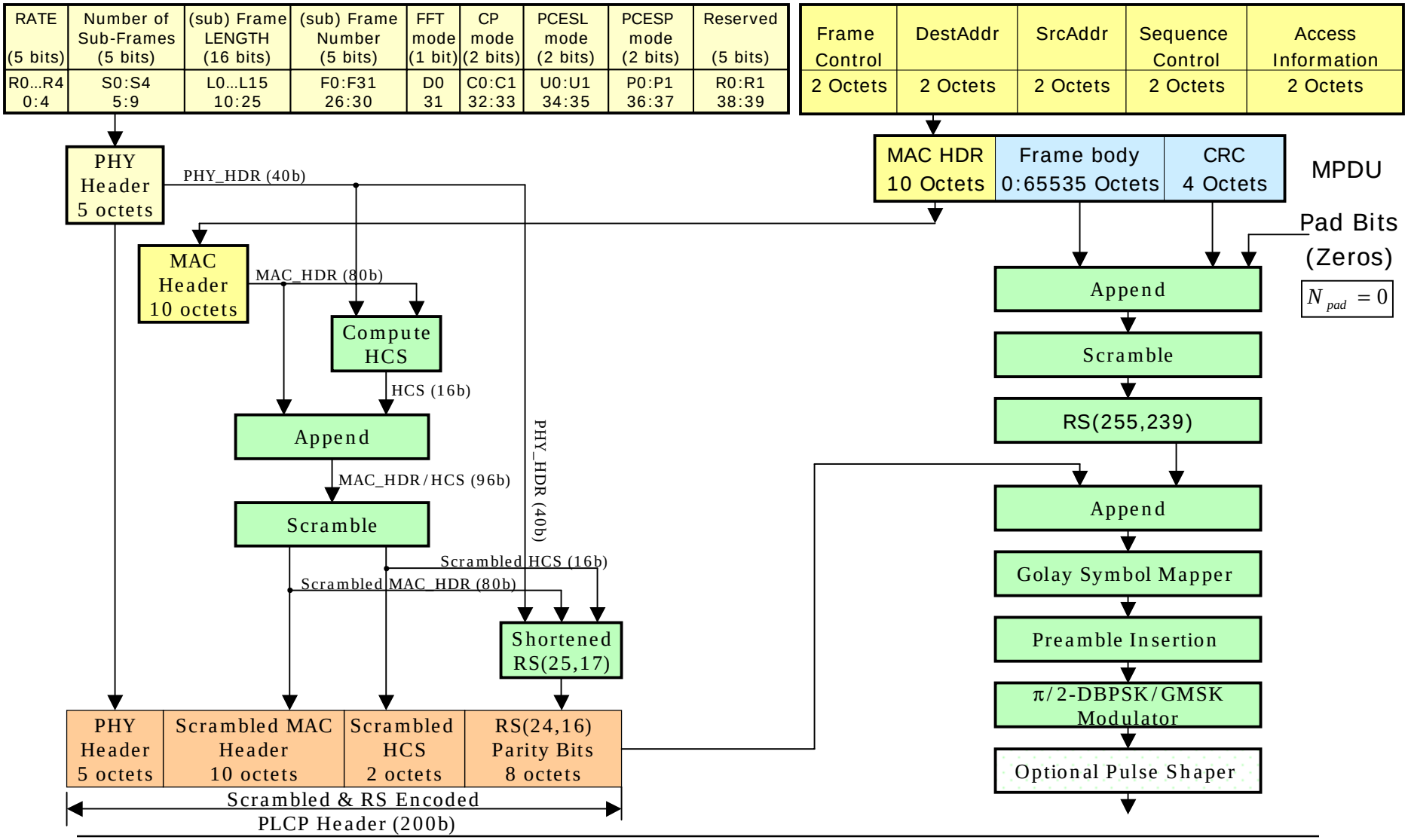
Parameter	Description	value	Unit
R_c	*Chip rate*	1728	MHz
T_c	*Chip duration*	0.579	ns
N_{psym}	*Preamble symbol length (chips)*	128	Chips
T_{psym}	*Preamble symbol duration*	74.074	ns
N_{cesym}	*CES symbol length (chips)*	256	Chips
T_{cesym}	*CES symbol duration*	148.148	ns
N_{dsym}	*Data symbol length (chips)*	64	Chips
T_{dsym}	*Data symbol duration*	37.037	ns
N_{cRS}	*Reed Solomon block length (chips)*	1856	Chips
T_{RSblk}	*Reed Solomon block duration*	1.074	µs

PSDU Frame Dependent Parameters

Common Mode: Frame-Related Parameters

Parameter	Description	Value				Unit
N_{sync}	*Number of symbols in the packet sync sequence*	Default mode:	30	Fast mode:	8	**a**128
T_{sync}	*Duration of the packet sync sequence*	Default mode:	2.222	Fast mode:	0.593	µs
N_{sfd}	*Number of symbols in the frame sync sequence*	2				**a**128
T_{sfd}	*Duration of the frame sync sequence*	0.148				µs
N_{ces}	*Number of symbols in the channel estimation sequence*	4				**a**256/**b**256
T_{ces}	*Duration of the channel estimation sequence*	0.593				µs
N_{pre}	*Number of equivalent symbols in the PLCP preamble*	Default mode:	40	Burst mode:	18	128 chips symbols
T_{pre}	*Duration of the PLCP preamble*	Default mode:	2.963	Burst mode:	1.333	µs
N_{phdr}	*Number of symbols in the PHY header*	40				**a**64/**b**64
T_{phdr}	*Duration of the PHY header*	0.741				µs
N_{mhdr}	*Number of symbols in the MAC header*	80				**a**64/**b**64
T_{mhdr}	*Duration of the MAC header*	1.481				µs
N_{chdr}	*Number of symbols in the header HCS & RSP*	80				**a**64/**b**64
T_{chdr}	*Duration of the header HCS & RSP*	1.481				µs
N_{hdr}	*Number of symbols in the frame header*	200				**a**64/**b**64
T_{hdr}	*Duration of frame header*	3.704				µs
N_{RSblk}	*Number of Reed Solomon Blocks in the frame*	ceil[(LENGTH + 4)/224]				RS blocks
N_{pad}	*Number of zero pad octets*	$224 \times N_{RSblk}$ - (LENGTH + 4)				octets
N_{frame}	*Number of symbols in the frame*	$N_{RSblk} \times 240$				128 chips symbols
T_{frame}	*Duration of the frame*	$N_{frame} \times T_{dsym}$				µs
$N_{cpacket}$	*Number of chips in the packet*	$N_{frame} \times 8 \times 32$				chips

Transmitter Reference Block Diagram



Spreading Codes: Desired Features

- Quasi-perfect code: Low SLL (Side Lobe Level) and wide ZCZ (Zero Correlation Zone) for improved Detection
- Perfect code for channel estimation, i.e. zero SLL
- Binary codes (1 bit DAC versus multi-bit DAC)
- Zero-mean codes for improved DC offset cancellation
- Selected code should support a parallel Low complexity matched filter architecture
- Maximum code length of 128 for multiple XTALs support (up to 50 ppm, ±25 ppm @ Tx/Rx).
- Should support SC & OFDM

Spreading Codes

- Golay complementary codes of various length N ($\mathbf{a}_N$,$\mathbf{b}_N$) are the spreading codes of choice
- Each code has a low SLL and a wide ZCZ
- The combination of their periodic & aperiodic autocorrelation provides a perfect code
- Only 1 bit DAC & 1 bit ADC
- Admit a very low-complexity highly parallelizable architecture
- Key enabler for a low complexity synchronization, channel estimation & above all a common mode engine

Spreading Codes summary

- SYNC/SFD codes:
  - $\mathbf{a}_{128}$ = [05C99C5005369CAFFA3663AF05369CAF]
  - $\mathbf{b}_{128}$ = [F5396CA0F5C66C5F0AC6935FF5C66C5F]
- CES codes:
  - $\mathbf{a}_{256}$ = [TBD]
  - $\mathbf{b}_{256}$ = [TBD];
- Header & Data codes:
  - $\mathbf{a}_{64}$ = [DE21212174748B74];
  - $\mathbf{b}_{64}$ = [2ED1D1D184847B84];
- Note : Hexadecimal convention: 5 = “0101” (i.e. MSB to LSB)

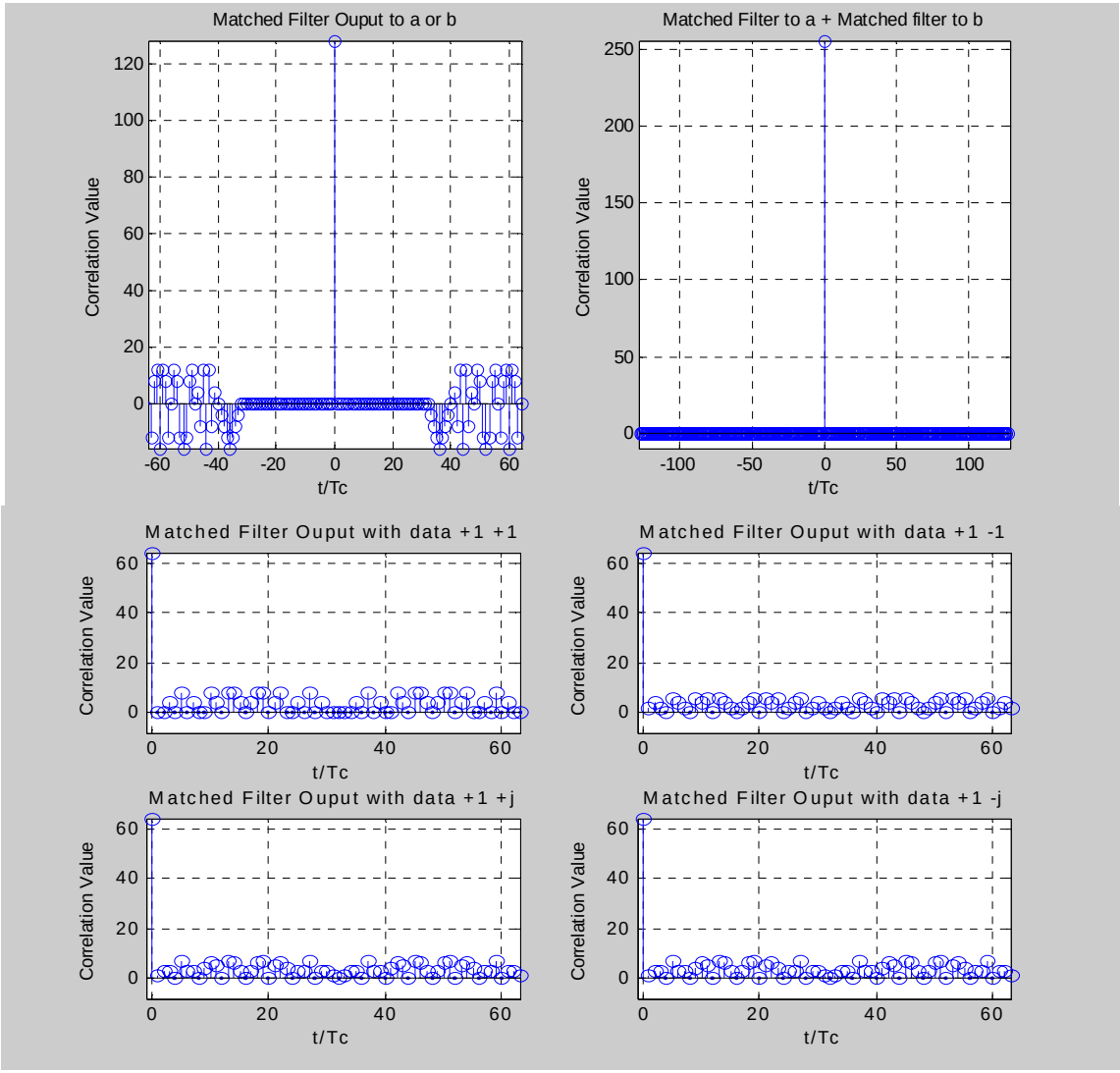
Spreading Codes Properties

Preamble Golay codes

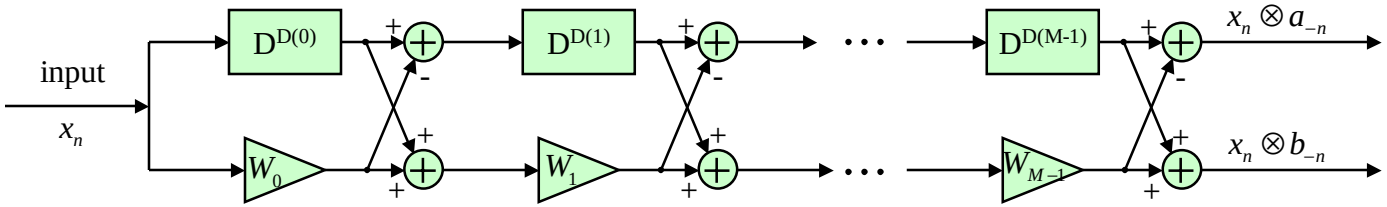
- **D** = [64 32 8 2 16 1 4];
- **W** = [++++-++]
- $\mathbf{a}_{128}$ = [05C99C5005369
- CAFFA3663AF05369CAF]
- $\mathbf{b}_{128}$ = [F5396CA0F5C6
- 6C5F0AC6935FF5C66C5F]

Header/Data Golay codes

- **D** = [16 8 32 16 1 4];
- **W** = [+-+-++]
- $\mathbf{a}_{64}$ = [DE21212174748B74];
- $\mathbf{b}_{64}$ = [2ED1D1D184847B84];



Spreading Codes Implementation

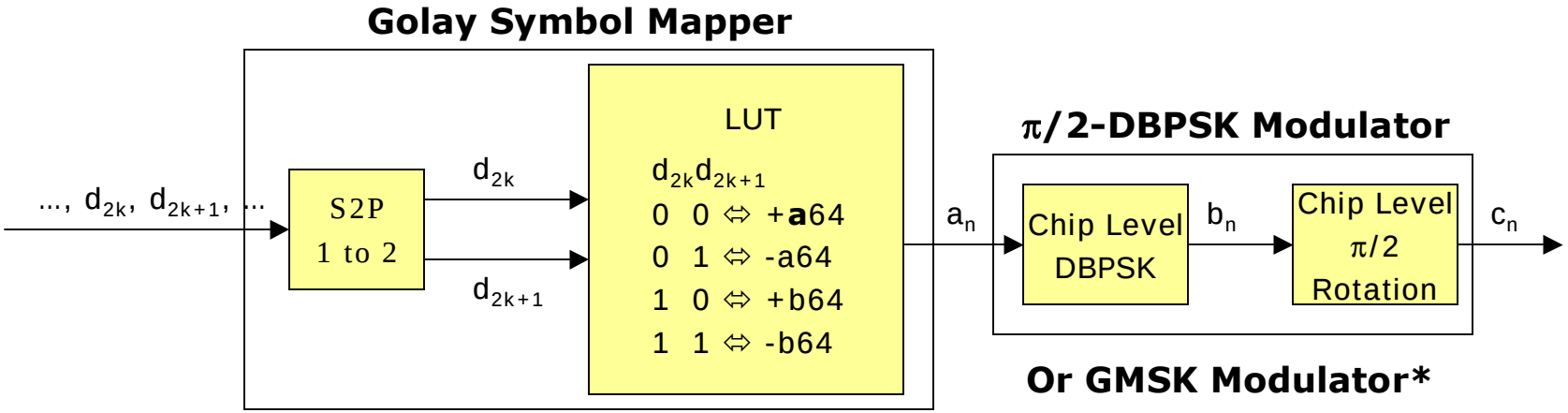


- Each Delay vector **D** and weight vector **W** specify a pair of complementary Golay codes
- Highly efficient Golay matched filter with only 14 adders for a length 128 code ("Budisin")
- It provides simultaneous matched filtering with the two complementary codes at once.
- Enables same preamble for SC, OFDM & interoperability common mode

Matlab Code

```
function [a,b] = golaySub(M,N,D,W);
a = [1 zeros(1,N-1)];b = a;
for m=1:M,
    ii = mod([0:N-1]-D(m),N);
    an = W(m)*a + b(ii+(1));
    bn = W(m)*a - b(ii+(1));
    a = an;b = bn;
end;
return;
```

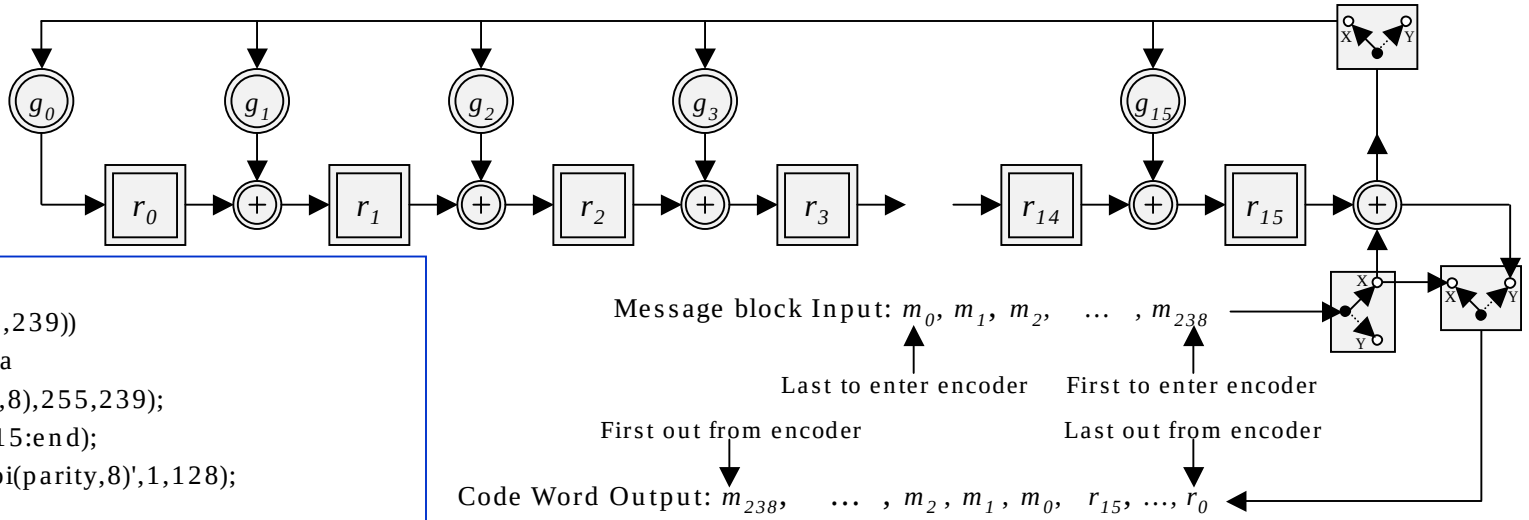
The Modulator & Mapper



- Mapping:
  - Each set of 2 bits will select which Golay code is to be transmitted
  - One symbol = 64 chips
  - One symbol carries 2 bits of information
  - Effective spreading factor ⇔ 32
  - Modulation used for both header and data
- Differential Encoder:
  - Chip level differential encoder: $b_n = b_{n-1} \oplus a_n$ with $b_{n-1} = 0$
- Rotator:
  - Chip level π/2-rotation: $c_n = j^n b_n$

*I. Lakkis, J. Su, & S. Kato, "A Simple Coherent GMSK Demodulator", PIMRC 2001

The Reed Solomon FEC over GF(2^8)



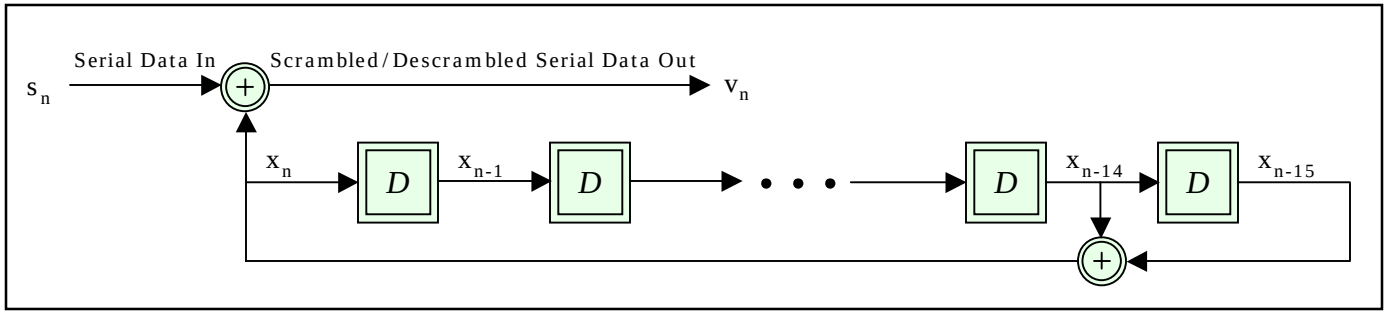
matlab code

```
data     = round(rand(8,239))
data     = (2.^[0:7])*data
parity   = rsenc(gf(data,8),255,239);
parity   = parity(:,end-15:end);
parity   = reshape(de2bi(parity,8)',1,128);
code     = [data parity];
```

- **Encoding Operation**
  - *Step 1.* Reset Shift Register (SR) to all zeros.
  - *Step 2.* The 3 switches are placed in position X and the K = 239 message symbols are fed into the encoder in order of decreasing index; the *K* message symbols are simultaneously sent out.
  - *Step 3.* After the last message symbol (m_0) has been fed into the Shift Register (SR), the switches are moved to position Y. At this point the SR contain the remainder generated by the division operation. These symbols are then shifted out of the SR.

- **Systematic Encoding for an RS(K+16,K) shortened from RS(255,239) over GF(2^8)**
  - Primitive polynomial: $P(z) = z^8 + z^4 + z^3 + z^2 + 1$ with root $z = 00000010$
  - *Generator polynomial:* $g(x) = \prod_{i=1:16}(x - z^i)$
  - *Symbol representation:* $m = b_7z^7 + b_6z^6 + \ldots + b_0 = [b_7b_6\ldots b_0]$ where b_7 is the msb and b_0 is the lsb
  - message polynomial: $m(x) = m_0 + m_1 x + \ldots + m_{238}x^{238}$ with $(m_{K:238} = 0)$
  - *Step 1. Multiply the message polynomial m(x) by x^{16}, $m(x)x^{16} = [0\ 0\ \ldots\ 0\ m_0\ m_1\ \ldots\ m_{238}]$*
  - *Step 2. Divide $x^6m(x)$ by g(x). Let r(x) be the remainder: $x^{16}m(x) = q(x)\ .g(x) + r(x)$*
  - *Step 3. Set $c(x) = x^{16}m(x) + r(x)$, i.e. $c(x) = [m_{238}\ldots m_K\ m_{K-1}\ \ldots\ m_0\ r_{15}\ldots\ r_0]$, m_{K-1} is transmitted first & r_0 is transmitted last in time*

The Scrambler

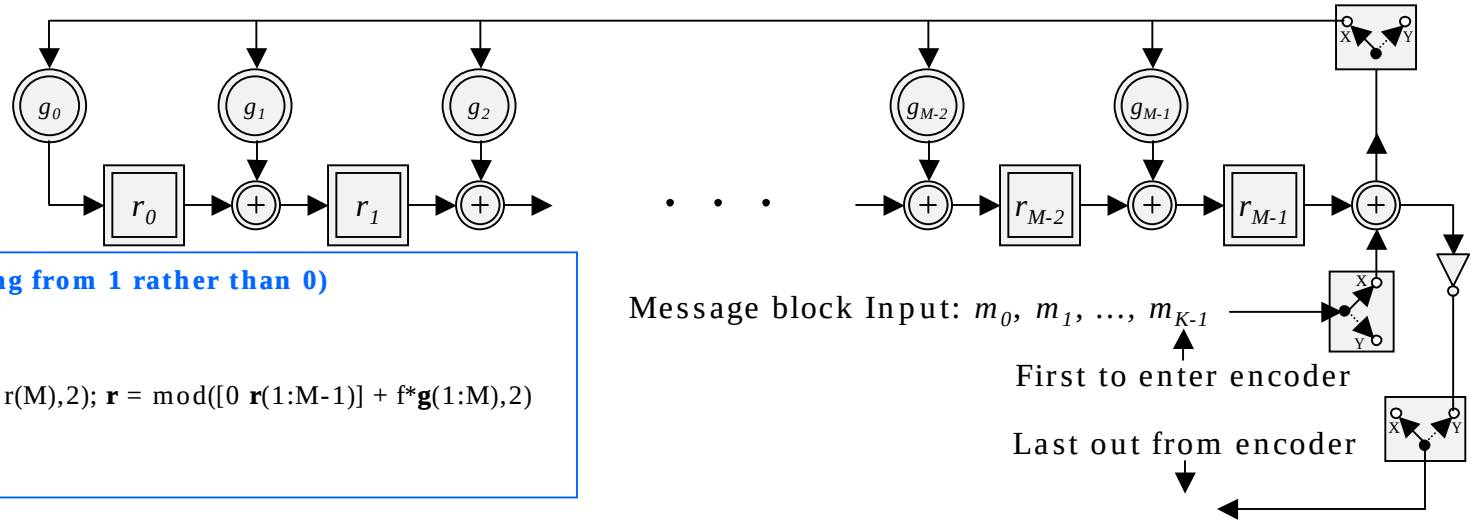


Seed Value: $x_{init} = [x_{-1}\ x_{-2} \ldots x_{-15}]$	PRBS out first 16 bits: $[x_0\ x_1 \ldots x_{15}]$
0011 1111 1111 111	0000 0000 0000 1000

matlab code

```
function [dataOut] = tcScrambler(dataIn,Fast)
shiftRegister  = [0 0 ones(1,13)];
for k = 0:length(dataIn) -1,
            feedback       = xor( shiftRegister(13+(1)) ,
            shiftRegister(14+(1)) );
            dataOut(k+(1))  = mod(dataIn(k+(1))+feedback , 2);
            shiftRegister   = [feedback shiftRegister([0:13]+(1))];
end;
return;
```

The FCS & HCS



matlab code (indexing from 1 rather than 0)

```
r = ones(1,M);
for k = 1:K,
        f = mod(d(k) + r(M),2); r = mod([0 r(1:M-1)] + f*g(1:M),2)
end;
r = xor(r(M:-1:1),1)
```

- **Encoding Operation**
  - *Step 1.* Reset Shift Register (SR) to all ones.
  - *Step 2.* The 3 switches are placed in position X and the *K* bits are fed into the encoder.
  - *Step 3.* After the last bit (m_0) has been fed into the Shift Register (SR), the switches are moved to position Y. At this point the SR contains the CRC bits. These bits are then shifted out of the SR and complemented.

- **FCS: MAC Frame Payload (M = 32)**
  - *FCS generator polynomial:*

    $g(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
    $= [11101101101110001000011001000001]$
  - MAC payload message polynomial:

    $m(x) = m_0 + m_1 x + \ldots + m_{K-1}x^{K-1}$ *with* (m_{K-1} = *lsb of first octet of MAC payload*)

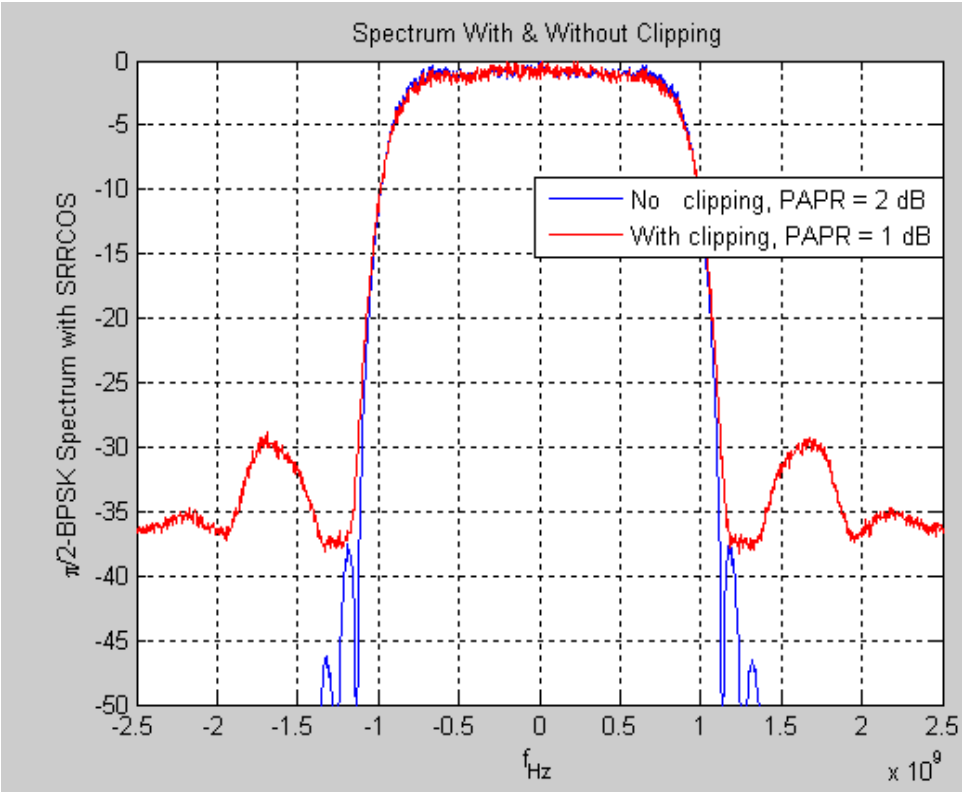
- **HCS: PHY & MAC headers (M = 16)**
  - *FCS generator polynomial:*

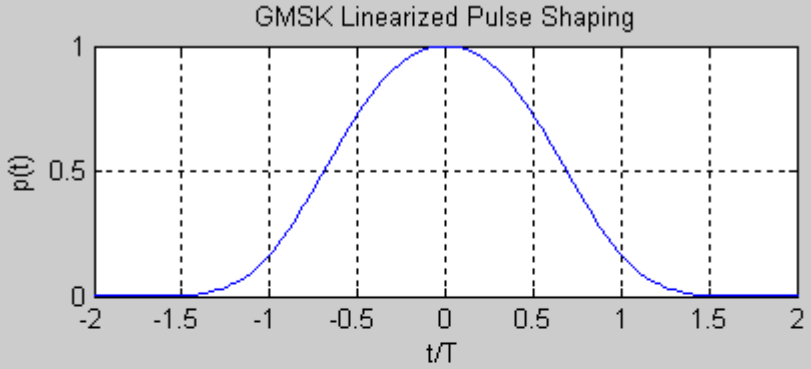
    $g(x) = x^{16} + x^{12} + x^5 + 1 = [10000100000010001]$
  - PHY & MAC headers polynomial (m_{119} *is first bit of PHY header &* m_0 *is last bit of MAC header)*

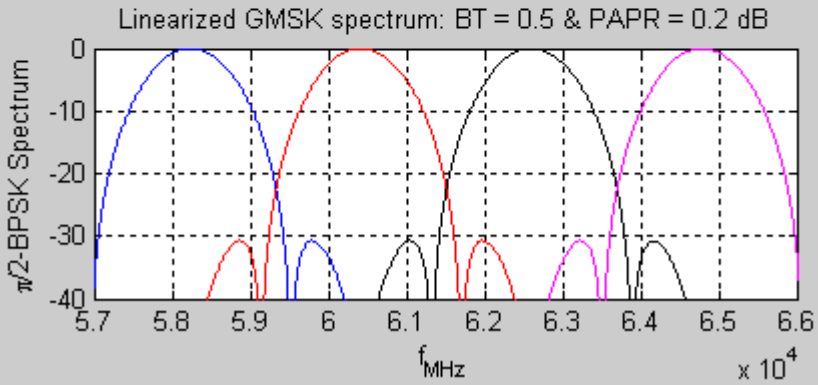
    $m(x) = m_0 + \ldots + m_{79}\,x^{79} + m_{80}\,x^{80} + \ldots + m_{119}x^{119}$

The Pulse Shaper

- The Pulse shaper is left up to the implementer. It can be implemented in digital and/or analog. Examples:
  - 1. GMSK or Linearized GMSK pulse with BT=0.5 (recommended);
  - 2. pure GMSK with BT = 0.5 (recommended);
  - 2. Square-root raised cosine with roll-off=0.25 with clipping /lifting;
  - 3. Square-root raised cosine with roll-off=0.25 without clipping



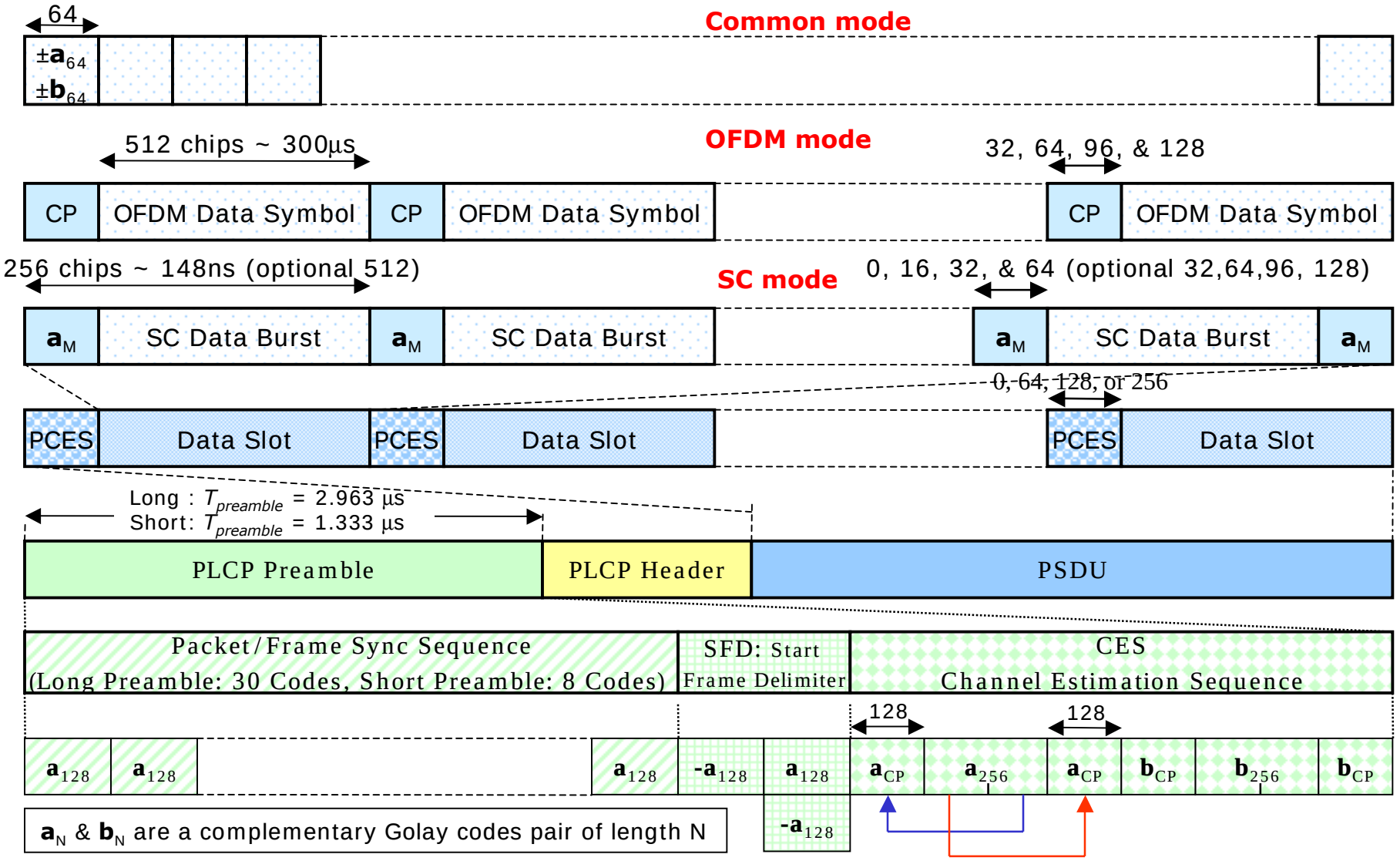




Unified Frame Format

- Unified Frame Format
- Key Features
- Frame Format: Single Carrier
- Frame Format: OFDM
- Frame Format: Common Mode

Unified Frame Format Concept



Unified Frame Format Features

- A PCES (Pilot CES) field is transmitted periodically to reacquire the channel in both SC and OFDM;
- Variable length Golay codes are used for this field;
- Preamble HW is reused during re-acquisition ⇔ no extra cost
- Mode specific frequency/timing tracking
  - Pilot tones for OFDM
  - CP as a known Golay code for SC
- Highly complex channel tracking is no longer needed
- The OFDM FFT(512) engine can be implemented as 2 smaller FFT(256) engines allowing HW reuse in SC mode with FDE (Frequency domain Equalization) which requires FFT(256) & IFFT(256)

Frame Format: Single Carrier

- The modulation of choice for low complexity low power devices
- Support for 3 device classes:
  - Class I (LDR): Low-Data-Rate, Low-power, low-complexity (Constant Envelope option) $\pi/2$-DBPSK/GMSK with data rates 50Mbps-1.5Gbps
  - Class II (MDR): Medium-Data-Rate, Quasi-constant envelope (QPSK) with data rates up to 3Gbps
  - Class III (HDR): High-Data-Rate, non-constant envelope (8PSK & 16QAM) with data rates up to 6Gbps
- Medium size FFT(256) & iFFT(256) for FDE is enough for all practical environments (optional 512 mode)
- Known Golay code of variable length will serve as CP. This puts the CP at works instead of being a Waste.
- The Golay prefix will be used for timing, frequency and channel tracking if desired.
- Pilot CES are used to re-acquire the channel

Frame Format: OFDM

- The modulation of choice for HDR (16-QAM and above),
- Data rates up to 6Gbps
- Allows future data rates extension without RF HW change
- FFT size of 512 allows operation in extremely harsh environments with very large delay spread
- Periodic pilot CES would alleviate the channel tracking task and reduces the sync engine tremendously
- SC with 16-QAM presents no advantages over OFDM
- *We need both SC & OFDM for different applications!*

Frame Format: Common Mode

- Common mode: necessary for interoperability between different devices & different networks
- It requires no additional circuitry to that used during preamble detection; it comes for free!
- Very low complexity with a single multiply and add (in serial implementation)
- Requires only Reed Solomon Code, already needed for the header!
- Used for beaconing, signaling and for BR (Base Rate) data packets
- The key enabler of collision avoidance between different networks

Unified PLCP Header

Aggregation Header

Default Header

RATE (5 bits)	Number of Sub-Frames (5 bits)	(sub) Frame LENGTH (16 bits)	(sub) Frame Number (5 bits)	FFT mode (1 bit)	CP mode (2 bits)	PCESL mode (2 bits)	PCESP mode (2 bits)	Reserved (5 bits)	sub-Frame 1 RATE (5 bits)	sub-Frame 2 RATE (5 bits)	• • •	sub-Frame N FEC mode (5 bits)
R0...R4 0:4	S0:S4 5:9	L0...L15 10:25	F0:F31 26:30	D0 31	C0:C1 32:33	U0:U1 34:35	P0:P1 36:37	R0:R1 38:39	40:44	45:49		35+5N:39+5N

RATE	SC (Mbps)	OFDM (Mbps)
00000	50Mbps CM	
00001	108	720
00010	216	1440
00011	432	2160
00100	864	2520
00101	1296	2880
00110	1512	4320
00111	1728	5040
01000	2592	930
01001	3024	1860
01010	3213	2232
01011	3888	3720
01100	4536	4463
01101	4820	RES
01110	5184	RES
01111	6048	RES
10000	6426	RES
10001:11111	3213	RES

CP Mode	Cyclic Prefix Length	
	SC-256	OFDM/ Sc-512
00	00	32
01	16	64
10	32	96
11	64	128

PCESL Mode	PCES Length	
	SC-256	OFDM/ SC-512
00	16	64
01	64	128
10	128	256
11	256	RES

PCESP Mode	PCES Period	
	SC-256	OFDM/ SC-512
00	2048	2048
01	4096	4096

FFT Mode	SC-FFT
0	256
1	512

- If the number of sub-Frames = 1 than it is a default header, otherwise it is an aggregation header
- Header is nominally transmitted at the default base rate of 50Mbps
- Optional Higher Header Rate for MDR & HDR

SFD	Header Rate	SC Rate	Header Rate	OFDM Rate
-1+1	50 Mbps	50-1296Mbps	50 Mbps	720-1440Mbps
-1-1	432 Mbps	1512-6426Mbps	720 or 930 Mbps	2160-5040 Mbps

Single Carrier Mode

- Key Features
- Rate Related Parameters
- Timing & Frame Related Parameters
- Short Spreading Codes
- Structured LDPC FEC

SC Rate Dependent Parameters

SC: PSDU Default Rate-Dependent Parameters

Device Class	Data Rate Mbps R	Chip Rate MHz R_C	Modulation Scheme	Time Spreading Length: L	FEC Rate R_{FEC}	FEC Type	Coded Bits Per Burst N_{CBPS}	Info Bits Per Burst N_{IBPS}
I	**108**	1728	π/2-BPSK	8	0.500	LDPC	256	128
I	**216**	1728	π/2-BPSK	4	0.500	LDPC	256	128
I	**432**	1728	π/2-BPSK	2	0.500	LDPC	256	128
I	**864**	1728	π/2-BPSK	1	0.500	LDPC	256	128
I	**1296**	1728	π/2-BPSK	1	0.750	LDPC	256	192
I	**1512**	1728	π/2-BPSK	1	0.875	LDPC	256	224
II	**1728**	1728	π/2-QPSK	1	0.500	LDPC	256	128
II	**2592**	1728	π/2-QPSK	1	0.750	LDPC	256	192
II	**3024**	1728	π/2-QPSK	1	0.875	LDPC	256	224
II	**3213**	1728	π/2-QPSK	1	0.933	LDPC	256	238
III	**3888**	1728	π/2-8PSK	1	0.750	LDPC	256	192
III	**4536**	1728	π/2-8PSK	1	0.875	LDPC	256	224
III	**4819.5**	1728	π/2-8PSK	1	0.933	LDPC	256	238
III	**5184**	1728	π/2-16QAM	1	0.750	LDPC	256	192
III	**6048**	1728	π/2-16QAM	1	0.875	LDPC	256	224
III	**6426**	1728	π/2-16QAM	1	0.933	LDPC	256	238

SC Timing & Frame Parameters

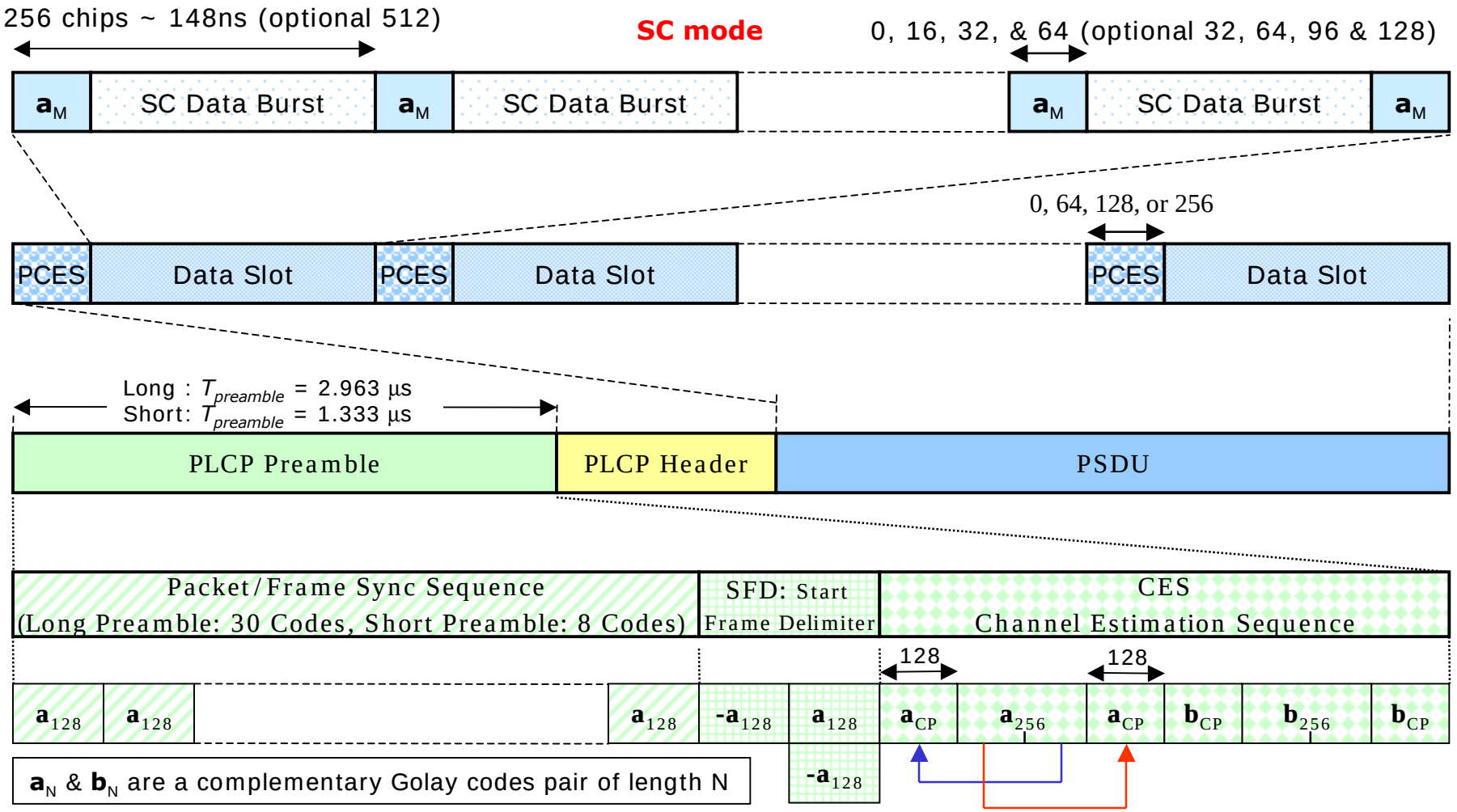
SC: Timing-Related Parameters

Parameter	Description	value				Unit	Formula
R_C	*Chip rate*	1728				MHz	
T_C	*Chip duration*	0.579				ns	$= 1/R_C$
N_{burst}	*Burst Size*	256				chips	
N_D	*Number of data chips*	256	240	224	192	chips	
N_{CP}	*Known Golay prefix length*	0	16	32	64	chips	
T_{burst}	*Burst duration (CP + Data)*	148.15				ns	$= 1/D_f$
T_D	*Data burst duration*	148.15	138.89	129.63	111.11		
T_{CP}	*Golay prefix duration*	0.00	9.26	18.52	37.04	ns	$= N_{CP} \times T_C$
F_{burst}	*Burst rate*	6.75				MHz	$= 1/T_{burst}$

SC Mode: Frame-Related Parameters

Parameter	Description	Value				Unit
N_{sync}	*Number of symbols in the packet sync seq.*	Default mode:	30	Fast mode:	8	**a**128
T_{sync}	*Duration of the packet sync seq.*	Default mode:	2.222	Fast mode:	0.593	µs
N_{sfd}	*Number of symbols in the frame sync seq.*	2				**a**128
T_{sfd}	*Duration of the frame sync sequence*	0.148				µs
N_{ces}	*Number of symbols in the channel estimation seq.*	4				**a**256/**b**256
T_{ces}	*Duration of the channel estimation seq.*	0.593				µs
N_{pre}	*Number of symbols in the PLCP preamble*	Default mode:	40	Fast mode:	18	128 chips symbols
T_{pre}	*Duration of the PLCP preamble*	Default mode:	2.963	Fast mode:	1.333	µs
N_{phdr}	*Number of symbols in the PHY header*	40				**a**64/**b**64 or **s**4
T_{phdr}	*Duration of the PHY header*	Default mode:	0.741	Fast mode:	0.093	µs
N_{mhdr}	*Number of symbols in the MAC header*	80				**a**64/**b**64 **or s4**
T_{mhdr}	*Duration of the MAC header*	Default mode:	1.481	Fast mode:	0.185	µs
N_{chdr}	*Number of symbols in the header HCS & RSP*	80				**a**64/**b**64 **or s4**
T_{chdr}	*Duration of the header HCS & RSP*	Default mode:	1.481	Fast mode:	0.185	µs
N_{hdr}	*Number of symbols in the frame header*	200				**a**64/**b**64 **or s4**
T_{hdr}	*Duration of frame header*	Default mode:	3.704	Fast mode:	0.463	µs
N_{frame}	*Number of symbols in the data field*	$4 \times \text{ceil}[(8 \times \text{LENGTH} + 32)/(4 \times N_{IBPS})]$				
T_{frame}	*Duration of the data field*	$N_{frame} \times T_{burst}$				
N_{cframe}	Number of chips in the frame	$= N_{frame} \times N_{FFT}$				
T_{packet}	*packet duration*	$= T_{frame} + T_{pre} + T_{hdr}$				
$N_{cpacket}$	*Number of chips in the packet*	Default (N_{cframe} + 11520)		Fast (N_{cframe} + 3104)		

SC Frame Format



SC PLCP Header

Aggregation Header

Default Header

RATE (5 bits)	Number of Sub-Frames (5 bits)	(sub) Frame LENGTH (16 bits)	(sub) Frame Number (5 bits)	FFT mode (1 bit)	CP mode (2 bits)	PCESL mode (2 bits)	PCESP mode (2 bits)	Reserved (5 bits)	sub-Frame 1 RATE (5 bits)	sub-Frame 2 RATE (5 bits)	• • •	sub-Frame N FEC mode (5 bits)
R0...R4 0:4	S0:S4 5:9	L0...L15 10:25	F0:F31 26:30	D0 31	C0:C1 32:33	U0:U1 34:35	P0:P1 36:37	R0:R1 38:39	40:44	45:49		35+5N:39+5N

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01101	4820	RES
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01	16	64
10	32	96
11	64	128

PCESL Mode	PCES Length	
	SC-256	OFDM/ SC-512
00	16	64
01	64	128
10	128	256
11	256	RES

PCESP Mode	PCES Period	
	SC-256	OFDM/ SC-512
00	2048	2048
01	4096	4096

FFT Mode	SC-FFT
0	256
1	512

- If the number of sub-Frames = 1 than it is a default header, otherwise it is an aggregation header
- Header is nominally transmitted at the default base rate of 50Mbps
- Optional Higher Header Rate for MDR & HDR

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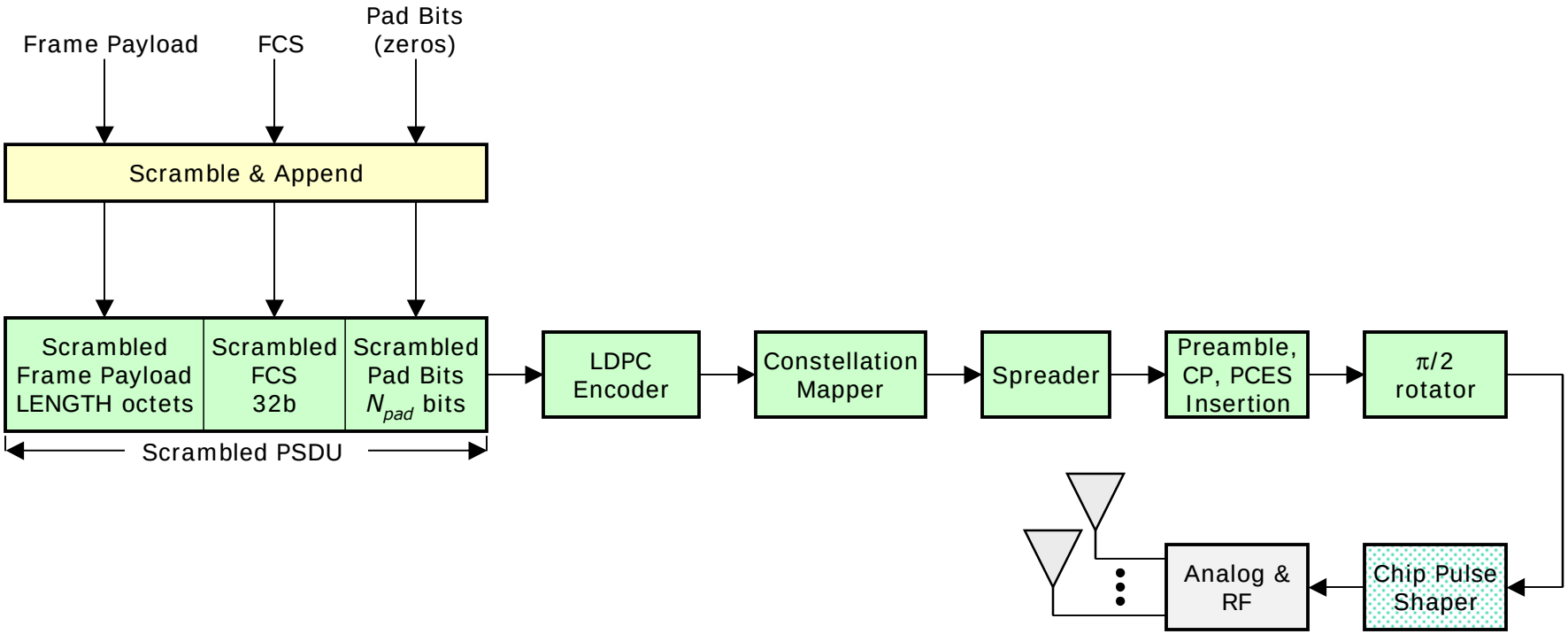
-1-1	432 Mbps	1512-6426Mbps	720 or 930 Mbps	2160-5040 Mbps

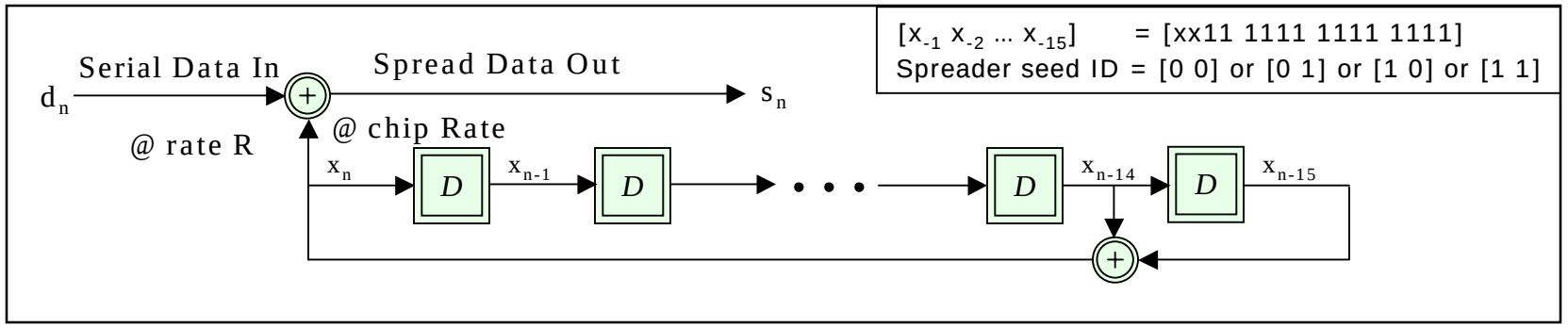
SC Transmitter Reference Diagram



$$N_{pad} = N_{IBPS} \times \lceil (8 \times LENGTH + 32) / N_{IBPS} \rceil - (8 \times LENGTH + 32)$$

LENGTH	: Number of octets in the frame payload
32	: FCS length in bits
N_{IBPS}	: Number of information bits per slot

Short Spreading Codes



- For low spreading code length (8 and below), there are no good codes.
- Use a varying spreading code generated by an LFSR
  - SC time spreading and
  - OFDM frequency spreading

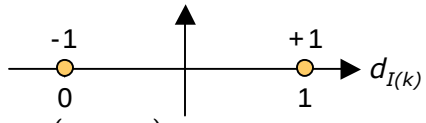
matlab code

```
function [dataOut] = tcSpreader(dataIn,spreaderSeedId,Fast)
shiftRegister  = [spreaderSeedId ones(1,13)];
for k = 0:length(dataIn) -1,
                feedback      = xor( shiftRegister(13+(1)) ,   shiftRegister(14+(1)) );
                dataOut(k+(1)) = mod(dataIn(k+(1))+feedback , 2);
                shiftRegister  = [feedback shiftRegister([0:13]+(1))];
end;
return;
```

The Constellation Mapper

BPSK encoding table

Input Bit b_k	I-out
0	-1
1	+1

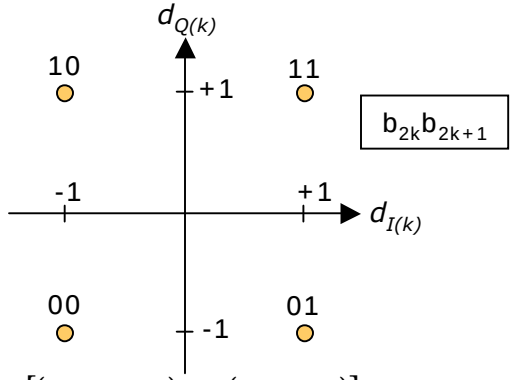


$$d_k = (2b_k - 1), \quad k = 0, 1, 2, \ldots$$

QPSK encoding table

Input Bit b_{2k}	I-out
0	-1
1	+1

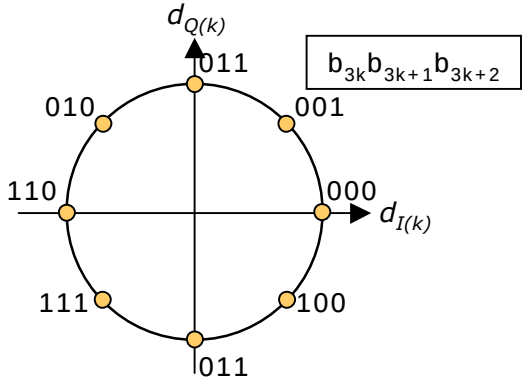
Input Bit b_{2k+1}	Q-out
0	-1
1	+1



$$d_k = \frac{1}{\sqrt{2}}\left[(2b_{2k+1} - 1) + j(2b_{2k} - 1)\right], \quad k = 0, 1, 2, \ldots$$

8PSK encoding table

Input Bit $b_{3k}\, b_{3k+1}\, b_{3k+2}$	IQ-out
000	exp(j0)
001	exp(jπ/4)
010	exp(j3π/4)
011	exp(jπ/2)
100	exp(j7π/4)
101	exp(j3π/2)
110	exp(jπ)
111	exp(j5π/4)



The LPDC Encoder

- No interleaving is required
- Supports rates ½, ¾, and 7/8
- Very low complexity systematic encoder
- Low complexity highly parallelizable decoder (gate count ~ 150Kgates)
- Throughput matched to that of RS
- 1 RS and 1 LDPC Decoder engine is needed for LDR devices
- Throughput of 1728 Mbps with Master clock of 216 MHz (BW/8) and 64 iterations

Rate	1/2	3/4	7/8
KK	288	432	504
NN	576	576	576
d_{min}	14	10	6

The LDPC: Rate ¾ & 7/8 Parity Check Matrices

- Parity check matrix **H** is specified by an exponent matrix **E**, i.e. $\mathbf{H} = \mathbf{J}^{\mathbf{E}}$
- Matrix **J** is the cyclic shift of the 18x18 Identity matrix, i.e.
- $J^{\infty} = 0$; $J^{0} = I$; $J^{18} = I$

$$J_{18\times 18} = \begin{bmatrix} 0 & 1 & 0 & \cdots & \cdots & 0 \\ 0 & 0 & 1 & \ddots & & \vdots \\ \vdots & \ddots & 0 & \ddots & \ddots & \vdots \\ \vdots & & & \ddots & \ddots & 0 \\ 0 & & & \ddots & 0 & 1 \\ 1 & 0 & \cdots & \cdots & 0 & 0 \end{bmatrix}$$

E78: Rate 7/8

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	2	11	9	10	4	15	2	5	12	16	16	10	5	13	2	8	10	5	10	6	5	17	10	8	6	7	16	0	2	∞	∞	∞
2	10	2	11	9	5	4	15	2	10	12	16	16	8	5	13	2	6	10	5	10	8	5	17	10	0	6	7	16	7	2	∞	∞
3	9	10	2	11	2	5	4	15	16	10	12	16	2	8	5	13	10	6	10	5	10	8	5	17	16	0	6	7	8	7	2	∞
4	11	9	10	2	15	2	5	4	16	16	10	12	13	2	8	5	5	10	6	10	17	10	8	5	7	16	0	6	5	8	7	2

E34: Rate 3/4

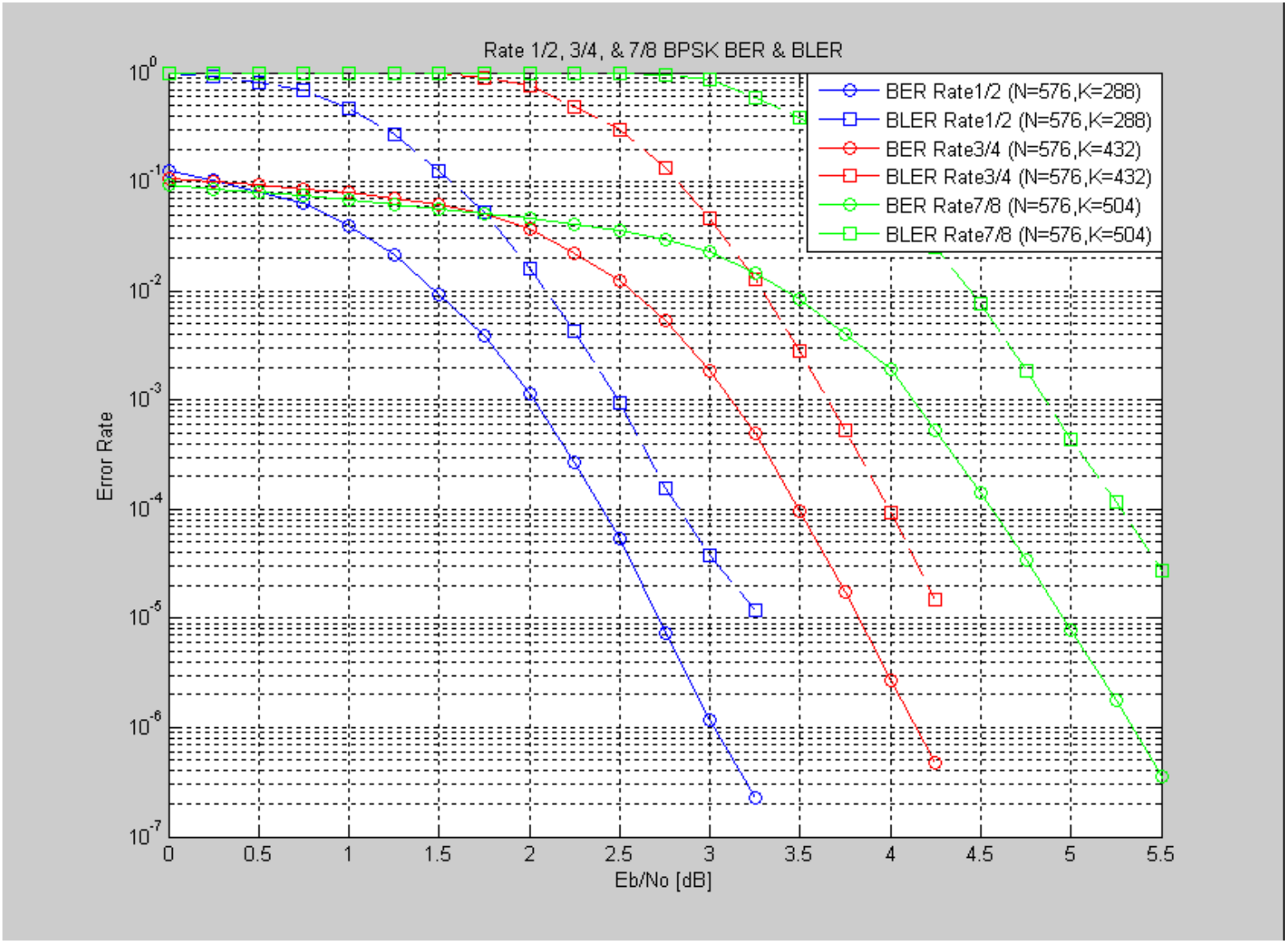
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	2	∞	9	∞	4	∞	∞	5	12	∞	16	∞	5	∞	2	∞	10	5	∞	∞	∞	∞	10	8	∞	7	∞	∞	∞	∞	∞	∞
2	∞	11	∞	10	∞	15	2	∞	∞	16	∞	10	∞	13	∞	8	∞	∞	10	6	5	17	∞	∞	6	∞	∞	∞	∞	∞	∞	∞
3	∞	2	∞	9	5	4	∞	∞	∞	12	∞	16	∞	5	∞	2	∞	10	5	∞	8	∞	∞	10	∞	∞	7	16	∞	2	∞	∞
4	10	∞	11	∞	∞	∞	15	2	10	∞	16	∞	8	∞	13	∞	6	∞	∞	10	∞	5	17	∞	0	6	∞	∞	7	∞	∞	∞
5	9	∞	2	∞	∞	5	4	∞	16	∞	12	∞	2	∞	5	∞	∞	∞	10	5	10	8	∞	∞	16	∞	∞	7	∞	∞	∞	∞
6	∞	10	∞	11	2	∞	∞	15	∞	10	∞	16	∞	8	∞	13	10	6	∞	∞	∞	∞	5	17	∞	0	6	∞	∞	∞	∞	∞
7	∞	9	∞	2	∞	∞	5	4	∞	16	∞	12	∞	2	∞	5	5	∞	∞	10	∞	10	8	∞	7	16	∞	∞	5	∞	∞	2
8	11	∞	10	∞	15	2	∞	∞	16	∞	10	∞	13	∞	8	∞	∞	10	6	∞	17	∞	∞	5	∞	∞	0	6	∞	8	7	∞

The LDPC: Rate ½ Parity Check Matrix

E12: Rate 1/2

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	2	∞	∞	∞	4	∞	∞	∞	∞	∞	2	∞	∞	5	∞	∞	∞	∞	10	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
2	∞	∞	9	∞	∞	∞	∞	5	5	∞	∞	¥	10	∞	∞	∞	∞	∞	∞	8	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
3	∞	11	∞	∞	∞	15	∞	∞	∞	∞	∞	8	∞	∞	∞	6	∞	17	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
4	∞	∞	∞	10	∞	∞	2	∞	∞	13	∞	¥	∞	∞	10	∞	5	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
5	∞	2	∞	∞	∞	4	∞	∞	∞	∞	∞	2	∞	∞	5	∞	∞	∞	∞	10	∞	∞	7	∞	∞	∞	5	∞	∞	∞	∞	∞
6	∞	∞	∞	9	5	∞	∞	∞	∞	5	∞	∞	∞	10	∞	∞	8	∞	∞	∞	∞	∞	∞	16	∞	2	∞	∞	∞	∞	∞	∞
7	∞	∞	11	∞	∞	∞	15	∞	8	∞	∞	∞	6	∞	∞	∞	∞	∞	17	∞	∞	6	∞	∞	7	∞	∞	∞	∞	∞	∞	∞
8	10	∞	∞	∞	∞	∞	∞	2	∞	∞	13	∞	∞	∞	∞	10	∞	5	∞	∞	0	∞	∞	∞	∞	∞	∞	8	∞	∞	∞	∞
9	∞	∞	2	∞	∞	∞	4	∞	2	∞	∞	∞	∞	∞	∞	5	10	∞	∞	∞	∞	∞	∞	7	∞	∞	∞	∞	∞	∞	∞	∞
10	9	∞	∞	∞	∞	5	∞	∞	∞	∞	5	∞	∞	∞	10	∞	∞	8	∞	∞	16	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
11	∞	∞	∞	11	∞	∞	∞	15	∞	8	∞	∞	∞	6	∞	∞	∞	∞	∞	17	∞	∞	6	∞	∞	∞	∞	∞	∞	∞	∞	∞
12	∞	10	∞	∞	2	∞	∞	∞	∞	∞	∞	13	10	∞	∞	∞	∞	∞	5	∞	∞	0	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
13	∞	∞	∞	2	∞	∞	∞	4	∞	2	∞	∞	5	∞	∞	∞	∞	10	∞	∞	7	∞	∞	∞	5	∞	∞	∞	∞	∞	∞	12
14	∞	9	∞	∞	∞	∞	5	∞	∞	∞	∞	5	∞	∞	∞	10	∞	∞	8	∞	∞	16	∞	∞	∞	∞	∞	2	∞	16	∞	∞
15	11	∞	∞	∞	15	∞	∞	∞	∞	∞	8	∞	∞	∞	6	∞	17	∞	∞	∞	∞	∞	∞	6	∞	∞	7	∞	∞	∞	10	∞
16	∞	∞	10	∞	∞	2	∞	∞	13	∞	∞	∞	∞	10	∞	∞	∞	∞	∞	5	∞	∞	0	∞	∞	8	∞	∞	16	∞	∞	∞

The LDPC: Performance



OFDM Mode

- Rate Dependent Parameters
- Timing Related Parameters
- Frame Related Parameters
- Transmitter Reference Diagram
- FEC Option I
- FEC Option II
- Constellation Mapper
- OFDM Modulator
- PSD

OFDM Rate Dependent Parameters

OFDM: PSDU Default Rate-Dependent Parameters

Data Rate Mbps R	Chip Rate MHz R_C	Modulation Scheme	Frequency Spreading Length: L	FEC Rate RFEC	FEC Type	Coded Bits Per Symbol NCBPS	Info Bits Per Symbol NIBPS
720	1728	QPSK	2	0.500	LDPC	480	240
1440	1728	QPSK	1	0.500	LDPC	480	240
2160	1728	QPSK	1	0.750	LDPC	480	360
2520	1728	QPSK	1	0.875	LDPC	480	420
2880	1728	16QAM	1	0.500	LDPC	480	240
4320	1728	16QAM	1	0.750	LDPC	480	360
5040	1728	16QAM	1	0.875	LDPC	480	420
930	1728	QPSK	1	0.333	Convolutional/RS	480	160
1860	1728	QPSK	1	0.667	Convolutional/RS	480	320
2232	1728	QPSK	1	0.800	Convolutional/RS	480	384
3720	1728	16QAM	1	0.667	Convolutional/RS	480	320
4463	1728	16QAM	1	0.800	Convolutional/RS	480	384

OFDM Timing Parameters

OFDM: Timing-Related Parameters

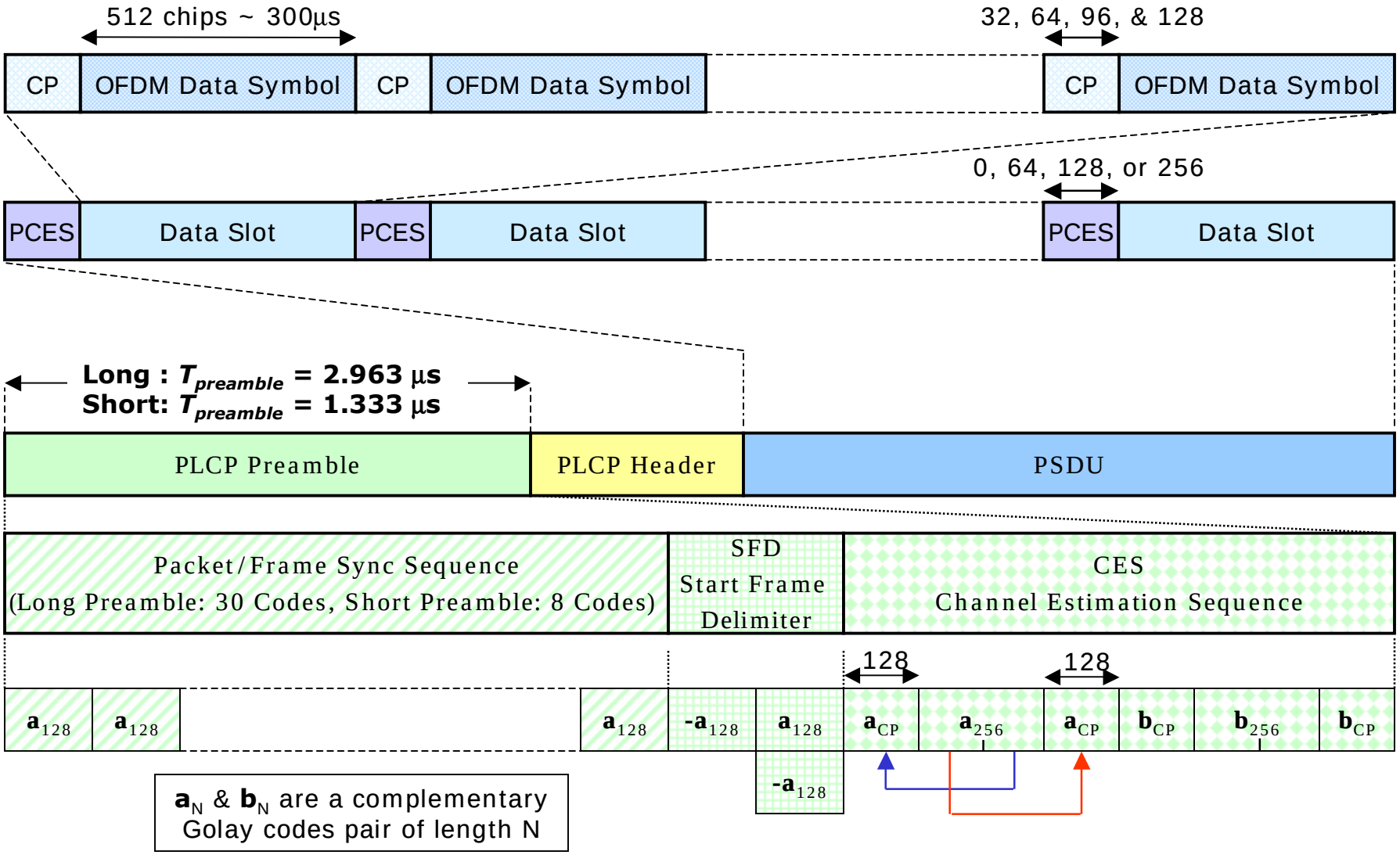
Parameter	Description	value				Unit	Formula
R_C	*Chip rate*	1728				MHz	
T_C	*Chip duration*	0.579				ns	$= 1/R_C$
N_{FFT}	*FFT Size*	512				subcarriers	
N_D	*Number of data subcarriers*	486				subcarriers	
N_{PF}	*Number of fixed pilot subcarriers*	8				subcarriers	
N_{PR}	*Number of running pilot subcarriers*	16				subcarriers	
N_P	*Total number of pilot subcarriers*	24				subcarriers	
N_G	*Number of guard subcarriers*	0				subcarriers	
N_{DC}	*Number of DC subcarriers*	1				subcarriers	
N_Z	*Number of zero (non DC) subcarriers*	1				subcarriers	
N_U	*Number of used subcarriers*	510					
N_{CP}	*Cyclic prefix length*	32	64	96	128	Chips	
D_f	*Subcarrier frequency spacing*	3.375				MHz	$= R_C/N_{FFT}$
B_U	*Used bandwidth*	1721.25				MHz	$= N_U \times D_f$
T_{FFT}	*IFFT/FFT duration*	296.30				ns	$= 1/D_f$
T_{CP}	*Cyclic prefix duration*	18.52	37.04	55.56	74.07	ns	$= N_{CP} \times T_C$
T_{SYM}	*Symbol duration*	314.81	333.33	351.85	370.37	ns	$= T_{FFT} + T_{CP}$
F_{SYM}	*Symbol rate*	3.176	3	2.842	2.7	MHz	$= 1/T_{SYM}$
N_{CPSYM}	*Number of chips per symbol*	544	576	608	640	Chips	$= N_{FFT} + N_{CP}$

OFDM Frame Related Parameters

OFDM Mode: Frame-Related Parameters

Parameter	Description	Value				Unit
N_{sync}	*Number of symbols in the packet sync seq.*	Default mode:	30	Fast mode:	8	**a**128
T_{sync}	*Duration of the packet sync seq.*	Default mode:	2.222	Fast mode:	0.593	µs
N_{sfd}	*Number of symbols in the frame sync seq.*	2				**a**128
T_{sfd}	*Duration of the frame sync sequence*	0.148				µs
N_{ces}	*Number of symbols in the channel estimation seq.*	4				**a**256/**b**256
T_{ces}	*Duration of the channel estimation seq.*	0.593				µs
N_{pre}	*Number of symbols in the PLCP preamble*	Default mode:	40	Fast mode:	18	128 chips symbols
T_{pre}	*Duration of the PLCP preamble*	Default mode:	2.963	Fast mode:	1.333	µs
N_{phdr}	*Number of symbols in the PHY header*	40				**a**64/**b**64 or **s**4
T_{phdr}	*Duration of the PHY header*	Default mode:	0.741	Fast mode:	0.093	µs
N_{mhdr}	*Number of symbols in the MAC header*	80				**a**64/**b**64 **or s4**
T_{mhdr}	*Duration of the MAC header*	Default mode:	1.481	Fast mode:	0.185	µs
N_{chdr}	*Number of symbols in the header HCS & RSP*	80				**a**64/**b**64 **or s4**
T_{chdr}	*Duration of the header HCS & RSP*	Default mode:	1.481	Fast mode:	0.185	µs
N_{hdr}	*Number of symbols in the frame header*	200				**a**64/**b**64 **or s4**
T_{hdr}	*Duration of frame header*	Default mode:	3.704	Fast mode:	0.463	µs
N_{frame}	*Number of symbols in the data field*	$4 \times ceil[(8 \times LENGTH + 32)/(4 \times NIBPS)]$				symbols
T_{frame}	*Duration of the data field*	$N_{frame} \times T_{SYM}$				µs
N_{cframe}	Number of chips in the frame	$N_{frame} \times (N_{CP} + N_{FFT})$				chips
T_{packet}	*packet duration*	$T_{frame} + T_{pre} + T_{hdr}$				µs
$N_{cpacket}$	*Number of chips in the packet*	Default: $(N_{cframe} + 11520)$		Fast: $(N_{cframe} + 3104)$		chips

OFDM Frame Format



OFDM PLCP Header

Aggregation Header

Default Header

RATE (5 bits)	Number of Sub-Frames (5 bits)	(sub) Frame LENGTH (16 bits)	(sub) Frame Number (5 bits)	FFT mode (1 bit)	CP mode (2 bits)	PCESL mode (2 bits)	PCESP mode (2 bits)	Reserved (5 bits)	sub-Frame 1 RATE (5 bits)	sub-Frame 2 RATE (5 bits)	. . .	sub-Frame N FEC mode (5 bits)
R0...R4 0:4	S0:S4 5:9	L0...L15 10:25	F0:F31 26:30	D0 31	C0:C1 32:33	U0:U1 34:35	P0:P1 36:37	R0:R1 38:39	40:44	45:49		35+5N:39+5N

RATE	SC (Mbps)	OFDM (Mbps)
00000	50Mbps CM	
00001	108	720
00010	216	1440
00011	432	2160
00100	864	2520
00101	1296	2880
00110	1512	4320
00111	1728	5040
01000	2592	930
01001	3024	1860
01010	3213	2232
01011	3888	3720
01100	4536	4463
01101	4820	RES
01110	5184	RES
01111	6048	RES
10000	6426	RES
10001:11111	3213	RES

CP Mode	Cyclic Prefix Length	
	SC-256	OFDM/ Sc-512
00	00	32
01	16	64
10	32	96
11	64	128

PCESL Mode	PCES Length	
	SC-256	OFDM/ SC-512
00	16	64
01	64	128
10	128	256
11	256	RES

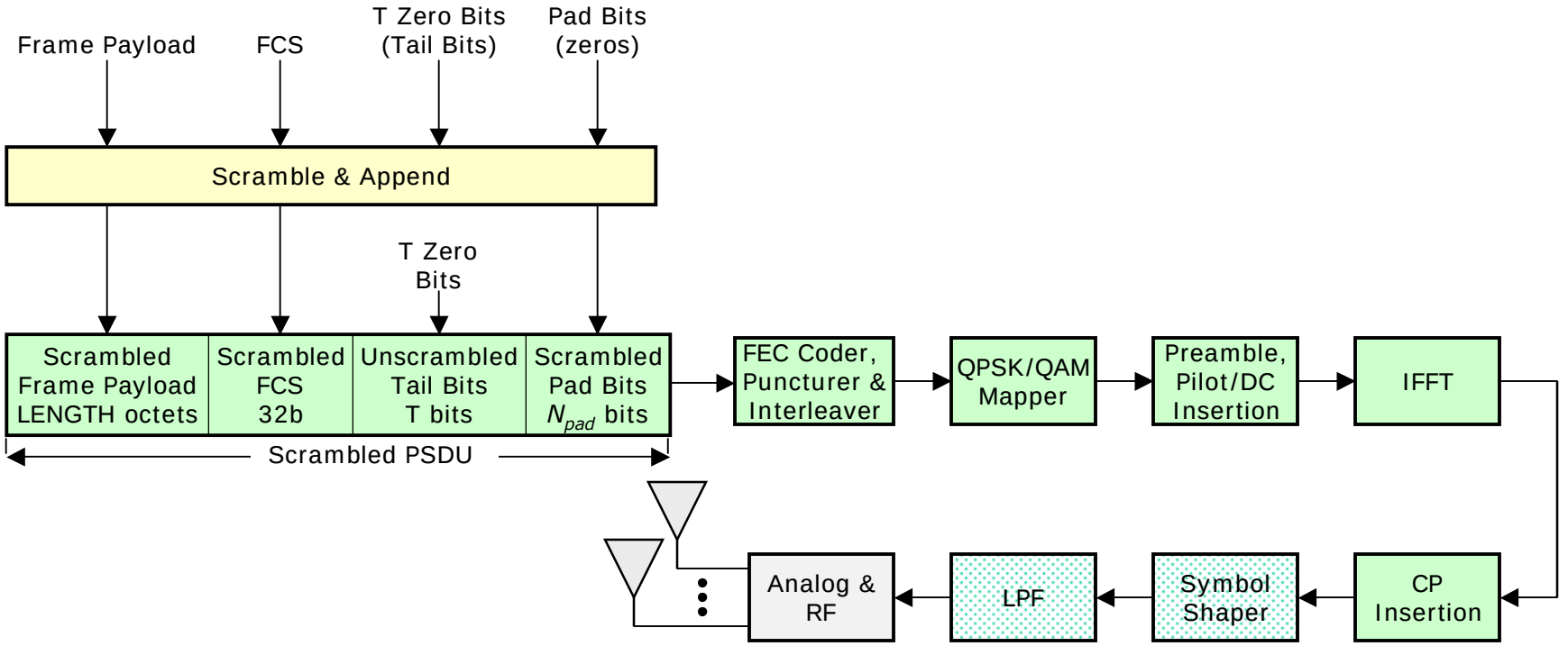
PCESP Mode	PCES Period	
	SC-256	OFDM/ SC-512
00	2048	2048
01	4096	4096

FFT Mode	SC-FFT
0	256
1	512

- If the number of sub-Frames = 1 than it is a default header, otherwise it is an aggregation header
- Header is nominally transmitted at the default base rate of 50Mbps
- Optional Higher Header Rate for MDR & HDR

SFD	Header Rate	SC Rate	Header Rate	OFDM Rate
-1+1	50 Mbps	50-1296Mbps	50 Mbps	720-1440Mbps
-1-1	432 Mbps	1512-6426Mbps	720 or 930 Mbps	2160-5040 Mbps

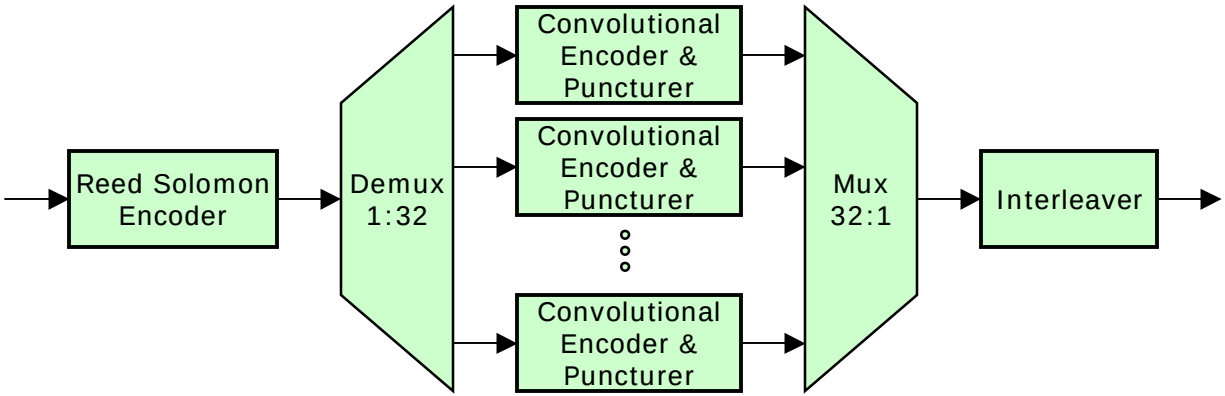
Transmitter Reference Diagram



$$N_{pad} = N_{IBP4S} \times \lceil (8 \times LENGTH + 32 + T) / N_{IBP4S} \rceil - (8 \times LENGTH + 32 + T)$$

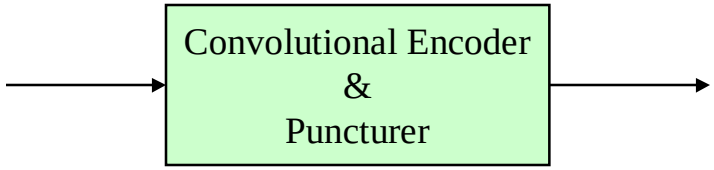
LENGTH	: Number of octets in the frame payload
32	: FCS length in bits
T	: Number of tail bits (0 for LDPC & 192 for convolutional)
N_{IBP4S}	: Number of information bits per four OFDM symbols

FEC Option I: Structure

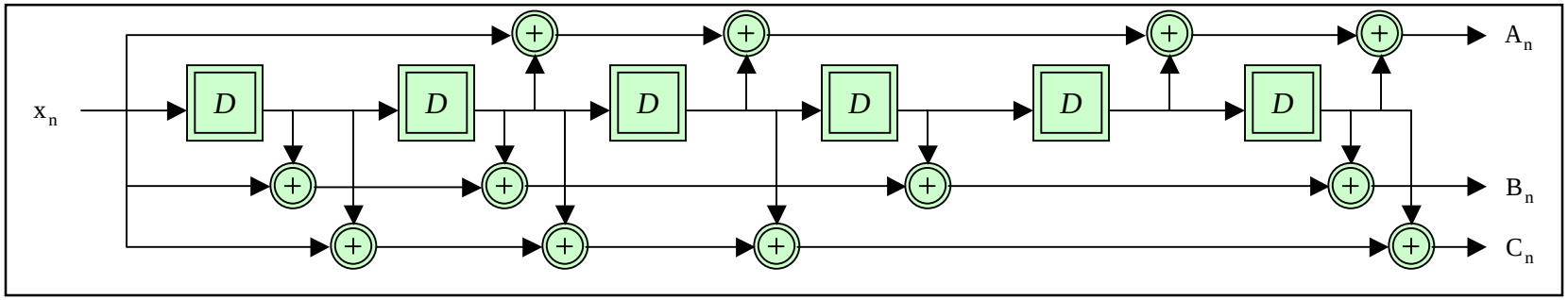


- Outer Reed Solomon RS(255,247) of rate 0.968:
  - For a master clock of 216MHz, one RS encoder has a throughput of 1728 Mbps
  - Up to implementer how to achieve higher throughput necessary with 16QAM (Master clock / buffering & multiple instantiation of RS encoder)
- Thirty two parallel convolutional encoders:
  - To achieve 16QAM throughput with a master clock of 216MHz
  - To enable future extension to 64QAM with a master clock of 432MHz

FEC Option I: The Convolutional Encoder



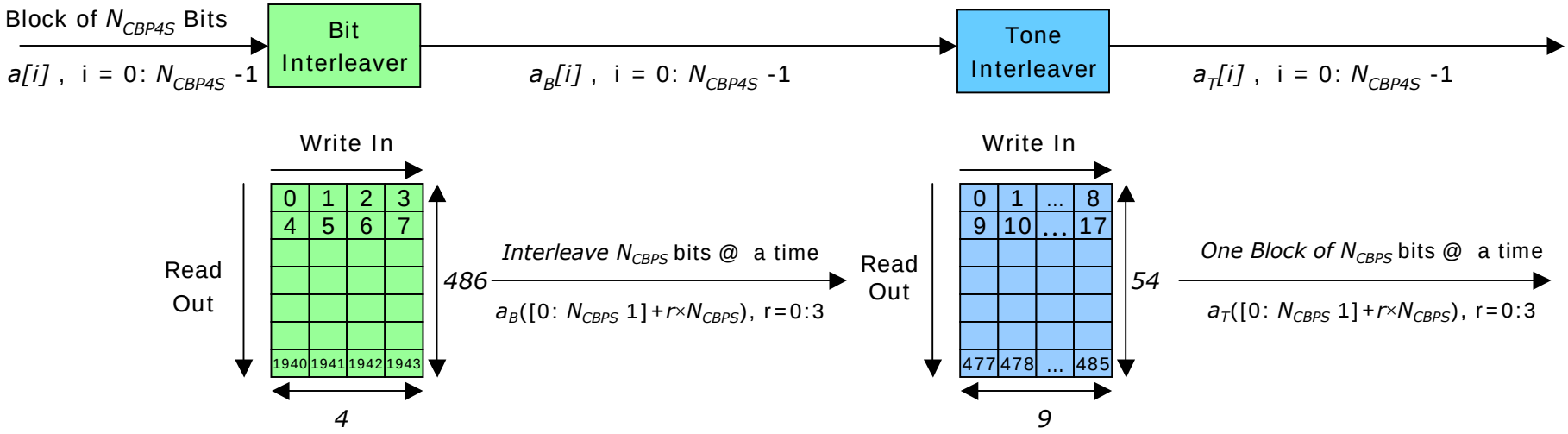
Convolutional encoder: R = 1/3, K = 7



Rate	Source Data	Encoded date	Bit Stolen Data	Period	#Stolen Bits
1/2	x_0	A_0 B_0 C_0	A_0 C_0	3	1
2/3	x_0 x_1	A_0 B_0 C_0 A_1 B_1 C_1 A_2 B_2 C_2 A_3 B_3 C_3	A_0 A_1 B_1 A_2 C_2 B_3	9	6
3/4	x_0 x_1 x_2	A_0 B_0 C_0 A_1 B_1 C_1 A_2 B_2 C_2	A_0 B_0 C_1 C_2	9	5
4/7	x_0 x_1 x_2 x_3	A_0 B_0 C_0 A_1 B_1 C_1 A_2 B_2 C_2 A_3 B_3 C_3	A_0 A_1 B_1 A_2 C_2 A_3 C_3	12	7
4/5	x_0 x_1 x_2 x_3	A_0 B_0 C_0 A_1 B_1 C_1 A_2 B_2 C_2 A_3 B_3 C_3	A_0 B_1 A_2 C_2 A_3	12	7

FEC Option I: The Interleaver

Coded Bits/ OFDM Symbol (N_{CBPS})	Coded Bits/ 4 OFDM Symbols (N_{CBP4S})	*Bit Interleaver*			Tone Interleaver		
		Block Size	N_{ROW}	N_{COL}	*Block Size*	N_{ROW}	N_{COL}
486	1944	1944	486	4	486	54	9



- Symbol Interleaver: permutes bits across 4 consecutive OFDM symbols ⇔ frequency & time diversity
- Intra-symbol tone interleaver: permutes the bits within an OFDM symbol across the data subcarriers ⇔ frequency diversity and robustness against narrow-band interferers

FEC Option II: LPDC

- No interleaving is required
- Supports rates ½, ¾, and 7/8
- Very low complexity systematic encoder
- Low complexity highly parallelizable decoder (gate count ~ 150Kgates)
- Throughput matched to that of RS
- 1 RS and 1 LDPC Decoder engine is needed for LDR devices
- Throughput of 1728 Mbps with Master clock of 216 MHz (BW/8) and 64 iterations

Rate	1/2	3/4	7/8
KK	288	432	504
NN	576	576	576
d_{min}	14	10	6

FEC Option II: Rate ¾ & 7/8 Parity Check Matrices

- Parity check matrix **H** is specified by an exponent matrix **E**, i.e. $\mathbf{H} = \mathbf{J}^{\mathbf{E}}$
- Matrix **J** is the cyclic shift of the 18x18 Identity matrix, i.e.
- $J^{\infty} = 0$; $J^{0} = I$; $J^{18} = I$

$$J_{18\times 18} = \begin{bmatrix} 0 & 1 & 0 & \cdots & \cdots & 0 \\ 0 & 0 & 1 & \ddots & & \vdots \\ \vdots & \ddots & 0 & \ddots & \ddots & \vdots \\ \vdots & & & \ddots & \ddots & 0 \\ 0 & & & \ddots & 0 & 1 \\ 1 & 0 & \cdots & \cdots & 0 & 0 \end{bmatrix}$$

E78: Rate 7/8

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	2	11	9	10	4	15	2	5	12	16	16	10	5	13	2	8	10	5	10	6	5	17	10	8	6	7	16	0	2	∞	∞	∞
2	10	2	11	9	5	4	15	2	10	12	16	16	8	5	13	2	6	10	5	10	8	5	17	10	0	6	7	16	7	2	∞	∞
3	9	10	2	11	2	5	4	15	16	10	12	16	2	8	5	13	10	6	10	5	10	8	5	17	16	0	6	7	8	7	2	∞
4	11	9	10	2	15	2	5	4	16	16	10	12	13	2	8	5	5	10	6	10	17	10	8	5	7	16	0	6	5	8	7	2

E34: Rate 3/4

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	2	∞	9	∞	4	∞	∞	5	12	∞	16	∞	5	∞	2	∞	10	5	∞	∞	∞	∞	10	8	∞	7	∞	∞	∞	∞	∞	∞
2	∞	11	∞	10	∞	15	2	∞	∞	16	∞	10	∞	13	∞	8	∞	∞	10	6	5	17	∞	∞	6	∞	∞	∞	∞	∞	∞	∞
3	∞	2	∞	9	5	4	∞	∞	∞	12	∞	16	∞	5	∞	2	∞	10	5	∞	8	∞	∞	10	∞	∞	7	16	∞	2	∞	∞
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5	9	∞	2	∞	∞	5	4	∞	16	∞	12	∞	2	∞	5	∞	∞	∞	10	5	10	8	∞	∞	16	∞	∞	7	∞	∞	∞	∞
6	∞	10	∞	11	2	∞	∞	15	∞	10	∞	16	∞	8	∞	13	10	6	∞	∞	∞	∞	5	17	∞	0	6	∞	∞	∞	∞	∞
7	∞	9	∞	2	∞	∞	5	4	∞	16	∞	12	∞	2	∞	5	5	∞	∞	10	∞	10	8	∞	7	16	∞	∞	5	∞	∞	2
8	11	∞	10	∞	15	2	∞	∞	16	∞	10	∞	13	∞	8	∞	∞	10	6	∞	17	∞	∞	5	∞	∞	0	6	∞	8	7	∞

FEC Option II: Rate ½ Parity Check Matrix

E12: Rate 1/2

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	2	∞	∞	∞	4	∞	∞	∞	∞	∞	2	∞	∞	5	∞	∞	∞	∞	10	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
2	∞	∞	9	∞	∞	∞	∞	5	5	∞	∞	¥	10	∞	∞	∞	∞	∞	∞	8	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
3	∞	11	∞	∞	∞	15	∞	∞	∞	∞	∞	8	∞	∞	∞	6	∞	17	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
4	∞	∞	∞	10	∞	∞	2	∞	∞	13	∞	¥	∞	∞	10	∞	5	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
5	∞	2	∞	∞	∞	4	∞	∞	∞	∞	∞	2	∞	∞	5	∞	∞	∞	∞	10	∞	∞	7	∞	∞	∞	5	∞	∞	∞	∞	∞
6	∞	∞	∞	9	5	∞	∞	∞	∞	5	∞	∞	∞	10	∞	∞	8	∞	∞	∞	∞	∞	∞	16	∞	2	∞	∞	∞	∞	∞	∞
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8	10	∞	∞	∞	∞	∞	∞	2	∞	∞	13	∞	∞	∞	∞	10	∞	5	∞	∞	0	∞	∞	∞	∞	∞	∞	8	∞	∞	∞	∞
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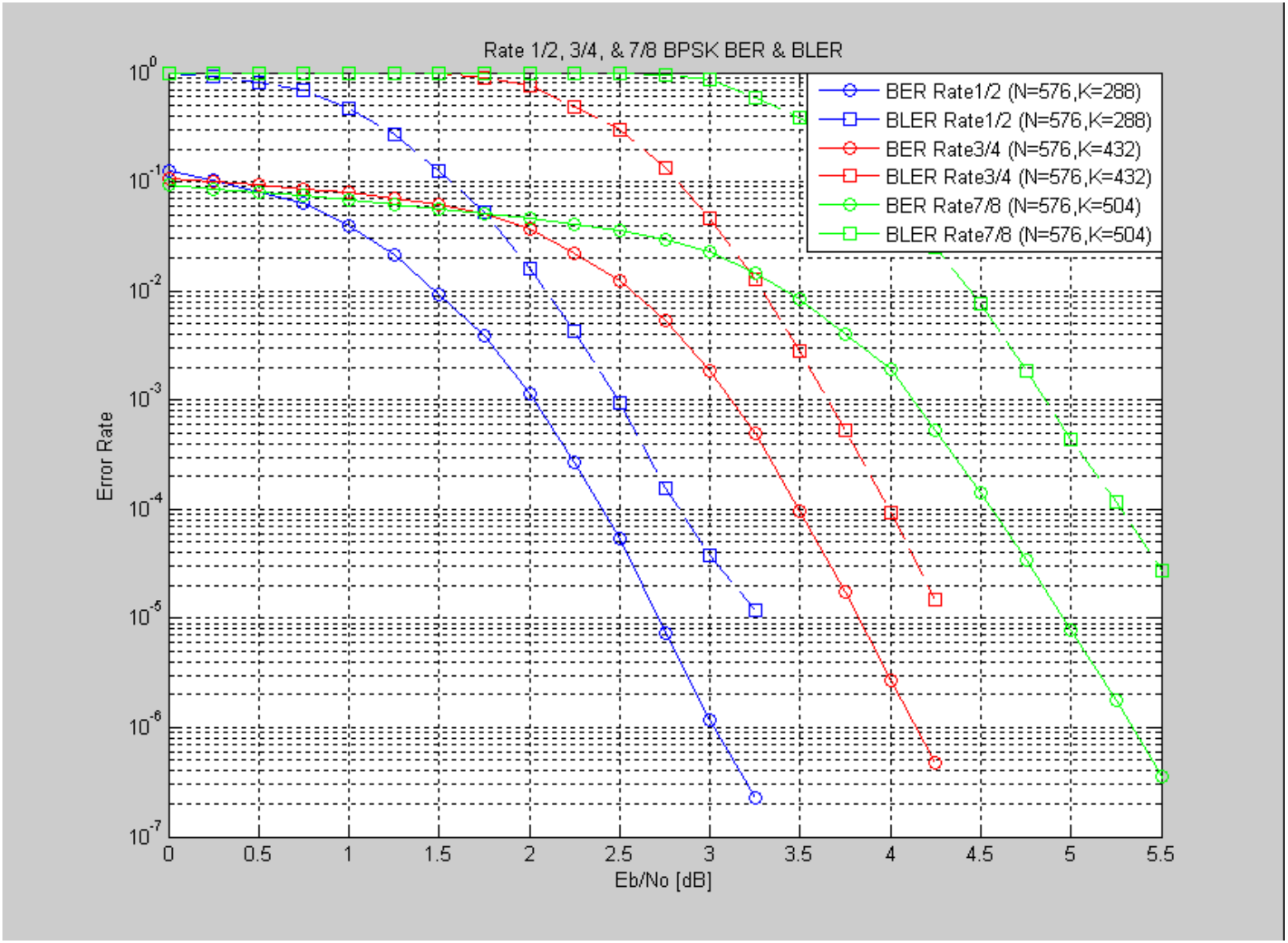
13	∞	∞	∞	2	∞	∞	∞	4	∞	2	∞	∞	5	∞	∞	∞	∞	10	∞	∞	7	∞	∞	∞	5	∞	∞	∞	∞	∞	∞	12
14	∞	9	∞	∞	∞	∞	5	∞	∞	∞	∞	5	∞	∞	∞	10	∞	∞	8	∞	∞	16	∞	∞	∞	∞	∞	2	∞	16	∞	∞
15	11	∞	∞	∞	15	∞	∞	∞	∞	∞	8	∞	∞	∞	6	∞	17	∞	∞	∞	∞	∞	∞	6	∞	∞	7	∞	∞	∞	10	∞
16	∞	∞	10	∞	∞	2	∞	∞	13	∞	∞	∞	∞	10	∞	∞	∞	∞	∞	5	∞	∞	0	∞	∞	8	∞	∞	16	∞	∞	∞

FEC Option II: Performance

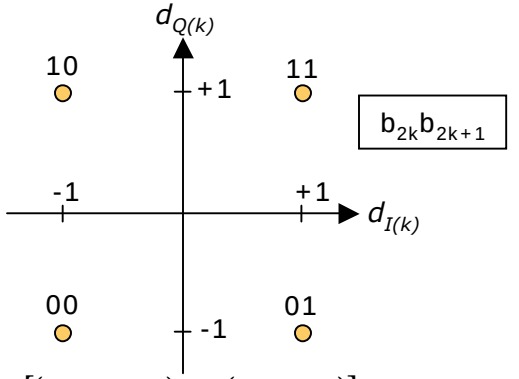


The Constellation Mapper

QPSK encoding table

Input Bit b_{2k}	I-out
0	-1
1	+1

Input Bit b_{2k+1}	Q-out
0	-1
1	+1

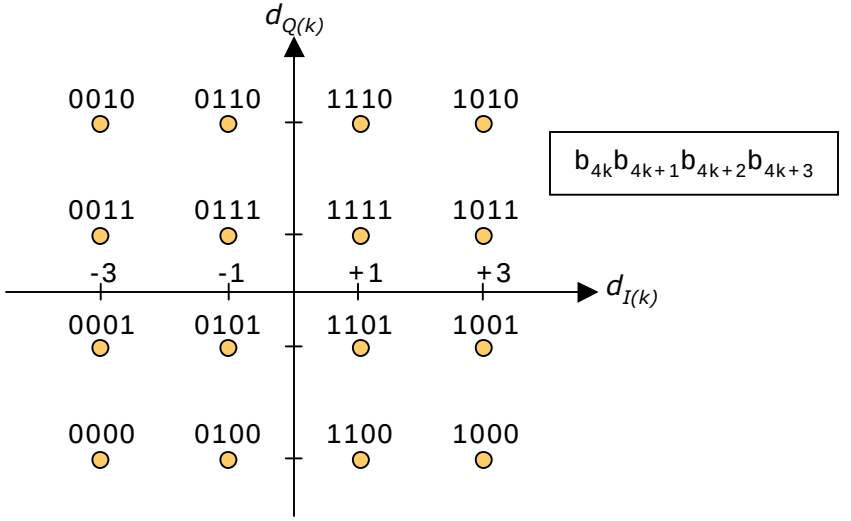


$$d_k = \frac{1}{\sqrt{2}}\left[(2b_{2k+1}-1)+j(2b_{2k}-1)\right], \quad k=0,1,2,\ldots$$

16-QAM mapping

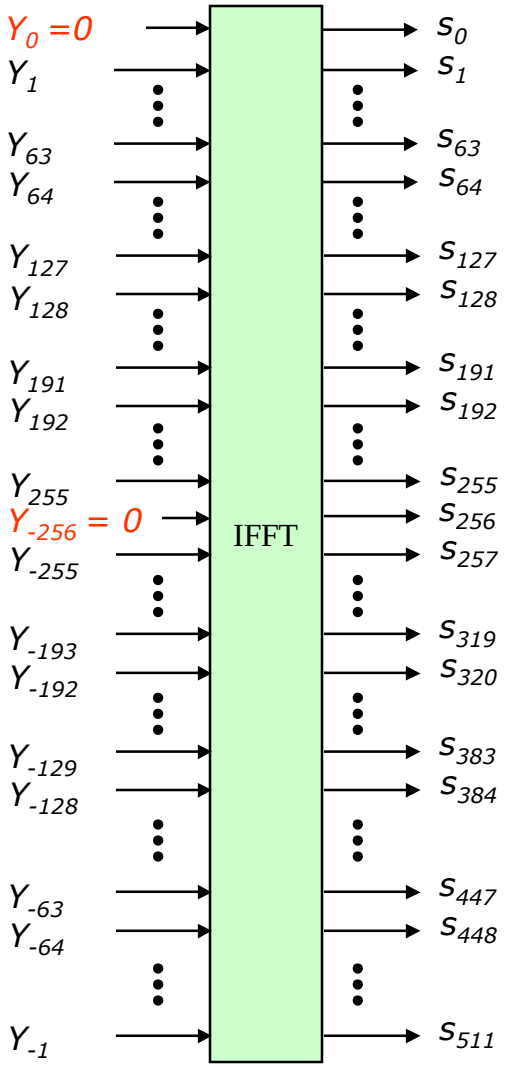
Input Bit $b_{4k}\,b_{4k+1}$	I-out
00	-3
01	-1
11	+1
10	+3

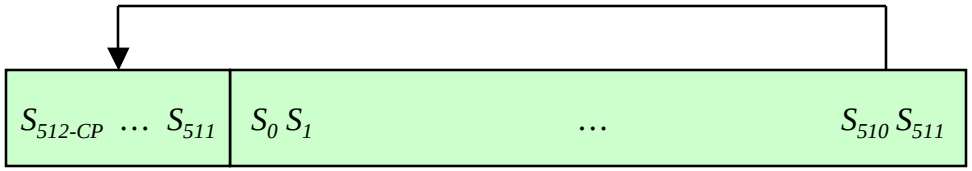
Input Bit $b_{4k}\,b_{4k+1}$	I-out
00	-3
01	-1
11	+1
10	+3



$$d_k = \frac{1}{\sqrt{10}}\left[(2b_{4k}-1)(3-2b_{4k+1})+j(2b_{4k+2}-1)(3-2b_{4k+3})\right], \quad k=0,1,2,\ldots$$

The OFDM Modulator





- CP Default value is 64, Optional: 32, 96, & 128

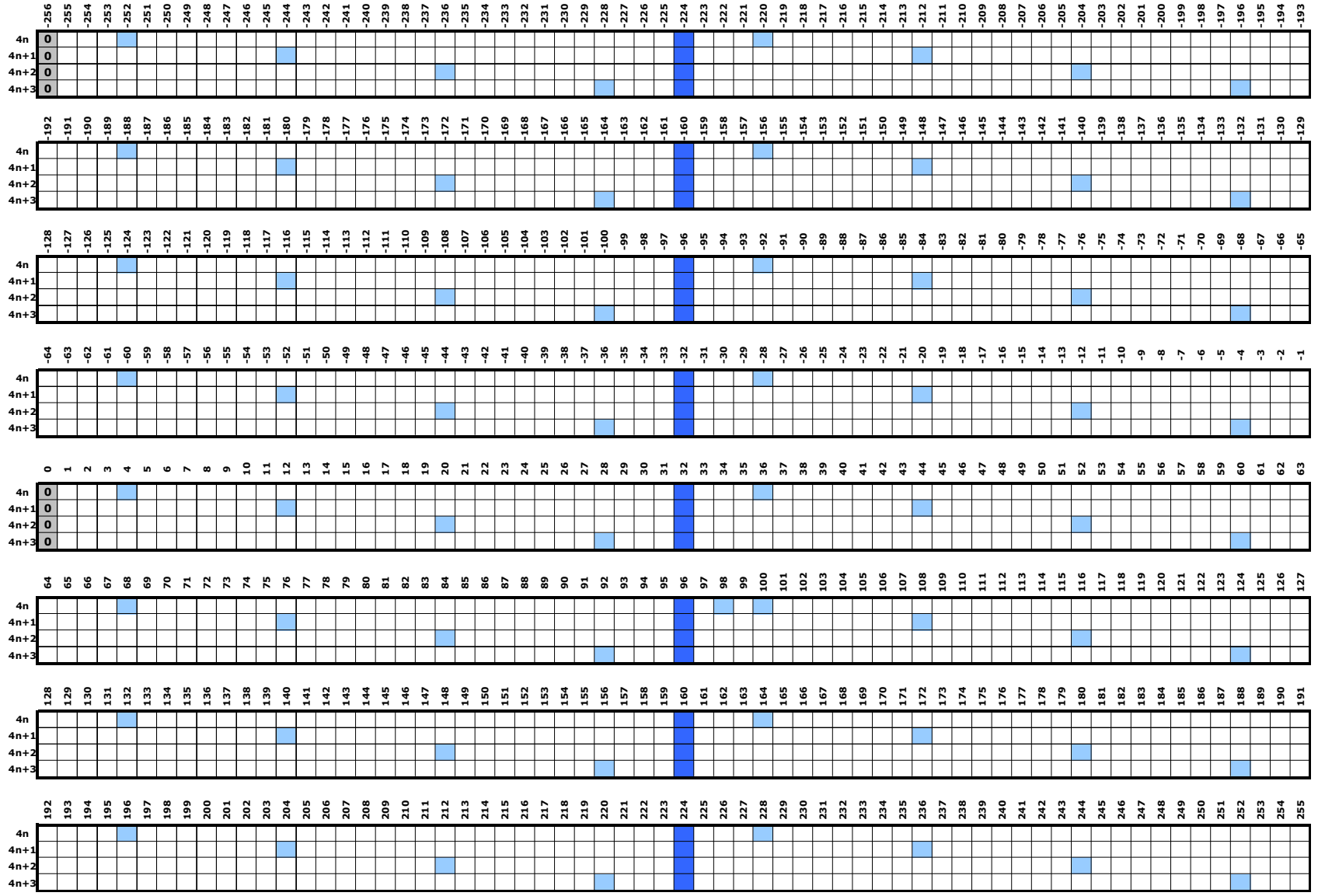
$$s_k^{(n)} = \frac{1}{\sqrt{N_{FFT}}} \sum_{m=-N_u/2}^{N_u/2} Y_m^{(n)} e^{j\frac{2\pi mk}{N_{FFT}}} \qquad k = 0:511$$

Pilots for CP ≥ 96		
Symbol #	**Fixed Pilots (8)**	**Variable Pilots (16)**
8n	-224:60:224	-254:32:226
8n+1	-224:60:224	-250:32:230
8n+2	-224:60:224	-246:32:234
8n+3	-224:60:224	-242:32:238
8n+4	-224:60:224	-238:32:242
8n+5	-224:60:224	-234:32:246
8n+6	-224:60:224	-230:32:250
8n+7	-224:60:224	-226:32:254

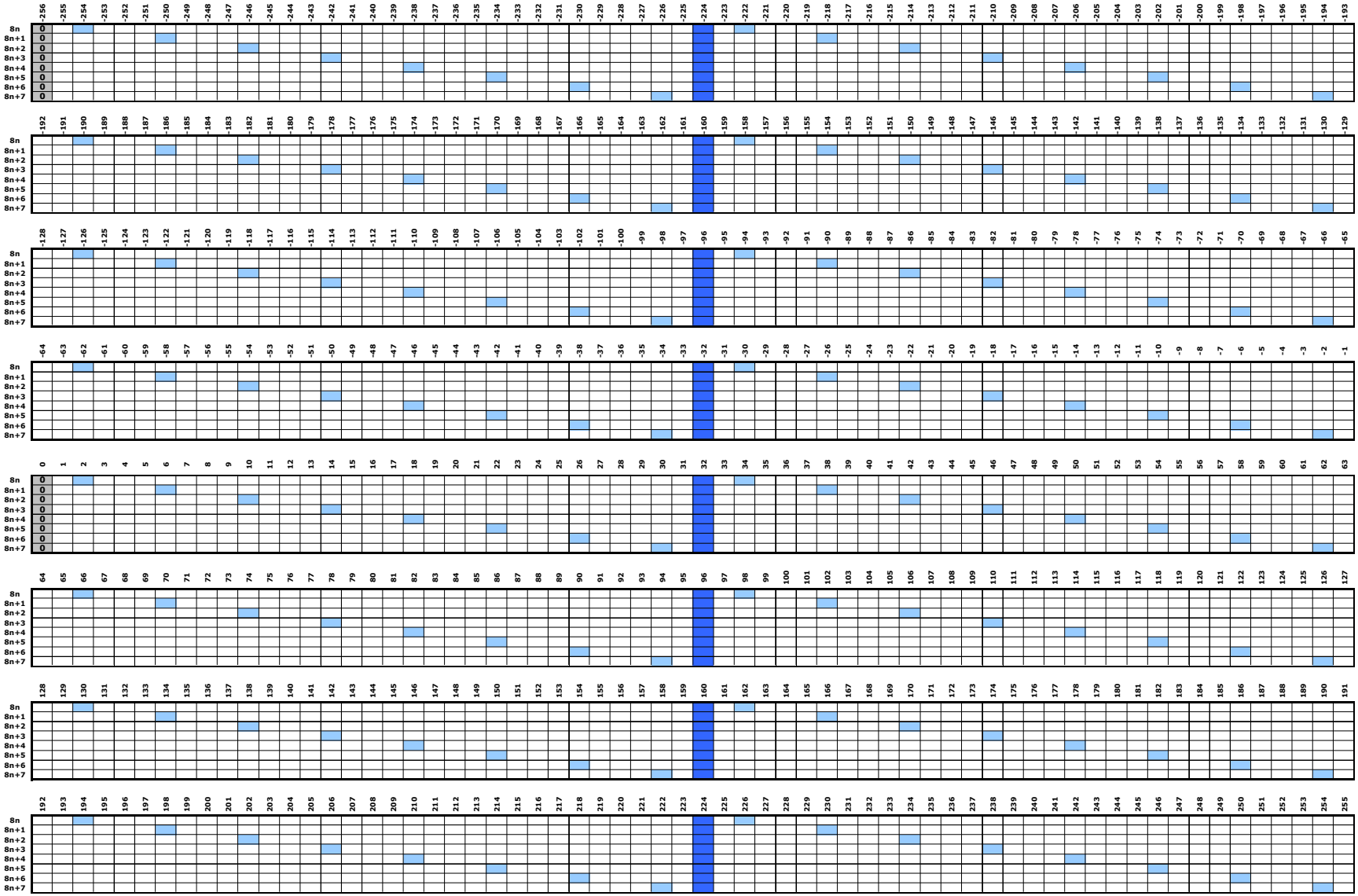
Pilots for CP ≤ 64		
Symbol #	**Fixed Pilots (8)**	**Variable Pilots (16)**
4n	-224:60:224	-252:32:228
4n+1	-224:60:224	-244:32:236
4n+2	-224:60:224	-236:32:244
4n+3	-224:60:224	-228:32:252

Zero & DC Subcarriers	2
Guard Subcarriers	0
Pilot Subcarriers	24
Data Subcarriers	486

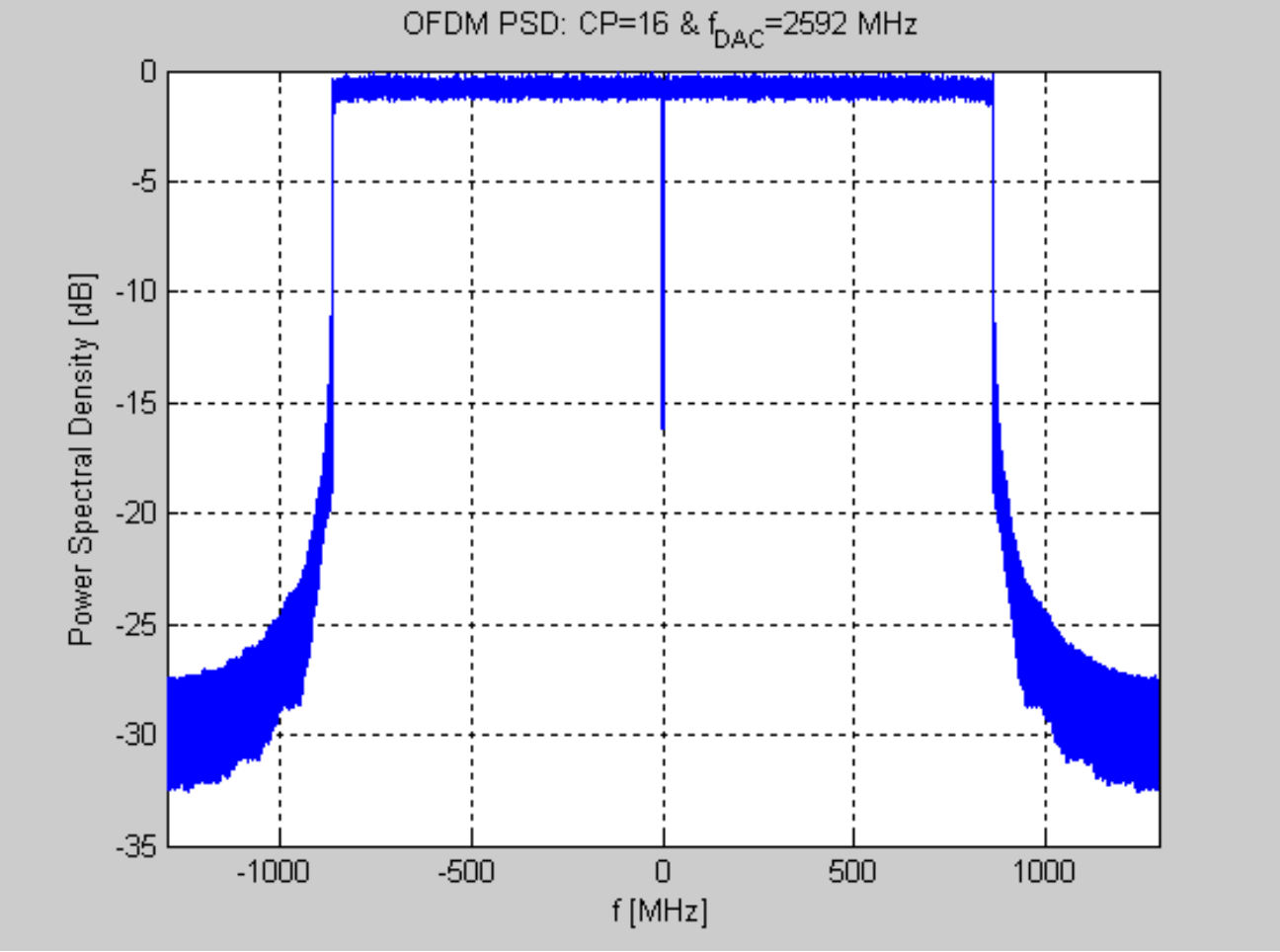
Pilot Structure (CP ≤ 64)



Pilot Structure (CP = 128)



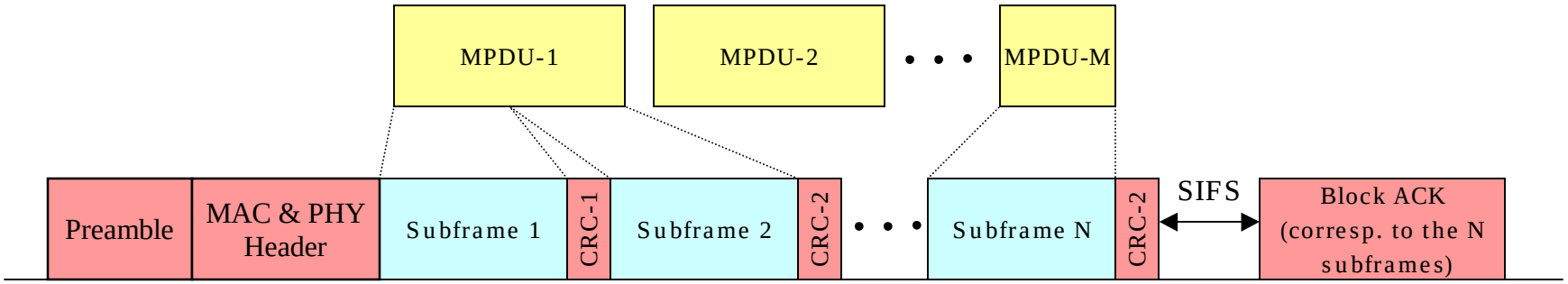
OFDM PSD



- Symbol Shaper & LPF are left to the implementer

MAC Enhancements

Aggregation Mode



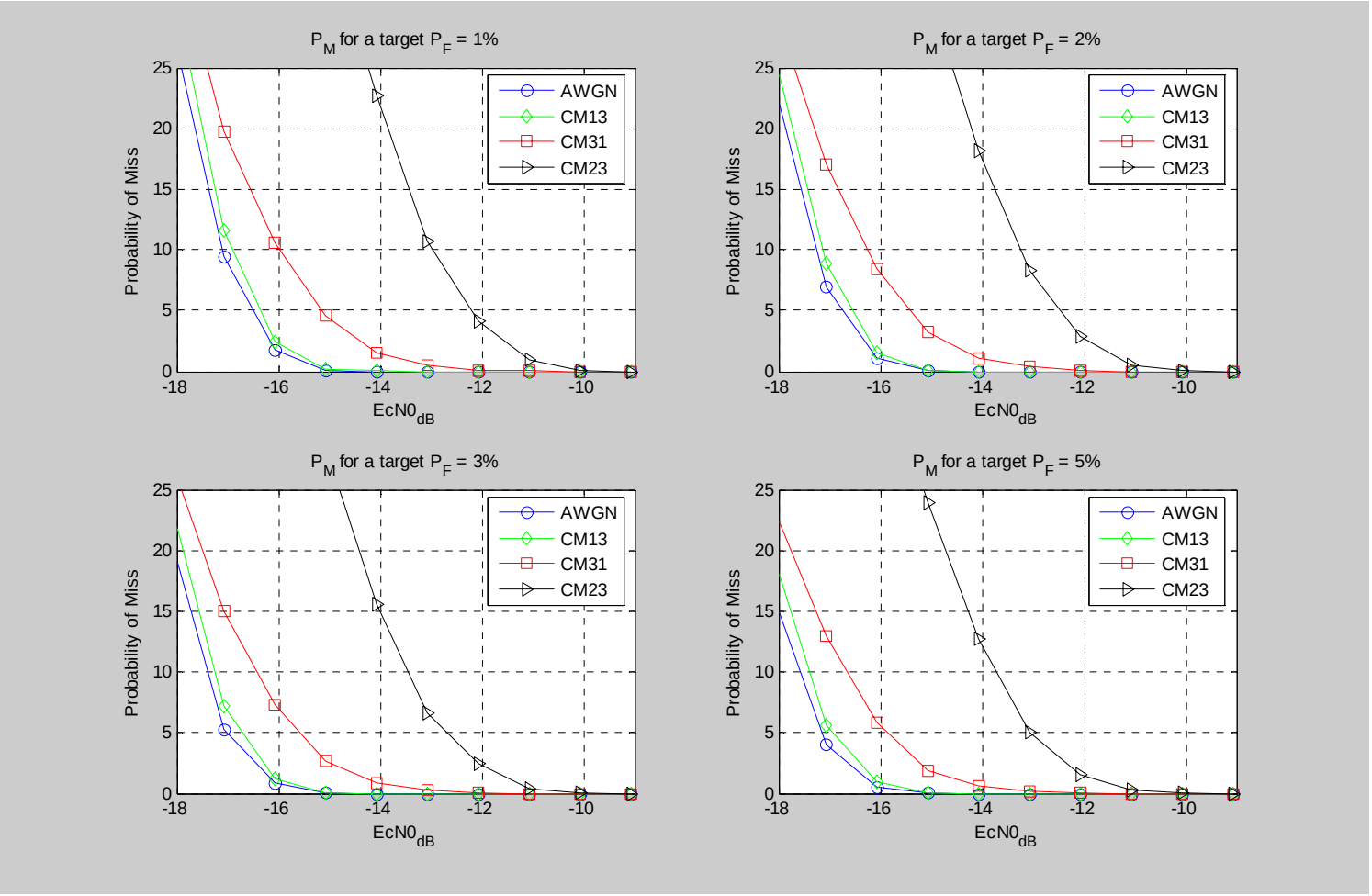
- PHY aggregation mode is highly efficient, minimizes the memory requirement at the device and is compliant with IEEE802.15.3b MAC
- MAC should support very lengthy MSDUs (and consequently very long MPDUs) or aggregated MPDUs,;
- PHY will fragment the frame into subframes, protect each subframe with its own CRC and allow retransmission of a subframe rather than the entire frame.
- The number of subframes can be negotiated between different devices. Once these parameters are negotiated they stay the same during one session. This reduces the overhead and these parameters need not be transmitted every frame or before each subframe.
- If errors occur at the receiving device, the receiving device will request from the transmitting device the retransmission of only those subframes in error and not the entire MPDU. This will increase the overall efficiency and capacity of the system.

Simulation Results

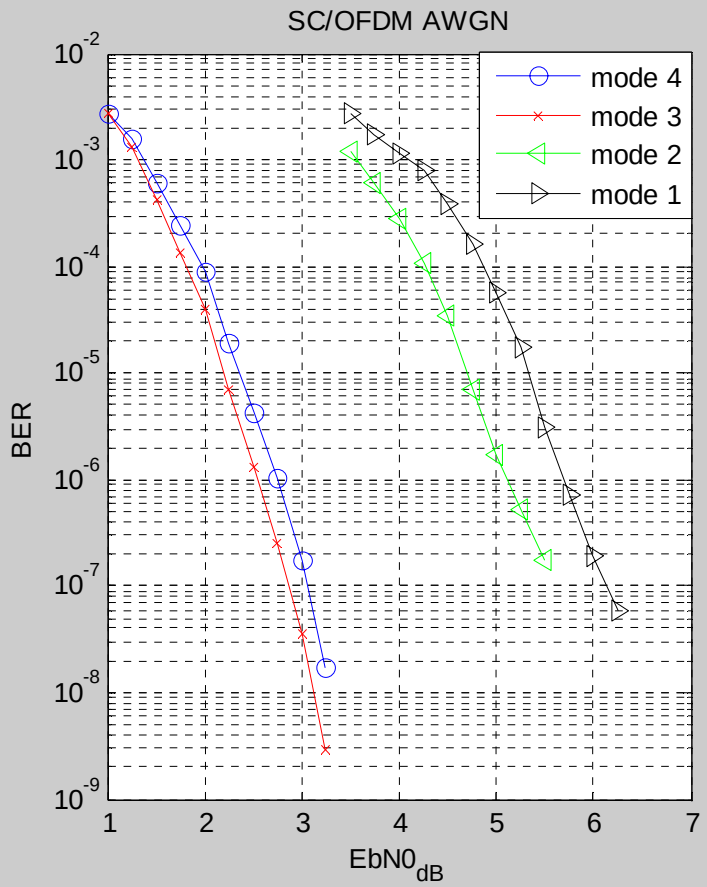
Simulation Assumptions

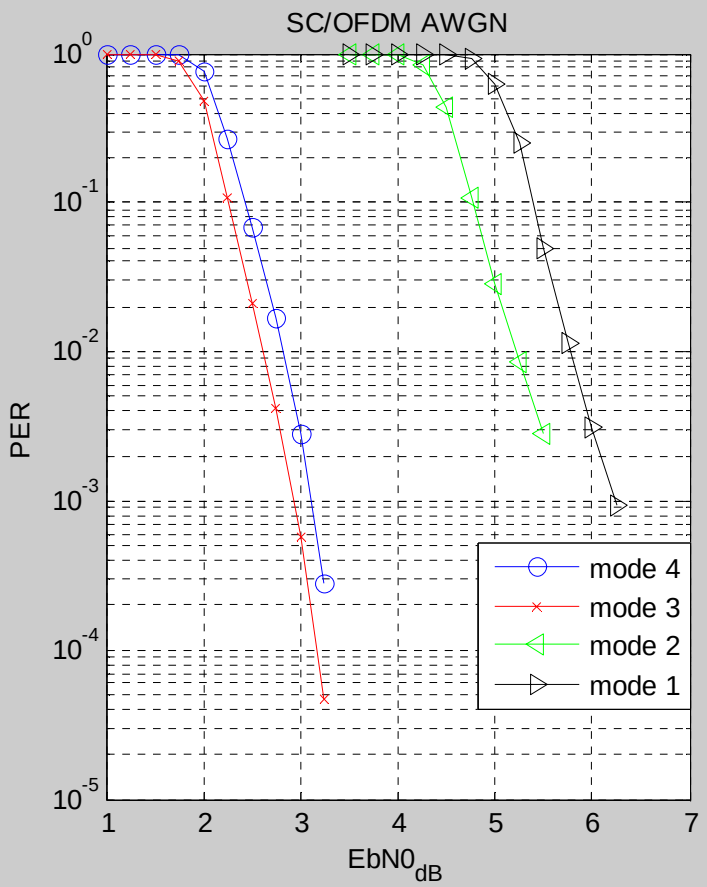
- Channel Bandwidth = 1720.32 MHz
- AWGN, CM13, CM23, CM31 (Golden Set)
- Omnidirectional antennas at both ends
- 50 ppm XTAL (±25 ppm @ each side)
- Simulation includes
  - Coarse/fine frequency acquisiton & tracking
  - Channel estimation
  - Frequency domain MMSE Equalizer
  - Soft bit generation
  - TLDPC & RS decoding

Long Preamble Miss Detection & False Alarm

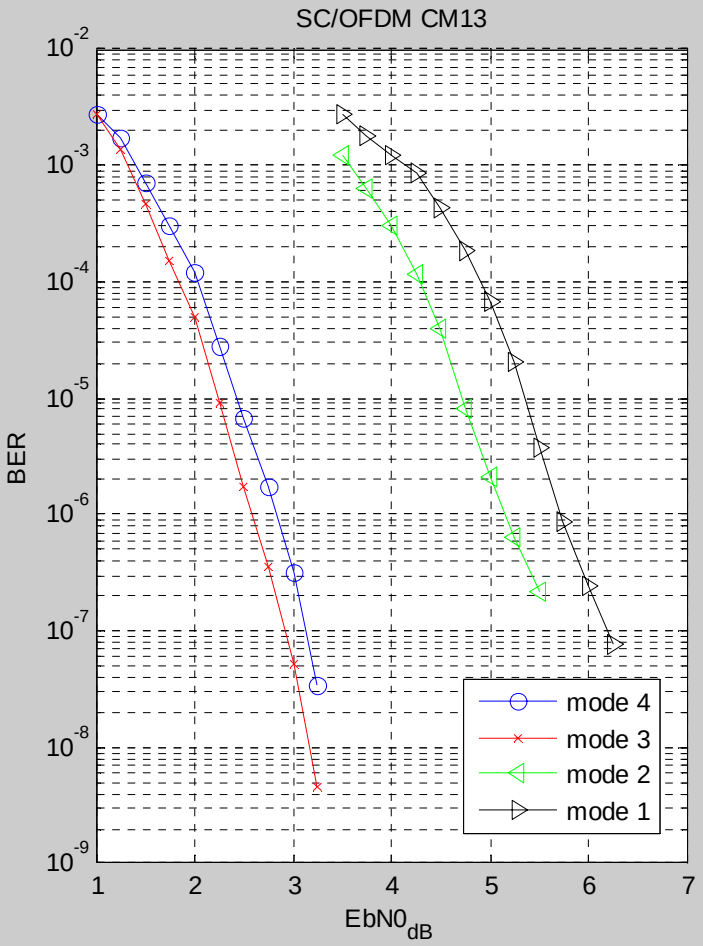


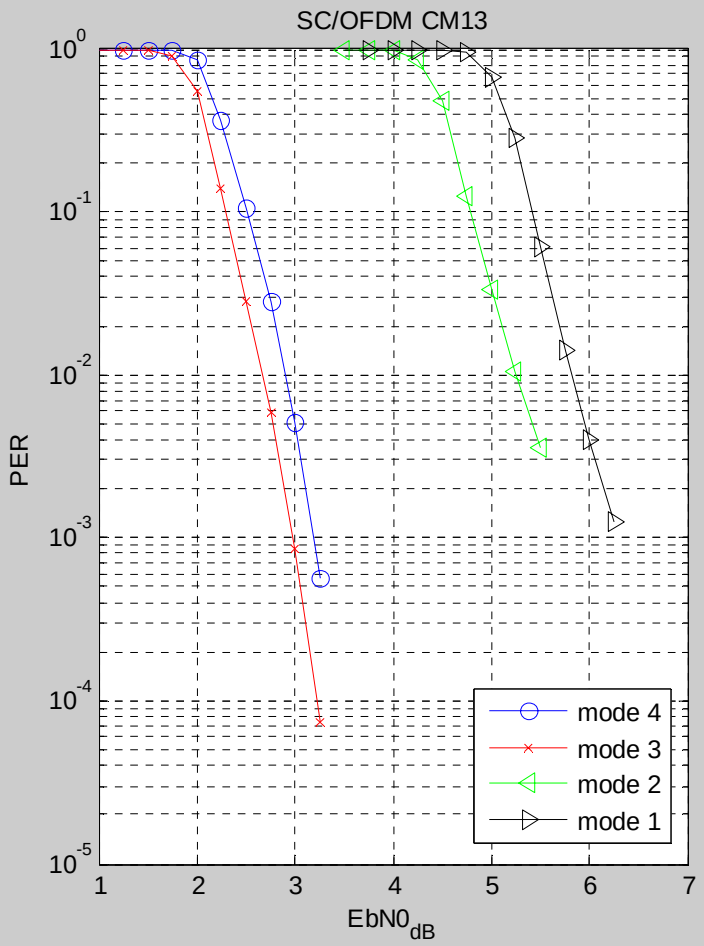
Simulation Results: AWGN



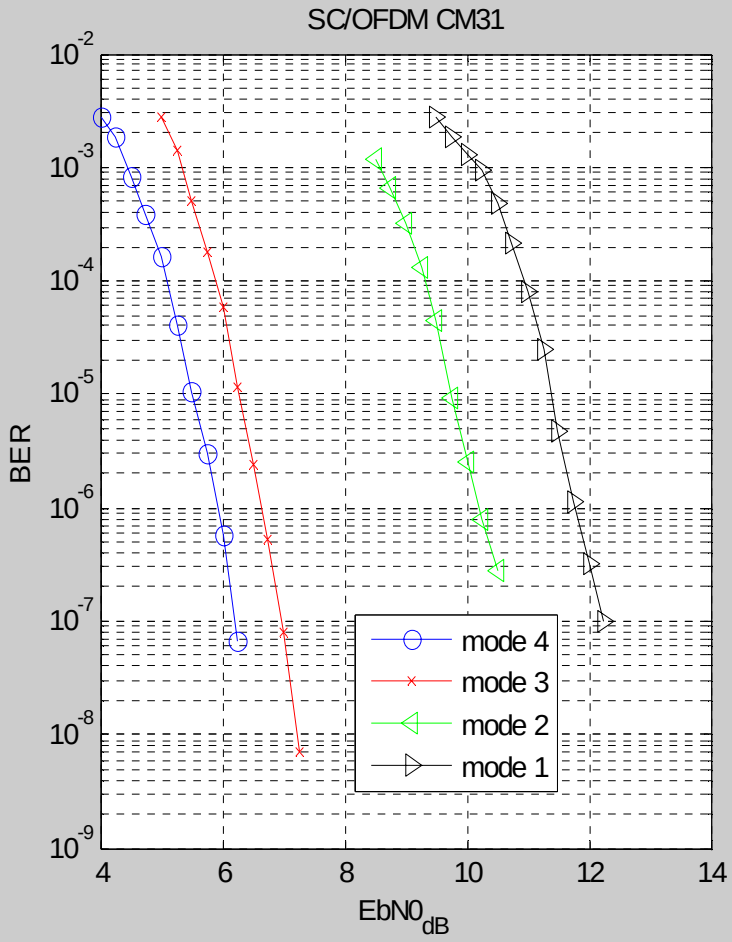


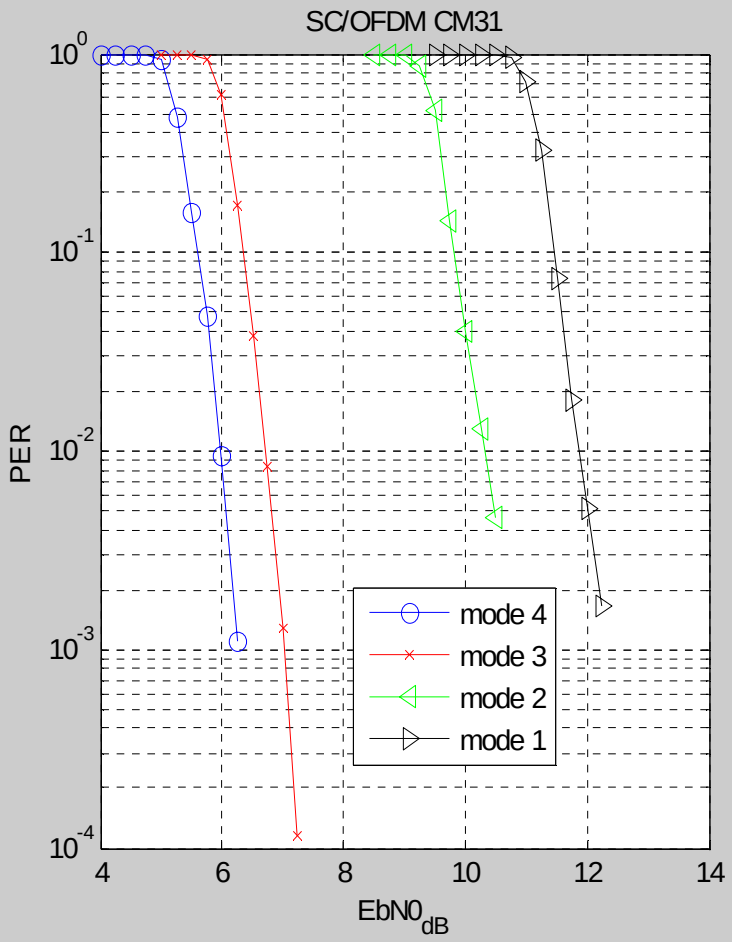
Simulation Results: CM13 (CP=0)



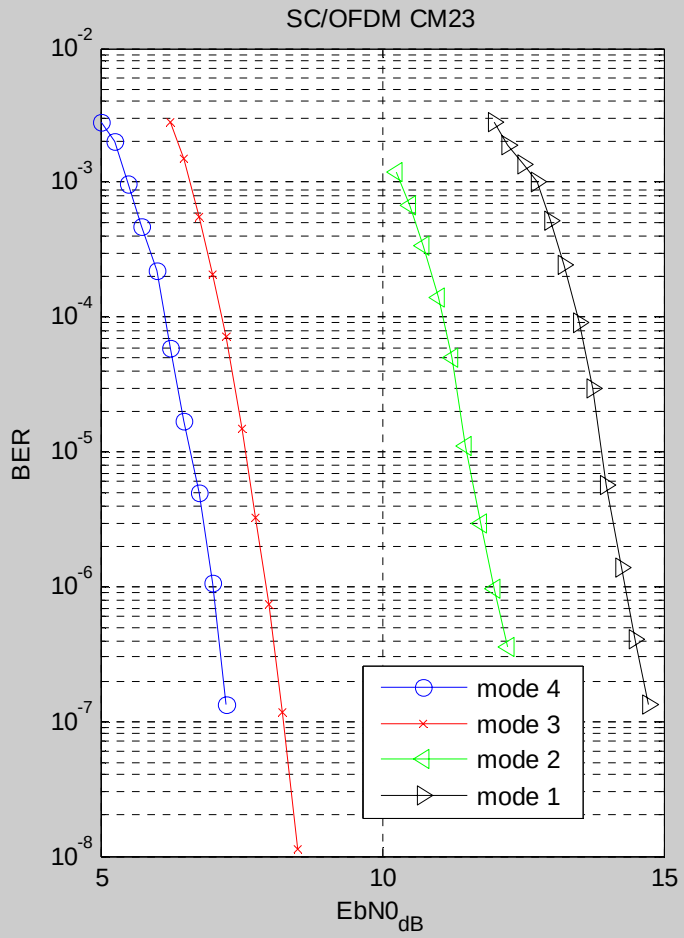


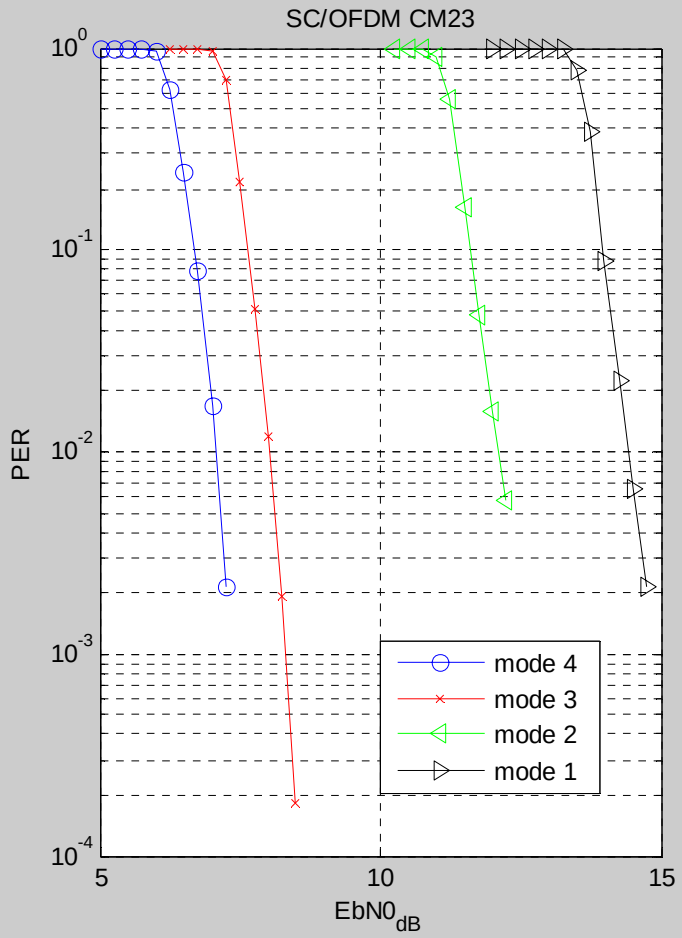
Simulation Results: CM31 (CP=64)





Simulation Results: CM23 (CP=64)





Link Budget: AWGN (8%PER)

Assumptions		
Radio Noise Figure	8.0	dB
Tx Antnna Gain	6.0	dB
Rx Antenna Gain	6.0	dB
High Data Rate Implementation Loss	0.0	dB
Medium/Low Data Rate Implementation Loss	0.0	dB

	Different Modes				
PARAMETERS	value	value	value	value	Unit
Transmitter					
Information Data Rate (Rb)	3967.962	2645.308	1511.605	755.802	Mbps
Geometric mean [fg = sqrt(fmin x fmax]	60.000	60.000	60.000	60.000	GHz
Bandwidth (BW)	1.7203	1.7203	1.7203	1.7203	GHz
Spectral DensityLimit	-22.36	-22.36	-22.36	-22.36	dBm/MHz
Tx Antenna Gain (GT)	6.0	6.0	6.0	6.0	dB
Tx Average Power (PT)	10.00	10.00	10.00	10.00	dBm
Receiver					
Rx Noise Figure Referred to the Antenna Terminal (NF)	8.0	8.0	8.0	8	dB
Eb/N0 (8% PER)	5.5	4.8	2.9	2.3	dB
Implementation Losses	0.0	0.0	0.0	0.0	dB
Rx Antenna Gain (GR)	6.0	6.0	6	6	
Sensitivity					
Propagation Loss Index	2	2	2	2	
Path Loss at 1m (L1)	68.00	68.00	68.00	68.00	dB
Minimum Rx Sensitivity Level (Smin)	-64.5	-67.0	-71.3	-74.9	dBm
Link Margin (M)	1.0	1.0	1.0	1.0	dB
Rx Power Caluclations					
Path Loss Ld = PR - (PT + GT + GR + M)	85.51	87.98	92.31	95.92	dB
Range d(m)	**7.51**	**9.97**	**16.41**	**24.86**	m

Link Budget: CM31 (8%PER)

Assumptions		
Radio Noise Figure	8.0	dB
Tx Antnna Gain	6.0	dB
Rx Antenna Gain	6.0	dB
High Data Rate Implementation Loss	0.0	dB
Medium/Low Data Rate Implementation Loss	0.0	dB

	Different Modes				
PARAMETERS	value	value	value	value	Unit
Transmitter					
Information Data Rate (Rb)	3967.962	2645.308	1511.605	755.802	Mbps
Geometric mean [fg = sqrt(fmin x fmax]	60.000	60.000	60.000	60.000	GHz
Bandwidth (BW)	1.7203	1.7203	1.7203	1.7203	GHz
Spectral DensityLimit	-22.36	-22.36	-22.36	-22.36	dBm/MHz
Tx Antenna Gain (GT)	16.0	16.0	16.0	16.0	dB
Tx Average Power (PT)	10.00	10.00	10.00	10.00	dBm
Receiver					
Rx Noise Figure Referred to the Antenna Terminal (NF)	8.0	8.0	8.0	8	dB
Eb/N0 (8% PER)	11.6	9.9	6.3	5.8	dB
Implementation Losses	0.0	0.0	0.0	0.0	dB
Rx Antenna Gain (GR)	16.0	16.0	16	16	
Sensitivity					
Propagation Loss Index	2.5	2.5	2.5	2.5	
Path Loss at 1m (L1)	68.00	68.00	68.00	68.00	dB
Minimum Rx Sensitivity Level (Smin)	-58.4	-61.9	-67.9	-71.5	dBm
Link Margin (M)	5.0	5.0	5.0	5.0	dB
Rx Power Caluclations					
Path Loss Ld = PR - (PT + GT + GR + M)	95.41	98.88	104.91	108.47	dB
Range d(m)	**2.61**	**3.59**	**6.25**	**8.68**	m

PHY-SAP Throughput

- Assumptions:
  - MPDU (MAC frame body + FCS) length = 16384 Octets
  - SIFS = 2.5 μs
  - MIFS = 0.5 μs

MPDU Length	Throughput @ 756Mbps	Throughput @ 1512Mbps	Throughput @ 2605Mbps	Throughput @ 3968Mbps
16384	586	1172	2020	3077

Summary

- Dual-mode SC (Single Carrier) / OFDM for different classes of devices
- SC is the mode of choice for low complexity medium data rate
- OFDM is the modulation of choice of very high data rate
- Low-complexity interoperability common mode for interoperability between different devices/networks
- Unified common frame format enabling a single HW supporting SC / OFDM
- Link Adaptation & Unequal Error Protection via low – complexity Structured Turbo LDPC, convolutional Codes / RS
- Balanced Channelization with multiple XTAL support