

**Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)****Submission Title:** [Dual-Mode Broadband and Wireless Network (DMBWN)]**Date Submitted:** [07 May, 2007]**Source:** [Ching-Kuang Tzung, Ta-Sung Lee\*, Jenn-Hwan Tarng\*, Yu-De Lin\*, Fu-Chiang Chen\*, Chi-Hsueh Wang, Tian-Wei Huang, Huei Wang, Shih-Yuan Chen, Powen Hsu, Tah-Hsiung Chu, Ruey-Beei Wu, and Chun-Hsiung Chen ]

Company [Department of Electrical Engineering, National Taiwan University, \* National Chiao Tung University, Hsin-Chu, Taiwan, ]

Address [No.1, Sec. 4, Roosevelt Road, Taipei 10617, Taiwan, R.O.C. ]

Voice:[+886 2 2363 3289], FAX: [+886 2 2368 3824 ], E-Mail:[cktzuang@cc.ee.ntu.edu.tw]

**Re:** []**Abstract:** [Description of the concept of Dual-Mode Broadband and Wireless Network]**Purpose:** [Contribution to TG3c at May 2007 meeting.]**Notice:** This document has been prepared to assist the IEEE P802.15. It is offered as a basis for discussion and is not binding on the contributing individual(s) or organization(s). The material in this document is subject to change in form and content after further study. The contributor(s) reserve(s) the right to add, amend or withdraw material contained herein.**Release:** The contributor acknowledges and accepts that this contribution becomes the property of IEEE and may be made publicly available by P802.15.

# Dual-Mode Broadband and Wireless Network (DMBWN)

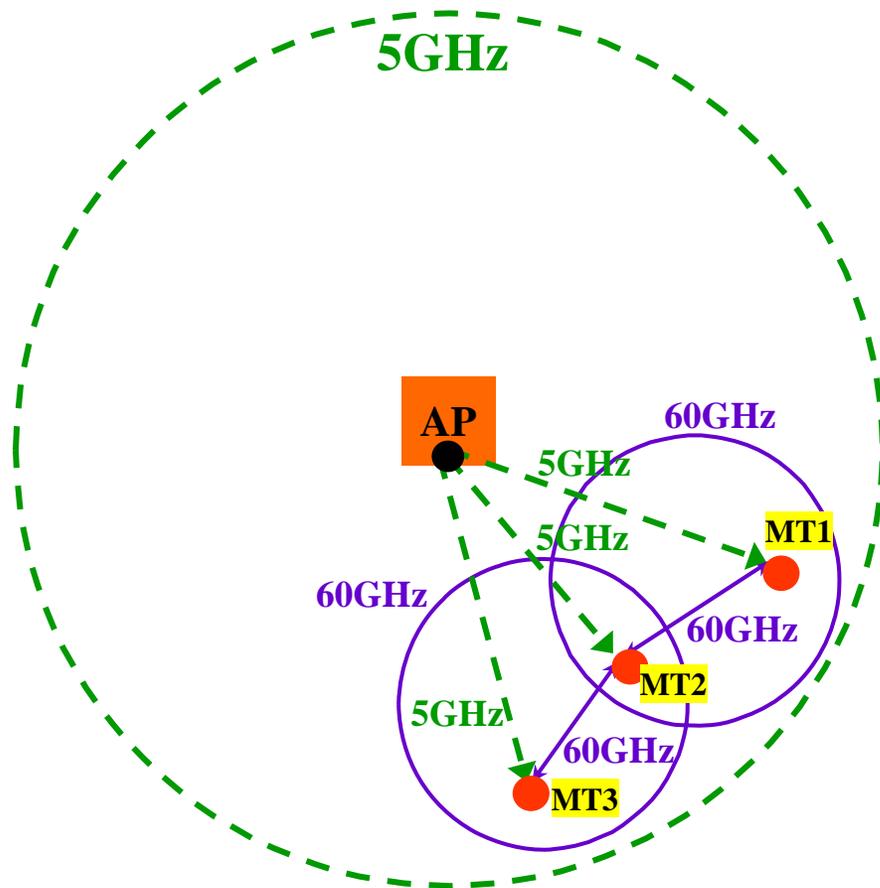
**Ching-Kuang Tzung, Ta-Sung Lee\*, Jenn-Hwan Tarng\*, Yu-De Lin\*,  
Fu-Chiang Chen\*, Chi-Hsueh Wang, Tian-Wei Huang, Huei  
Wang, Shih-Yuan Chen, Powen Hsu, Tah-Hsiung Chu, Ruey-  
Beei Wu, and Chun-Hsiung Chen**

**National Taiwan University**

**\*National Chiao Tung University**

**May 07, 2007**

# Dual-Mode Broadband and Wireless Network (DMBWN): a **backward compatible** system concept



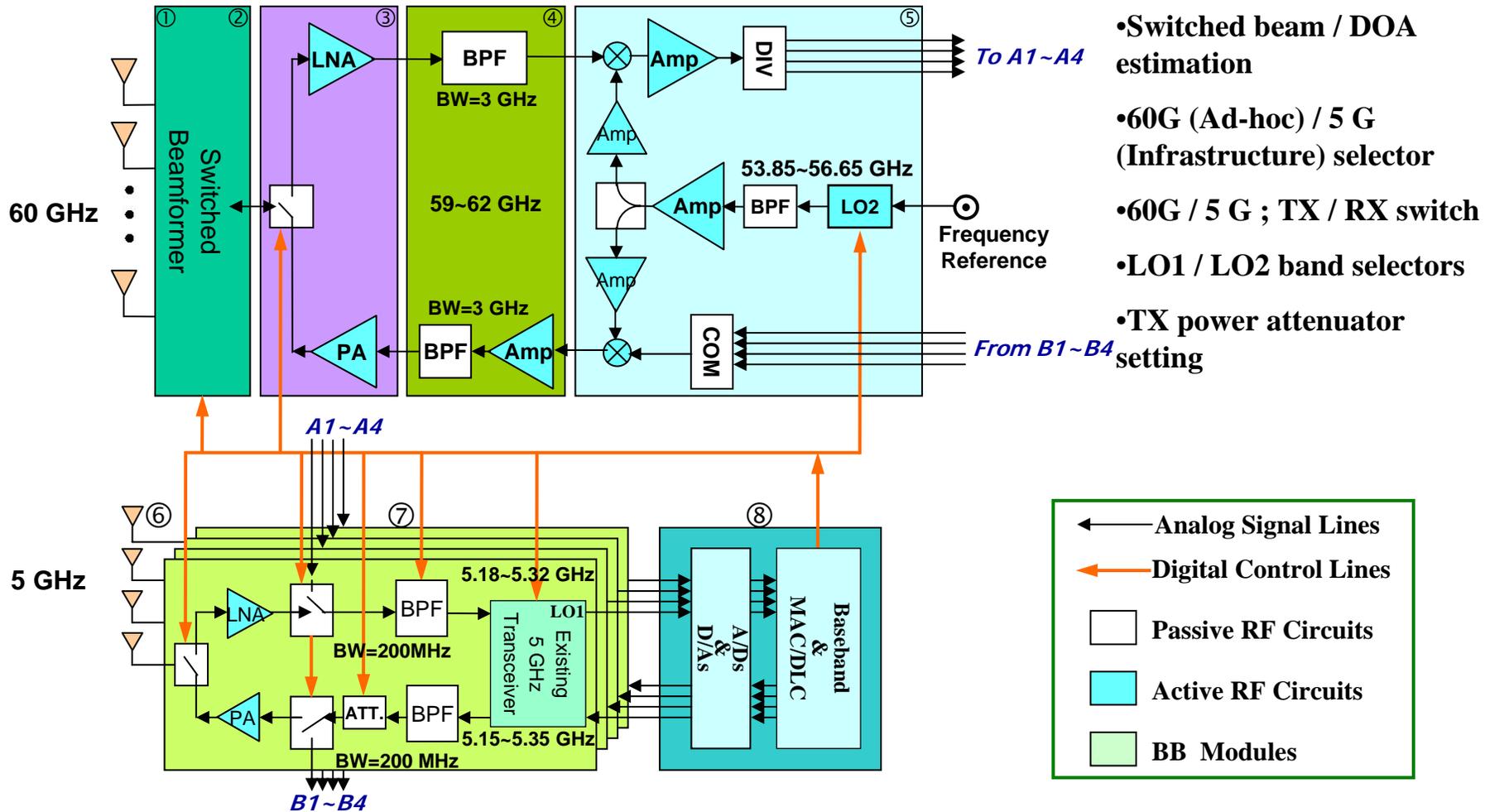
RF front-end architecture for 5GHz / 60GHz RF signal transmission/reception

Smart antenna array based on switched beamforming

# Motivation & Overview

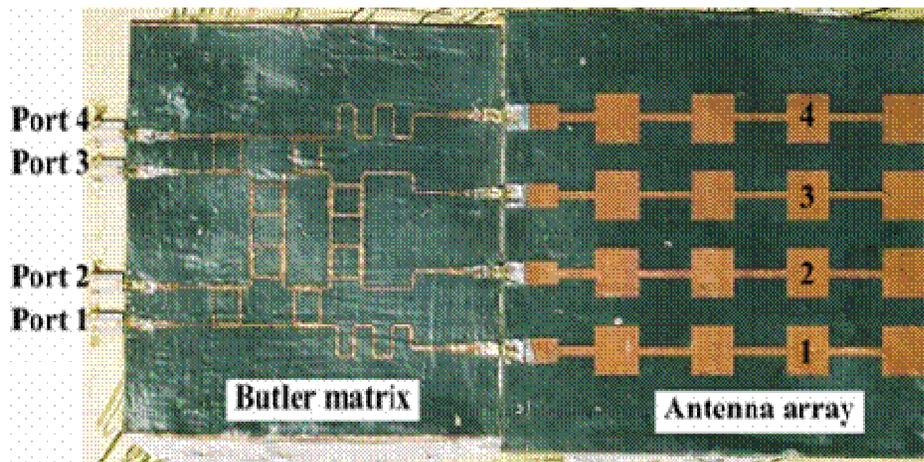
- **Long Range:** lower operation frequency for communicating long-distance terminals.
- **Backward Compatible System:** the baseband realization is highly compatible with the OFDM based IEEE 802.11a/n standard.
- **5-GHz band,**
  - Infrastructure mode
  - MIMO-OFDM technique is adopted to improve the performance
- **60-GHz band,**
  - ad-hoc mode
  - Single -Carrier with Frequency-Domain Equalization (SC-FDE) strategy combined with switched beamforming for interference suppressing

# 60/5 GHz Dual-Mode Wireless Network Station

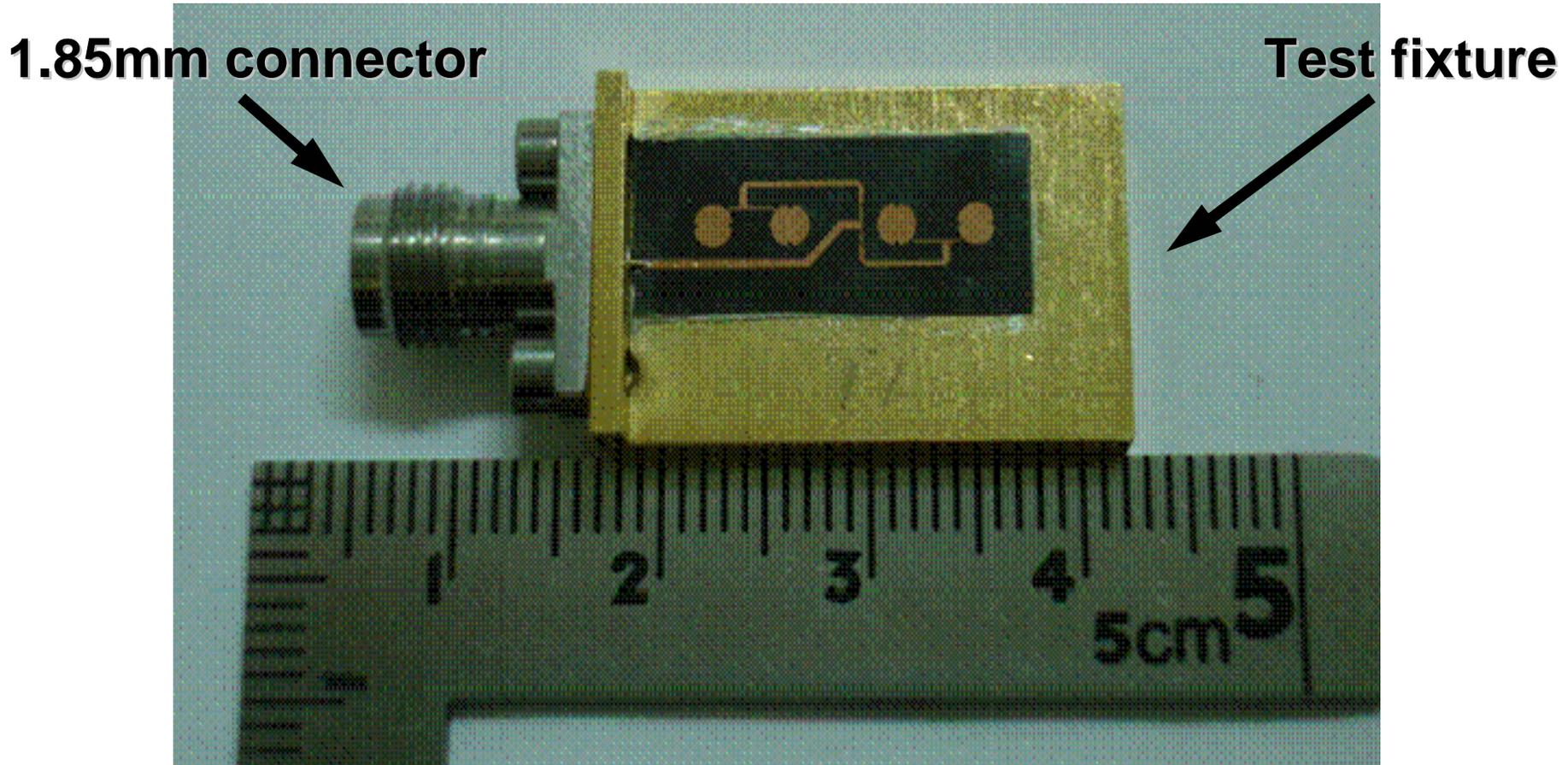


# 60-GHz Switched-Beam Antenna

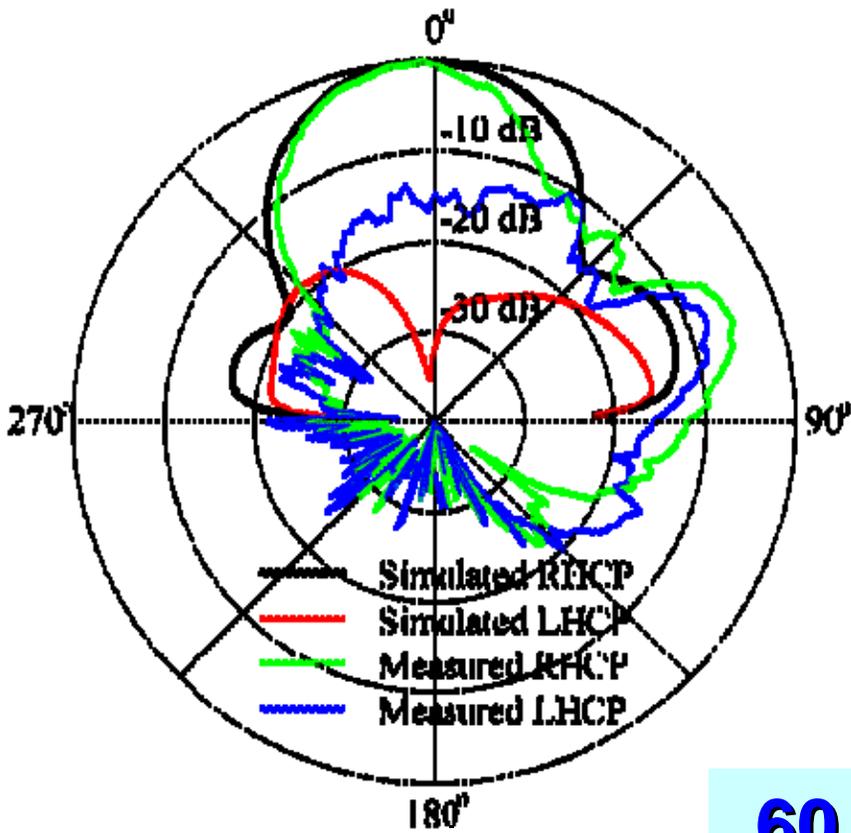
- 60-GHz switched-beam antenna array has been developed in National Taiwan University
  - Linear polarization  $\rightarrow$  circular polarization
  - 4 elements  $\rightarrow$  8 elements



# Photo of 1×4 Circular Patch Array

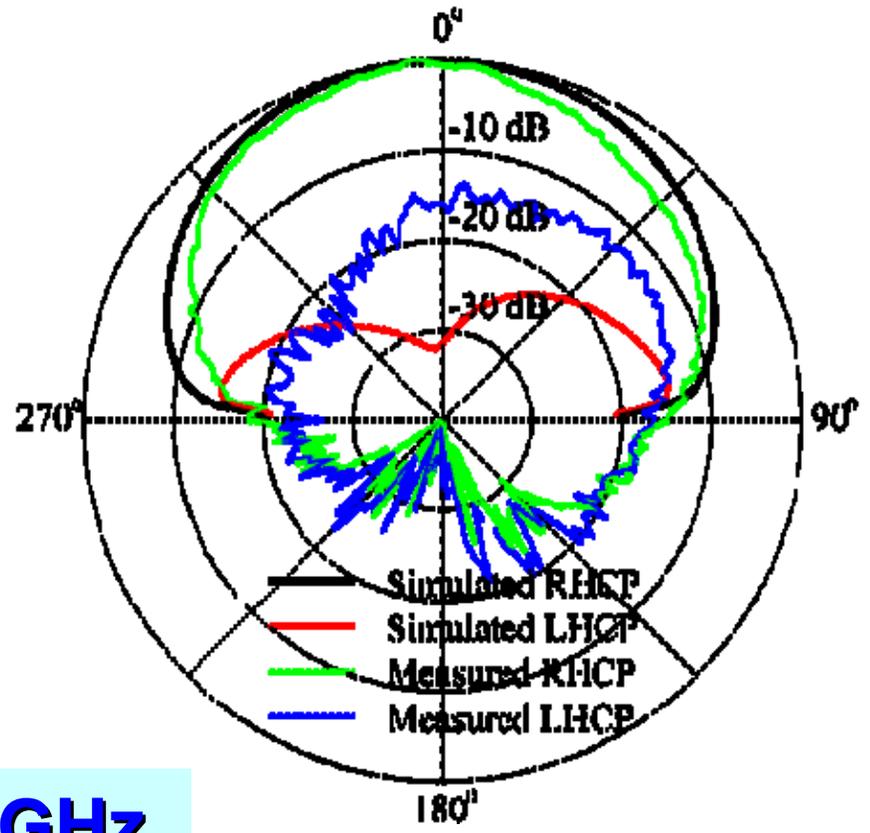


# Radiation Patterns (1×2 array)



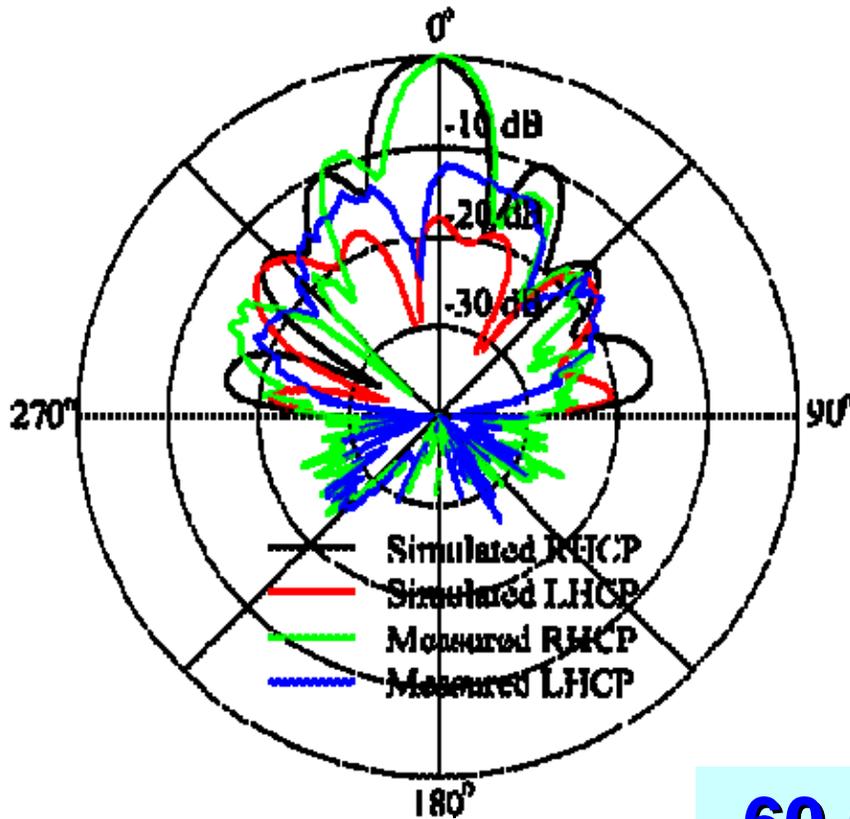
**x-z plane**

**60.5 GHz**

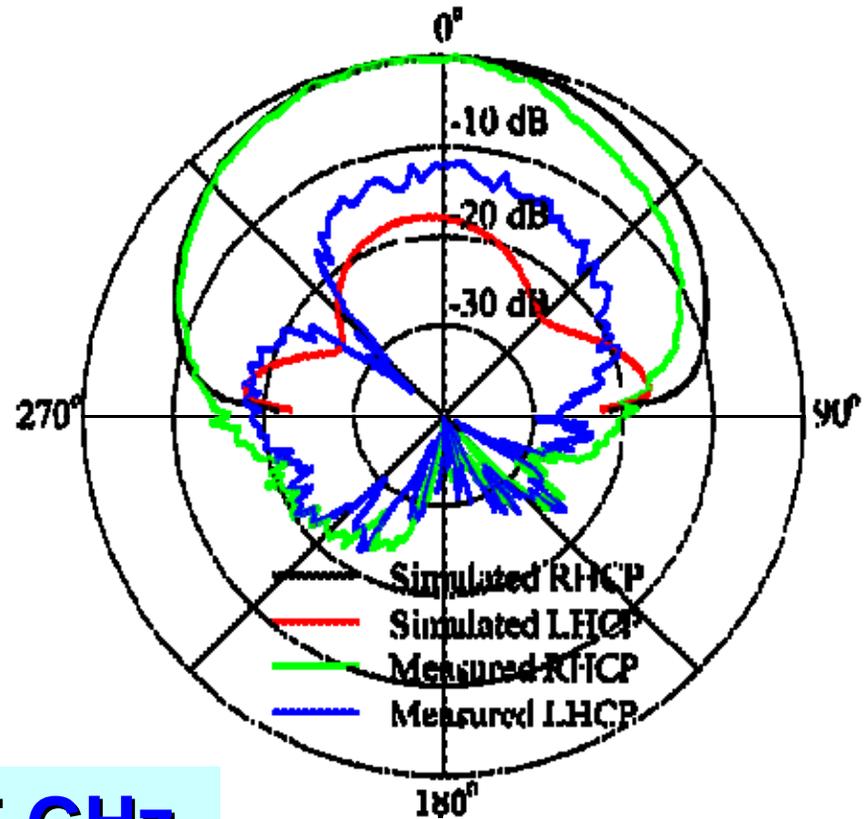


**y-z plane**

# Radiation Patterns (1×4 array)



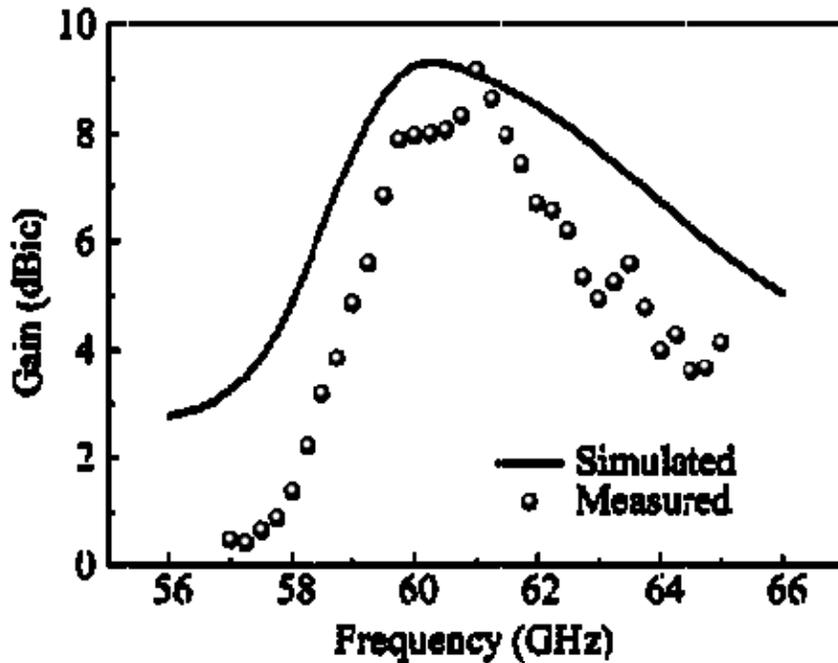
**x-z plane**



**y-z plane**

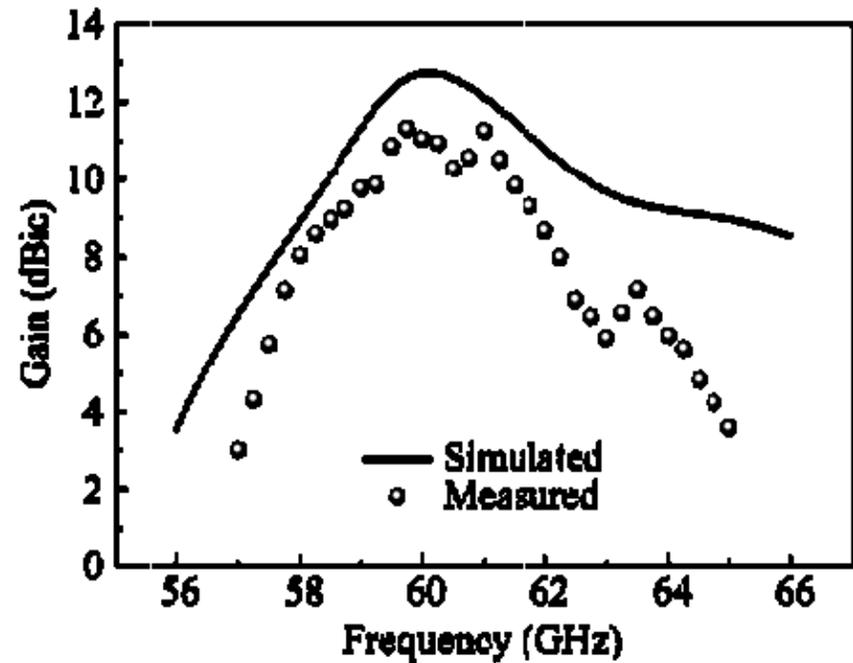
**60.5 GHz**

# In-Band Peak Gains



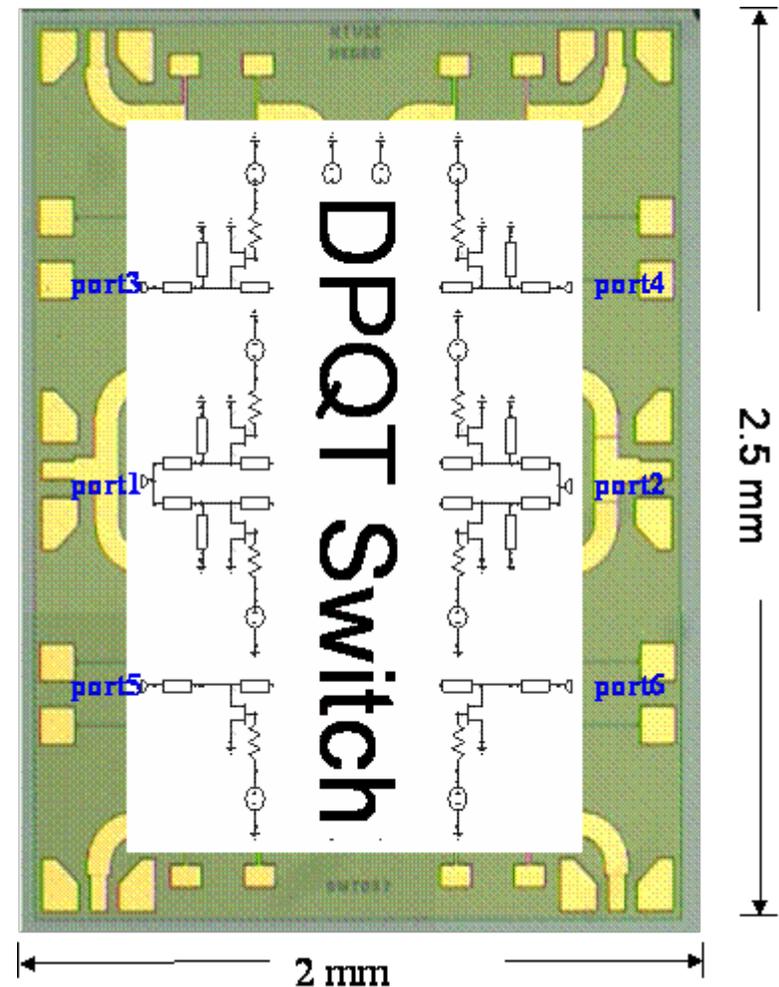
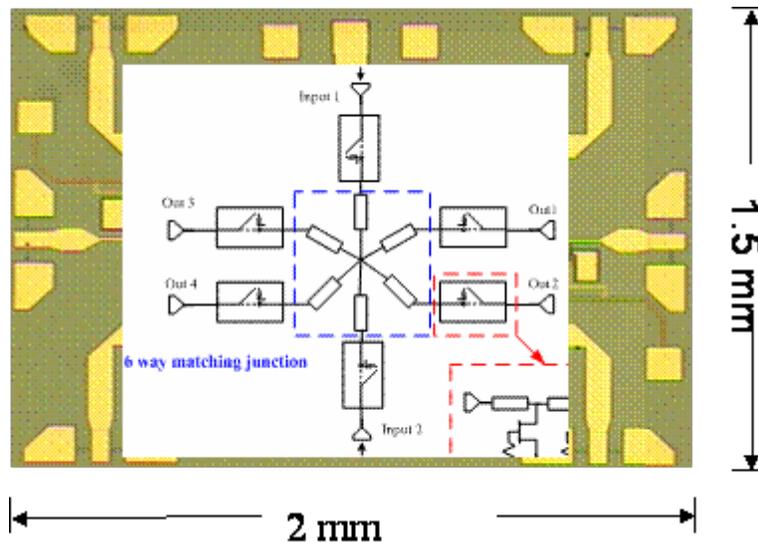
**1×2 array**

**RHCP**



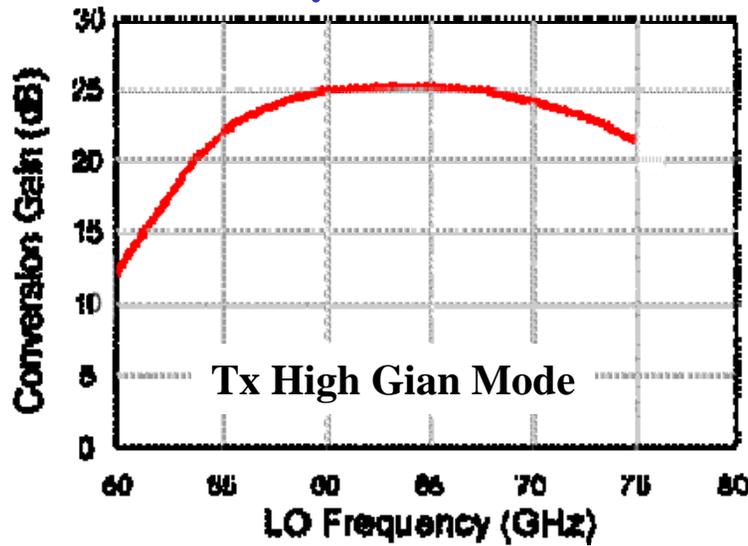
**1×4 array**

# 60GHz DPQT Switch

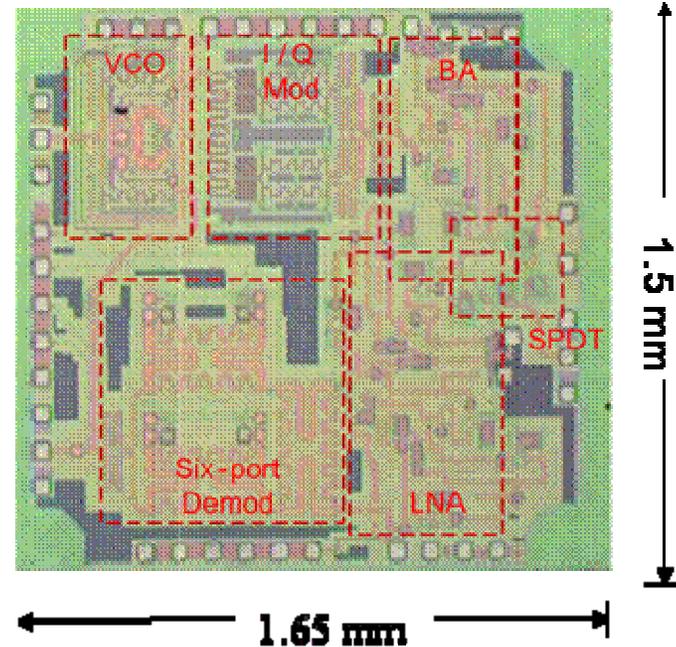
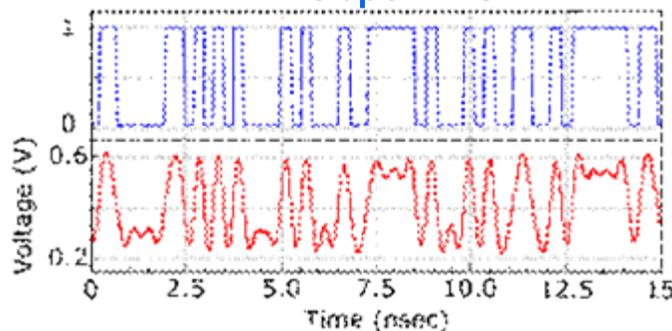


- ❑ 0.15 mm PHEMT , DPQT Switch
- ❑ Low insertion loss at 60GHz
- ❑ High isolation

# A 0.13 $\mu\text{m}$ CMOS 60-GHz Transceiver



Rx: 4Gbps BPSK



- ❑ Low power consumption (97mW)
- ❑ Tx Pout = -2dBm, IQ Modulation
- ❑ Miniature chip size, and **Low Cost**

C-H. Wang, H-Y. Chang, P-S. Wu, K-Y. Lin, T-W. Huang, H. Wang, C-H. Chen, "A 60GHz Low-Power Six-Port Transceiver for Gigabit Software-Defined Transceiver Applications," 2007 *International Solid-State Circuit Conference (ISSCC)*, San Francisco, CA, Feb. 2007.

# 25-75 GHz 90nm CMOS Gilbert-cell Mixer

Process : 90nm CMOS

Topology : Gilbert-cell

Chip size: 0.55 mm × 0.55 mm

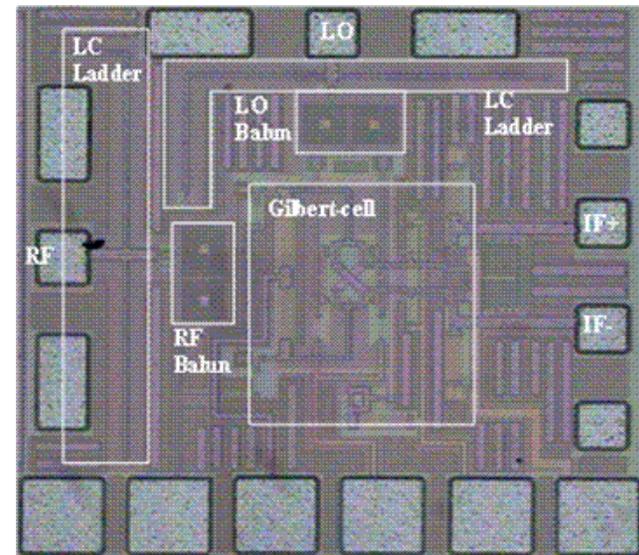
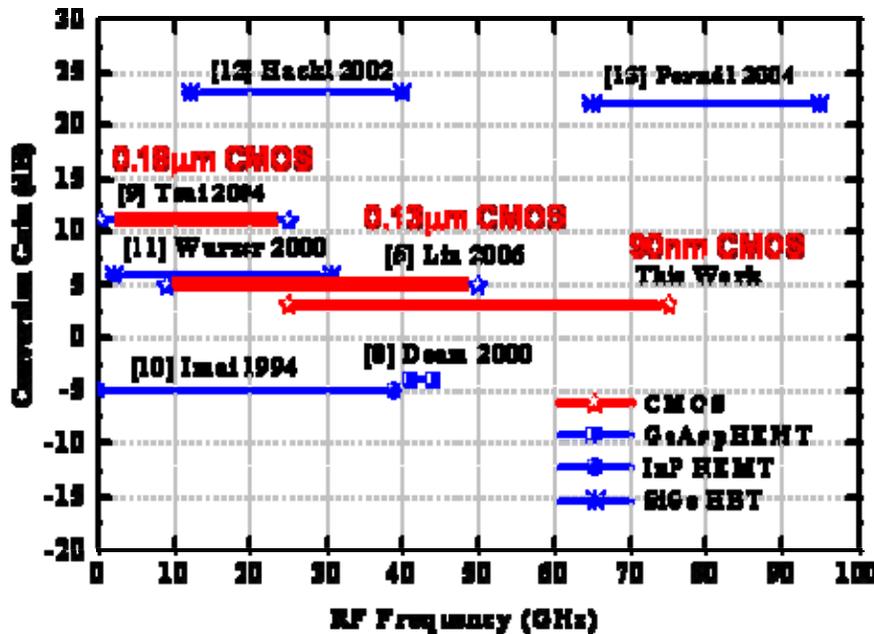
RF Frequency : 25-75 GHz

Conversion Gain :  $3 \pm 2$  dB

LO Driver Power : 6 dBm

Power Consumption : 93 mW

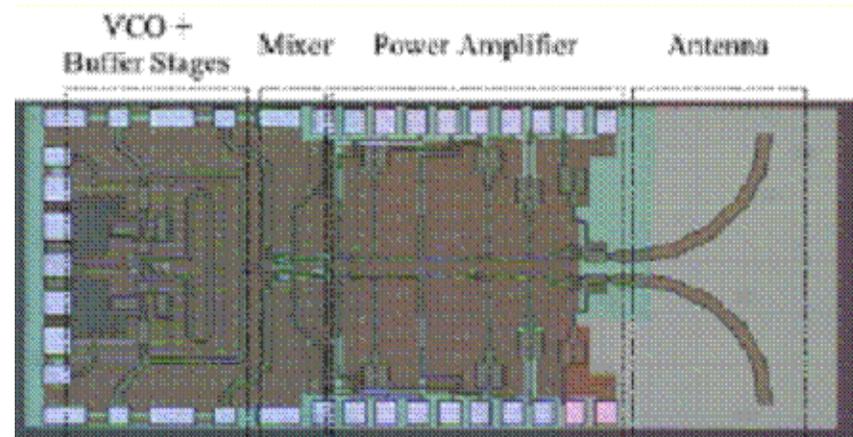
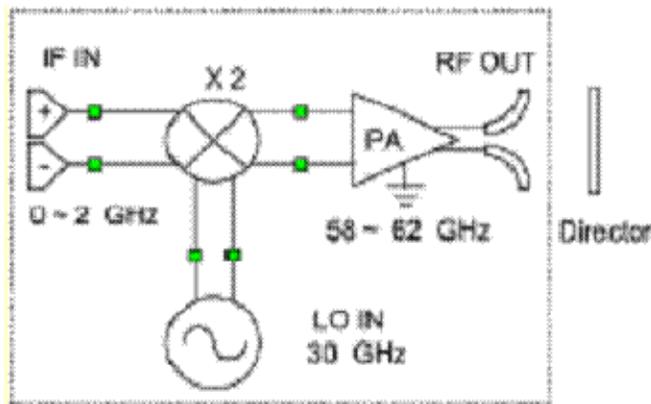
Isolation : 30 dB



Jeng-Han Tsai, Pei-Si Wu, Chin-Shen Lin, Tian-Wei Huang, John G.J. Chern, and Wen-Chu Huang, " A 25-75-GHz Broadband Gilbert-cell Mixer Using 90-nm CMOS Technology," *IEEE Microwave and Guided Wave Letters*, April 2007.

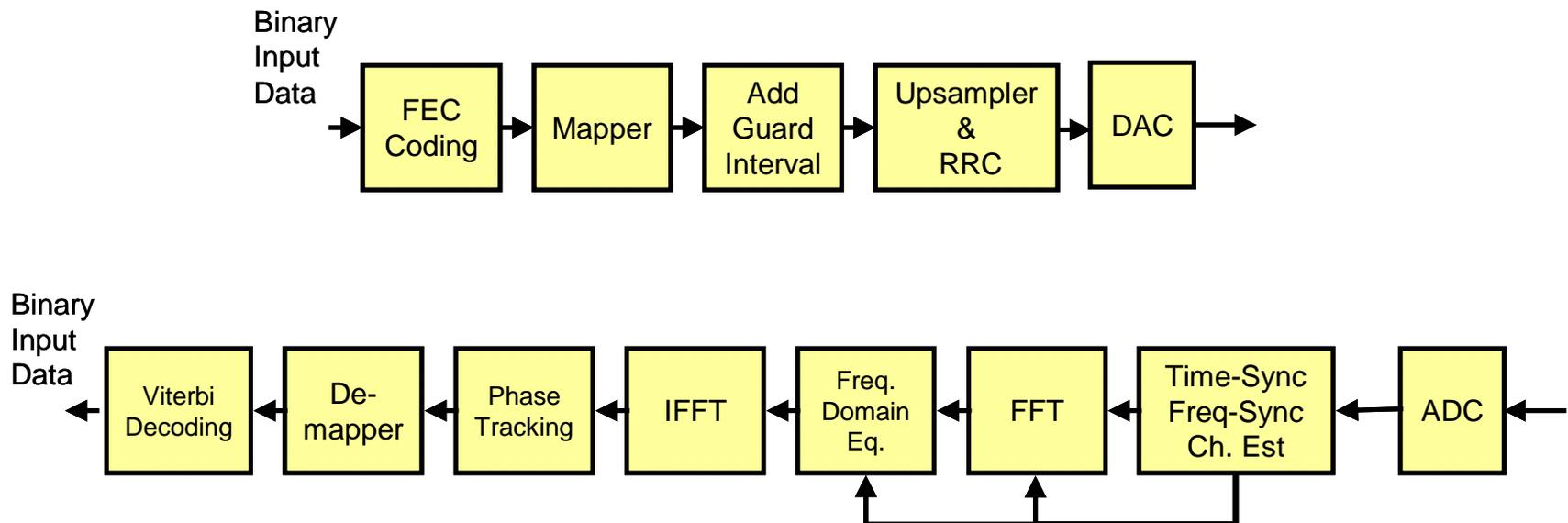
# 60-GHz Transmitter with Integrated Antenna

- Technology: 0.18- $\mu$  m SiGe BiCMOS process
- Chip size: 1.3 x 0.8 mm<sup>2</sup>
- Conversion gain: 20.2 dB
- Output power: 15.8 dBm
- DC power consumption: 281 mW



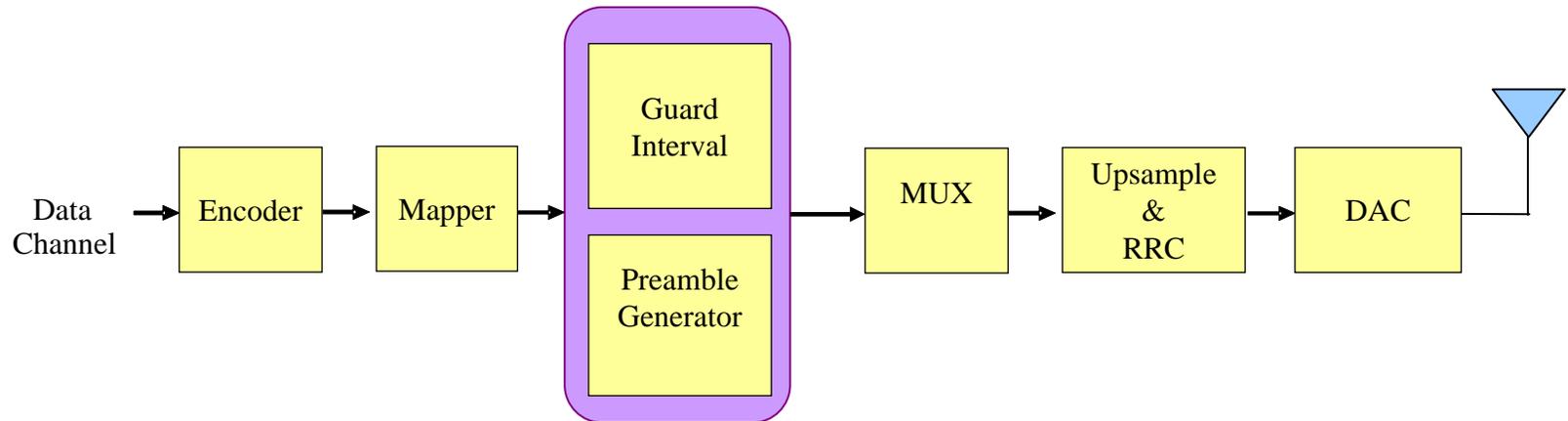
Chi-Hsueh Wang, Yi-Hsien Cho, Chin-Shen Lin, Huei Wang, Chun-Hsiung Chen, Dow-Chih Niu, John Yeh, Chwan-Ying Lee, and John Chern, "A 60-GHz transmitter with integrated antenna in 0.18-mm SiGe BiCMOS technology," 2006 *International Solid-State Circuit Conference (ISSCC)*, San Francisco, CA, Feb. 2006.

# 60-GHz Single Carrier Baseband (1)



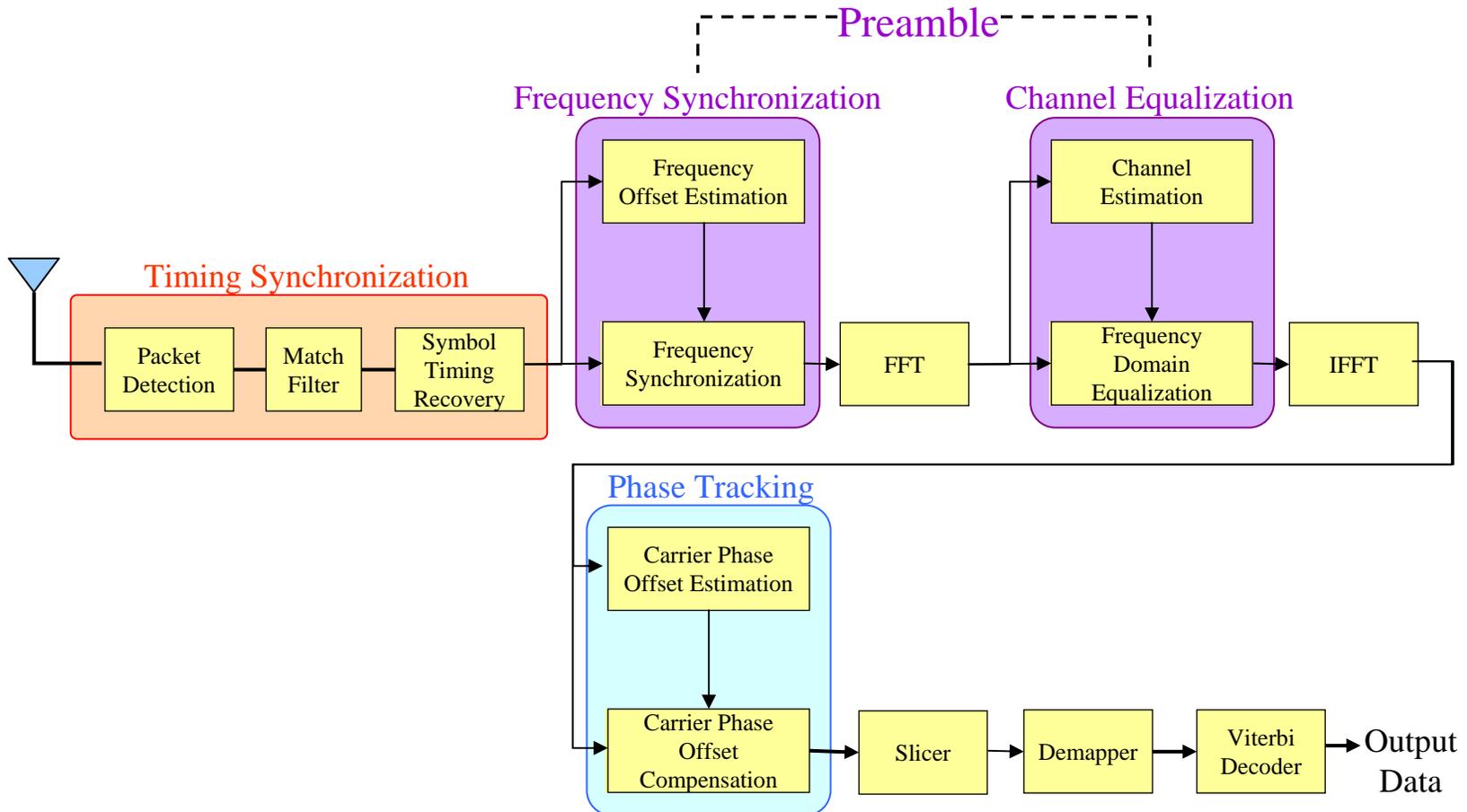
Diagrammatical description of the SC-FDE system.

# 60-GHz Single Carrier Baseband (1)



Diagrammatical description of the SC-FDE transmitter

# 60-GHz Single Carrier Baseband (2)



Diagrammatical description of the SC-FDE receiver

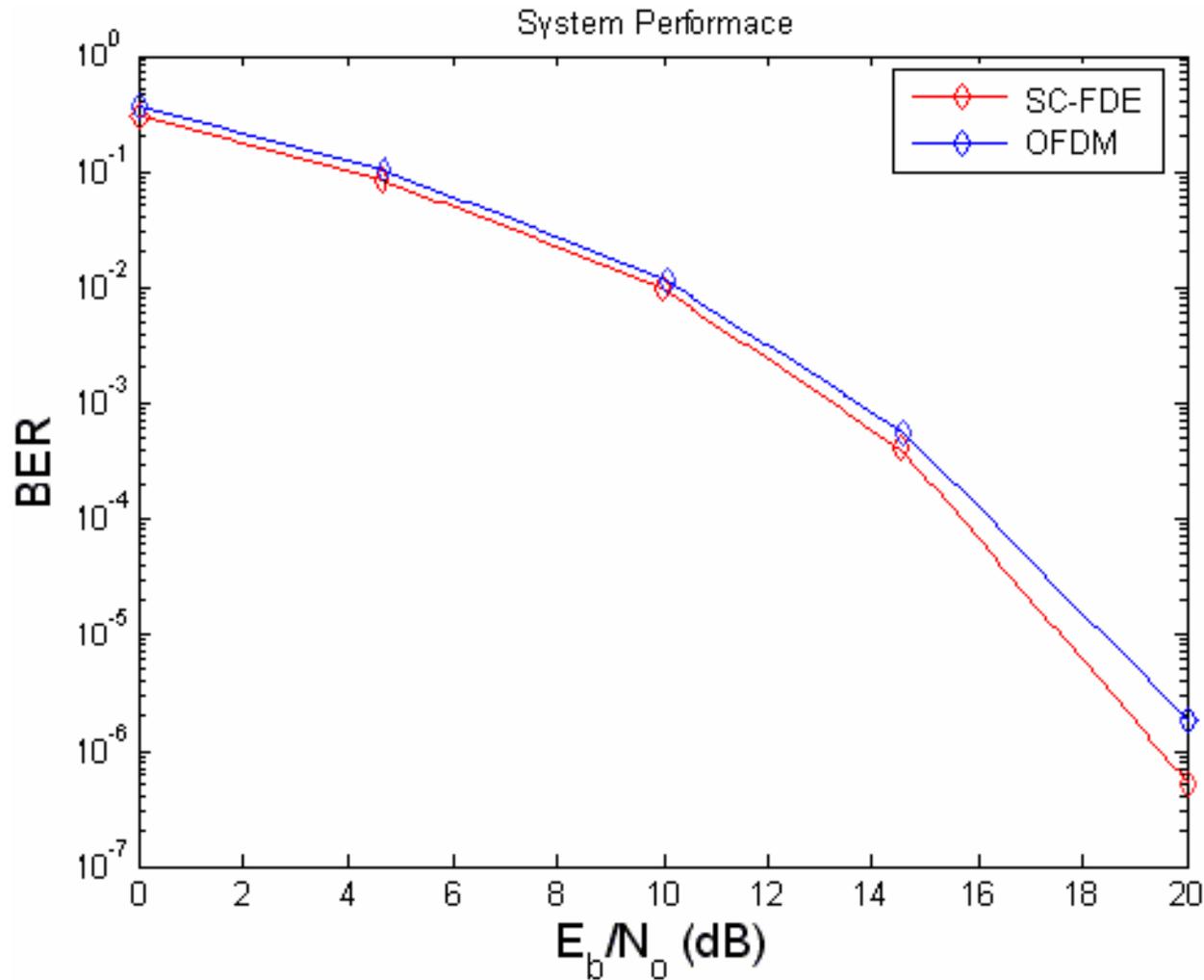
# Functionality Description of Single Carrier Transceiver

- **Transmitter**
  - **Preamble:** The preamble channels, following the structure used in IEEE 802.11a, is attached in front of the data
  - **Upsample & RRC (Polyphase Interpolator):** Most of the samples in the upsampled signal are zero and thus required no operations in root-raised cosine filter. With the polyphase structure, a factor of  $L$  (the upsample rate) is saved for computation
- **Receiver**
  - **Symbol Timing Recovery:** To sample message signals at the receiver, a delay-locked loop is used to find the peaks of the output waveforms
  - **Frequency Estimation:** Short preamble is used to correct the frequency offset
  - **Channel Estimation:** Long preamble is used to perform channel estimation in the frequency domain
  - **Phase Estimation:** To correct the frequency offset that varies during the reception of the packet

# Parameters of Single Carrier Transceiver

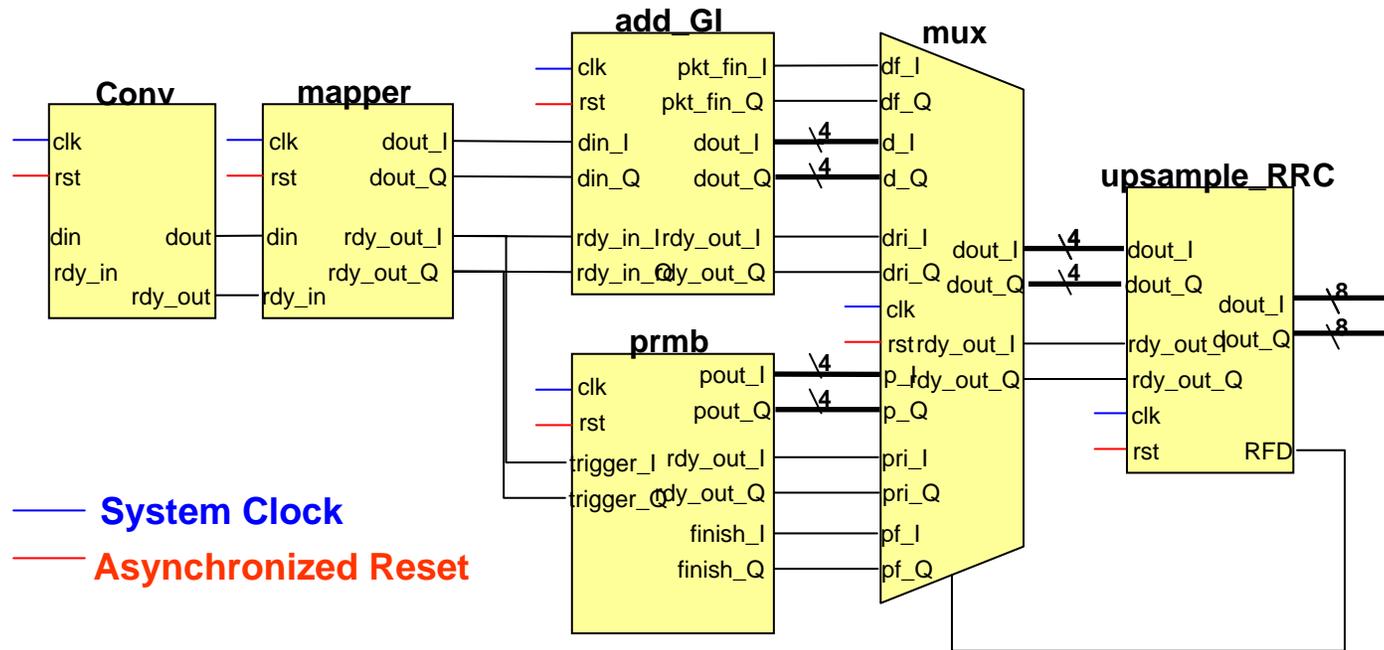
Number of frames/packet	6
Number of total symbols/frame	64
Number of data symbols/frame ( $N_S$ )	48
Number of Guard Interval symbols/frame ( $N_G$ )	16
FFT Size	64
Long Preamble Size (symbols)	64+16 (CP)
Short Preamble Size (symbols)	16
Modulation Schemes	QPSK
Coding Rates	1/3
Pulse Shaping	RRC ( $\alpha=0.25$ )

# Performance of Single Carrier Receiver



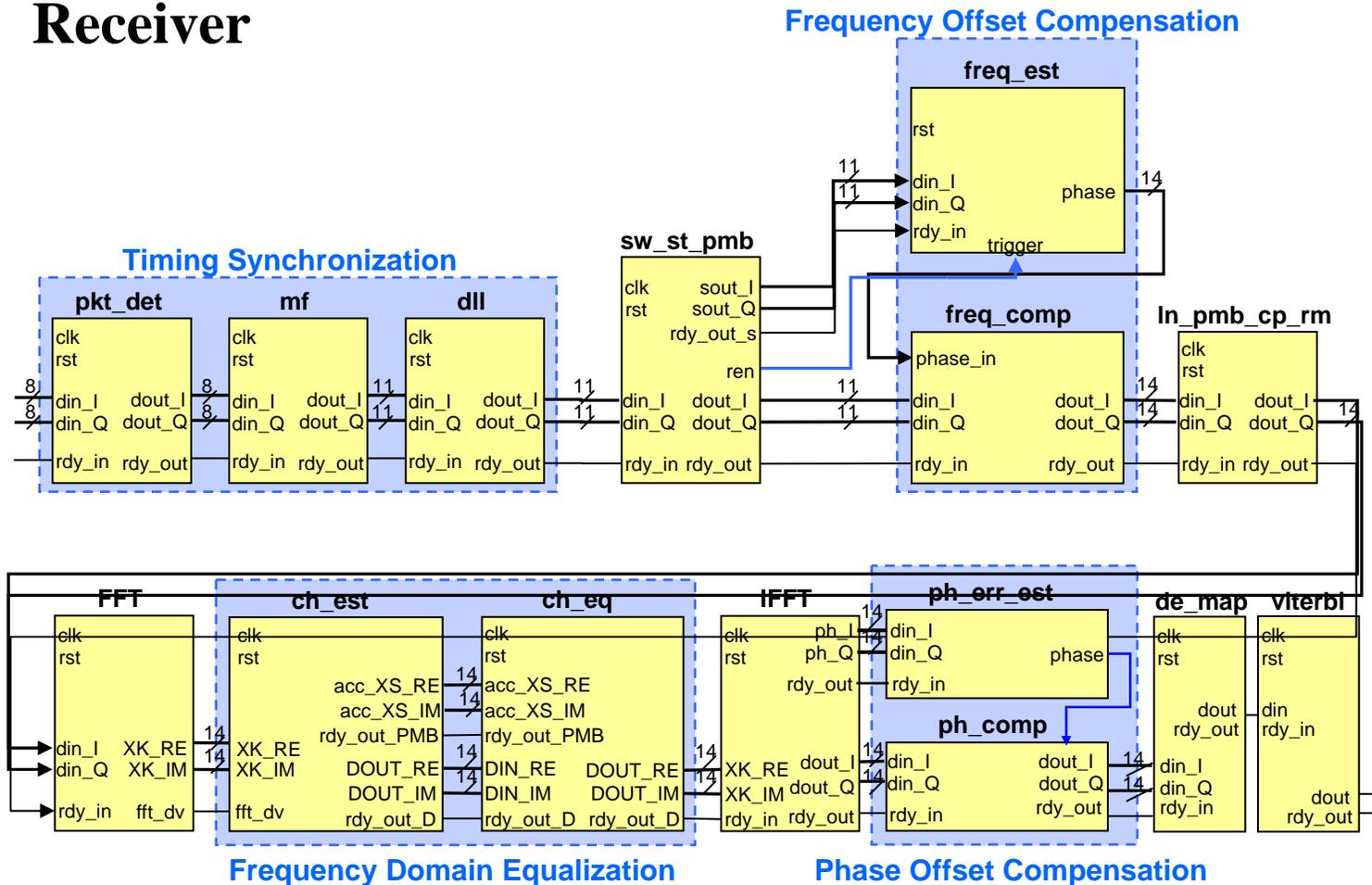
# 60-GHz Single Carrier Baseband HW Architecture (1)

- Transmitter



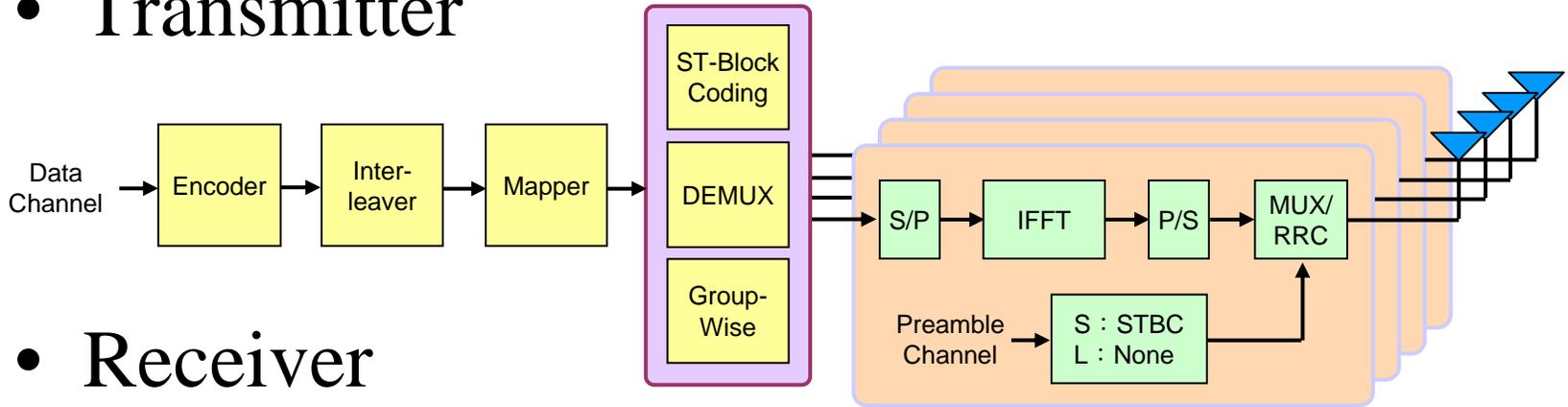
# 60-GHz Single Carrier Baseband HW Architecture (2)

- Receiver

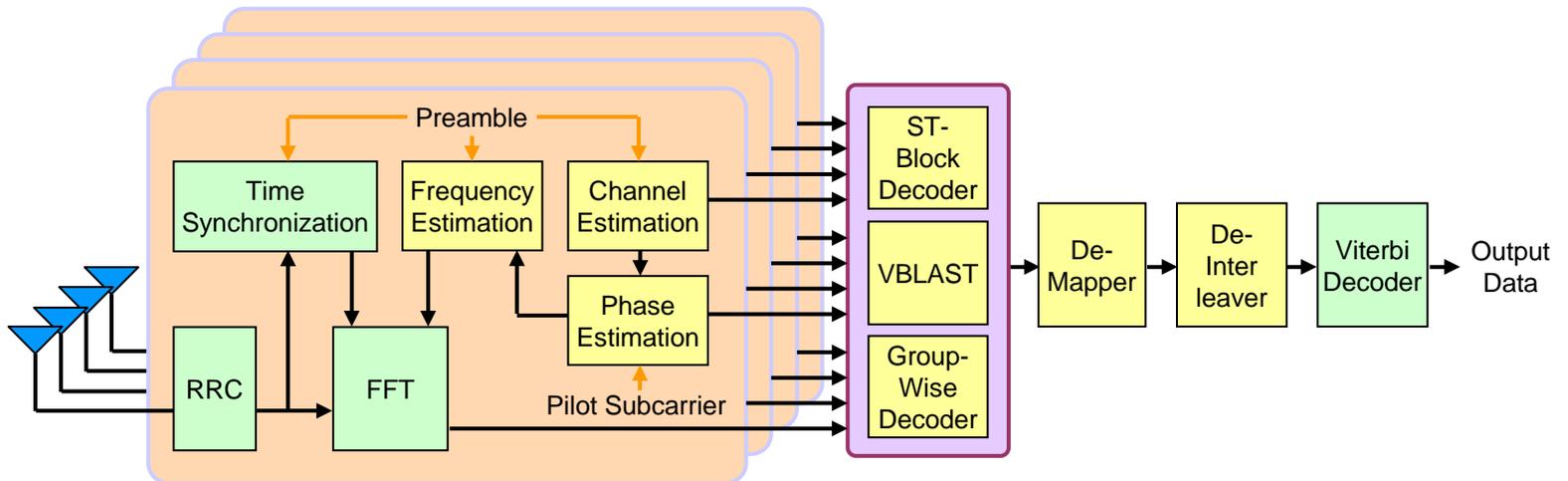


# 5 GHz MIMO-OFDM Transceiver Architecture

- Transmitter



- Receiver



# Functionality Description of MIMO-OFDM Transceiver (1)

- **Transmitter**
  - **Channel Encoder** : Using the convolution code for error correction
  - **Interleaver** : The transmitted information is better resistant to the channel distortion by distributing the same coded bits into different positions in the packet
  - A MIMO system is typically designed to meet two different, yet opposite, targets:
    - High spectral efficiency (**Spatial Multiplexing**) : **VBLAST**
    - Reliable transmission (**Spatial Diversity**) : **Space-time block codes (STBC)**
  - **Preamble** : The preamble channels, coded by the rule of STBC, will be attached in front of the data channel modulated by IFFT

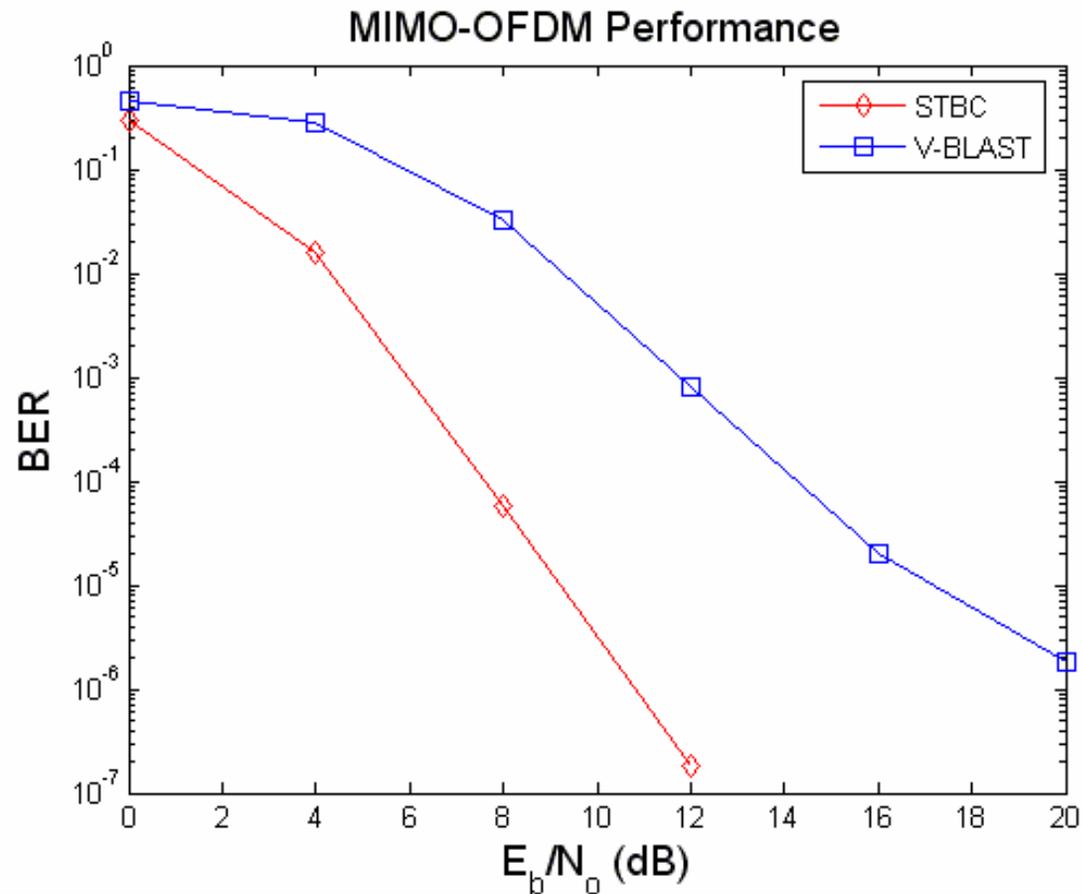
# Functionality Description of MIMO-OFDM Transceiver (2)

- **Receiver**
  - **Time Synchronization** : To find out where the symbol boundaries are and what the optimal timing instants are to minimize the effects of inter-symbol-interference (ISI) and inter-carrier-interference (ICI)
  - **Frequency Estimation** : To correct the frequency offset, which is caused by the difference of oscillator frequencies at the transmitter and the receiver
  - **Channel Estimation** : Owing to the same symbol structure as data symbols, long preamble becomes the best candidate for performing this job
  - **Phase Estimation** : To correct the frequency offset that varies during the reception of the packet
  - **Space-Time Block Decoder** : Decode the data with diversity gain
  - **VBLAST Decoder** : Decode the data with multiplexing gain

# Parameters of MIMO-OFDM Transceiver

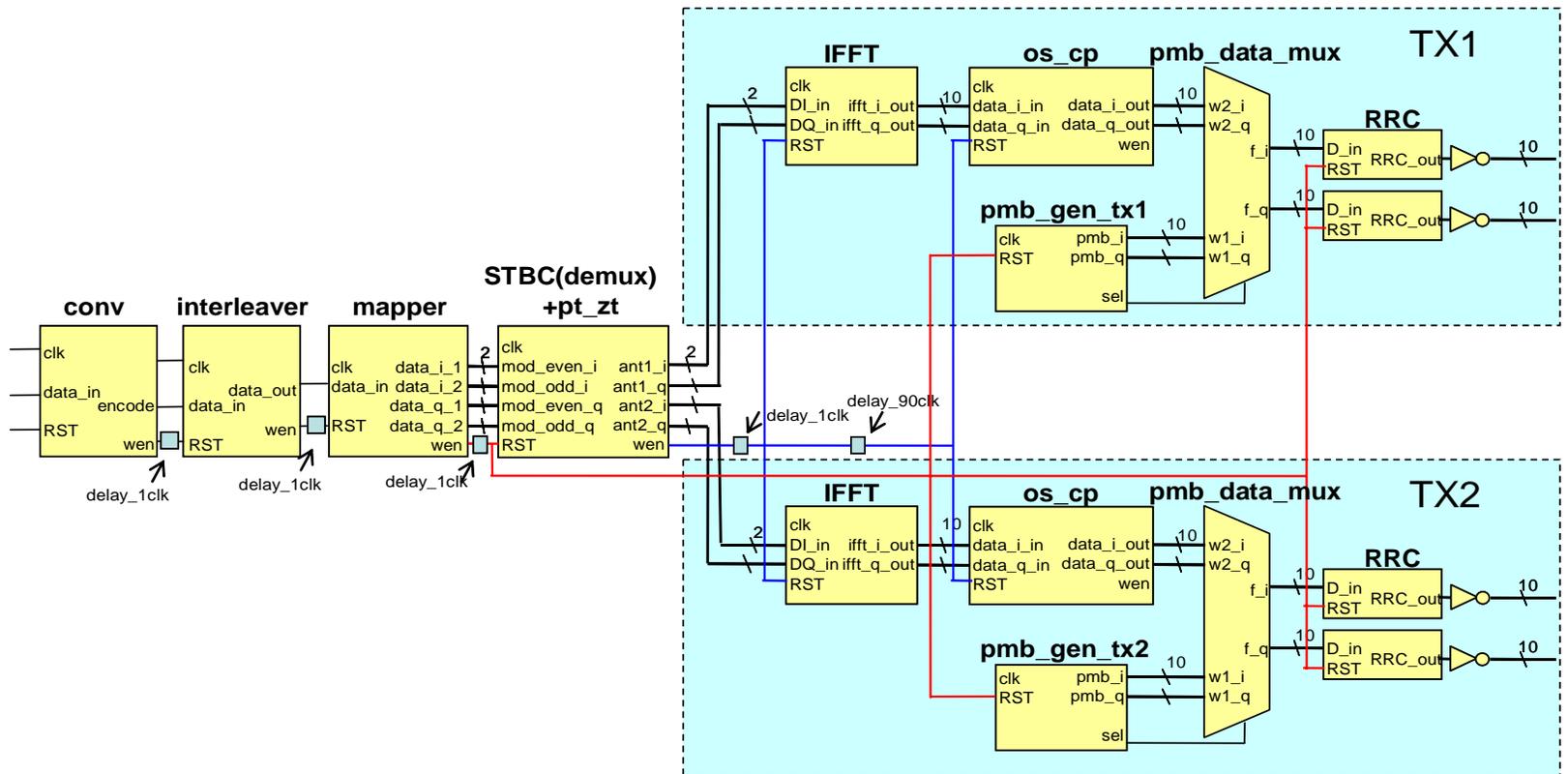
Number of Transmit Antennas	2
Number of Receive Antennas	2
Number of Long Preambles / Packet	2
Number of Short Preambles / Packet	10
Number of OFDM Symbols / Packet	6
Number of Data Tones / Symbol	48
Number of Zero Tones / Symbol	12
Number of Pilot Tones / Symbol	4
FFT Size	64 {-32:31}
Long Preamble Size	64+16 (CP)
Short Preamble Size	16
Locations of Data Tones	{-26:-22, -20:-8, -6:-1, 1:6, 8:20, 22:26}
Locations of Zero Tones	{-32:-27, 0, 27:31}
Locations of Pilot Tones	{-21, -7, 7, 21}

# Performance of MIMO-OFDM Receiver



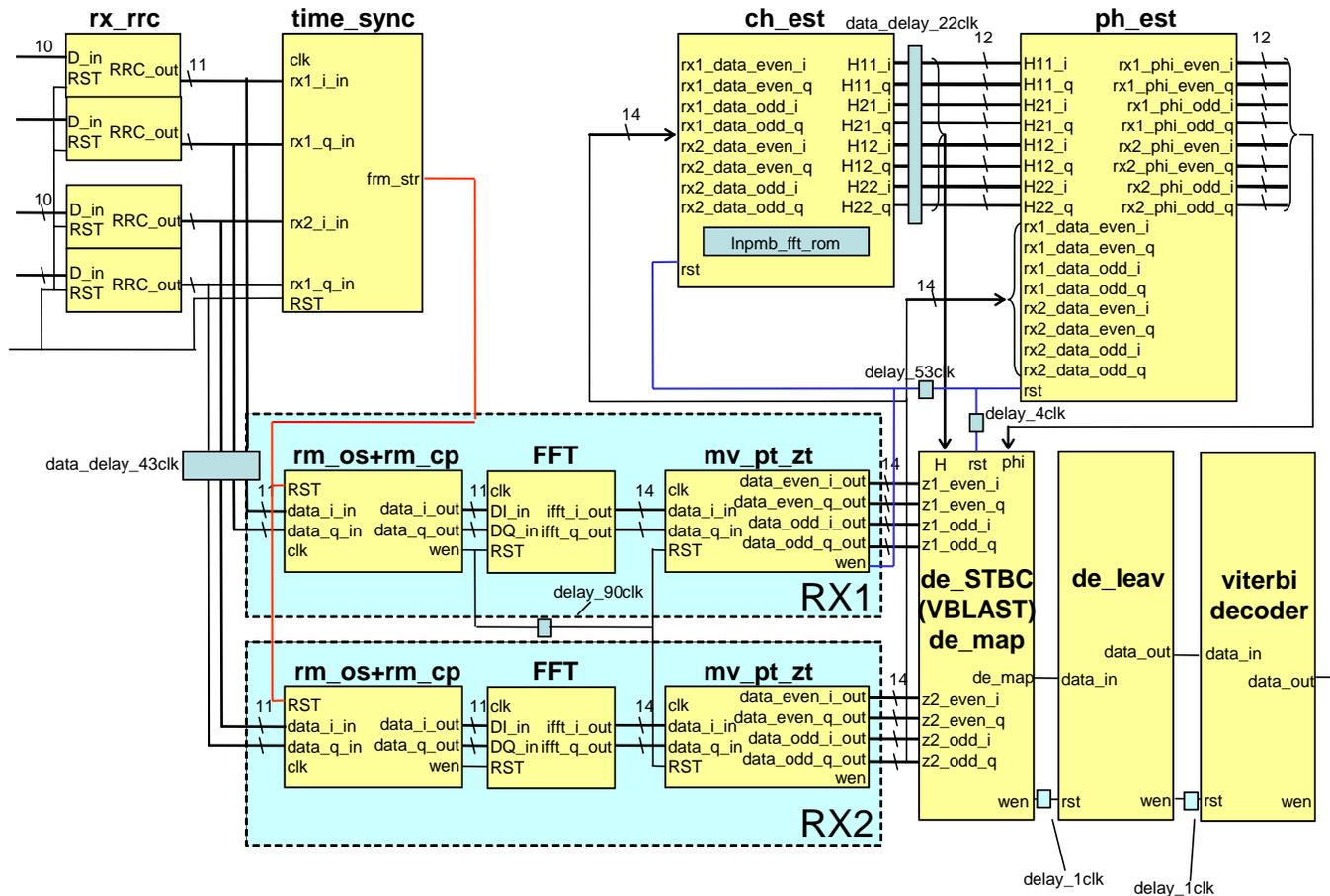
# 5-GHz MIMO-OFDM Baseband HW Architecture (1)

- Transmitter



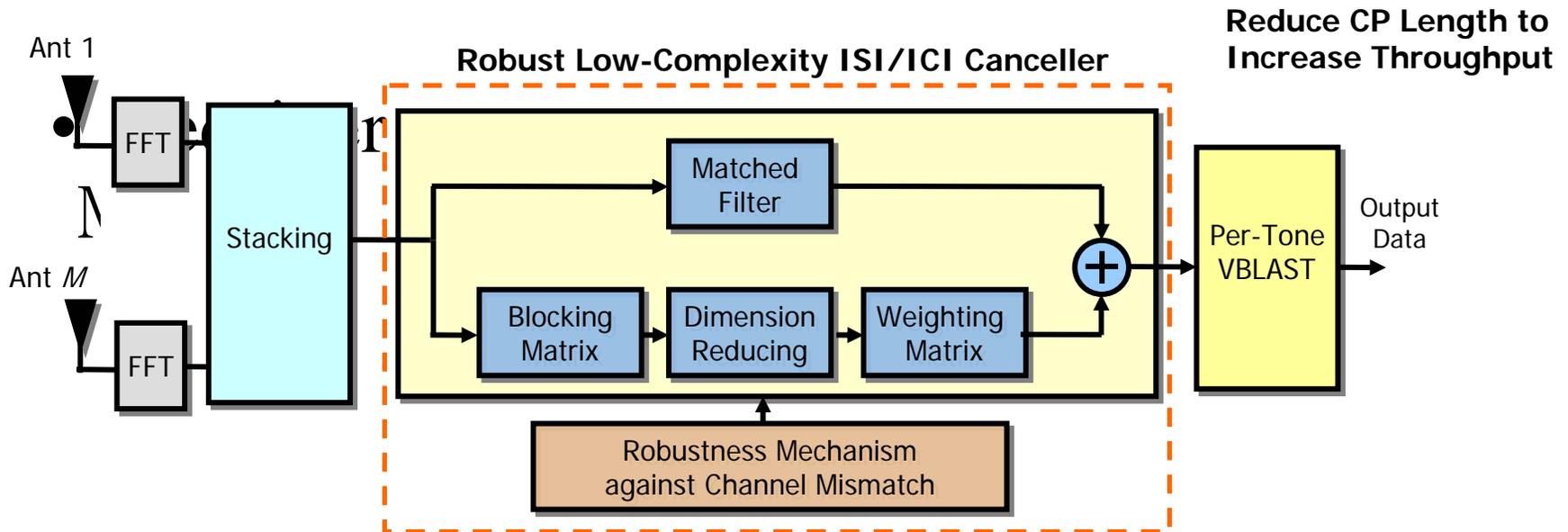
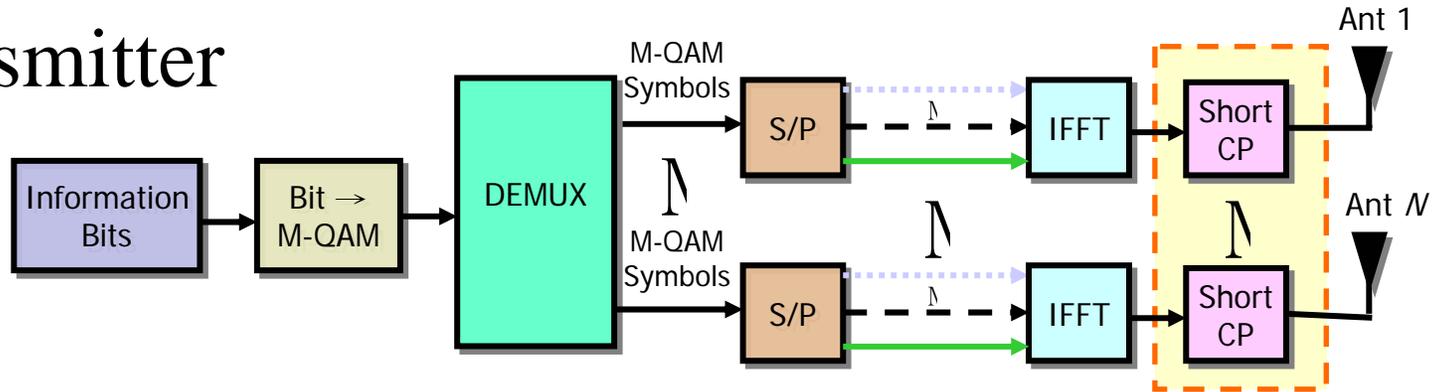
# 5-GHz MIMO-OFDM Baseband HW Architecture (2)

- Receiver



# High Throughput MIMO-OFDM Technique

- Transmitter

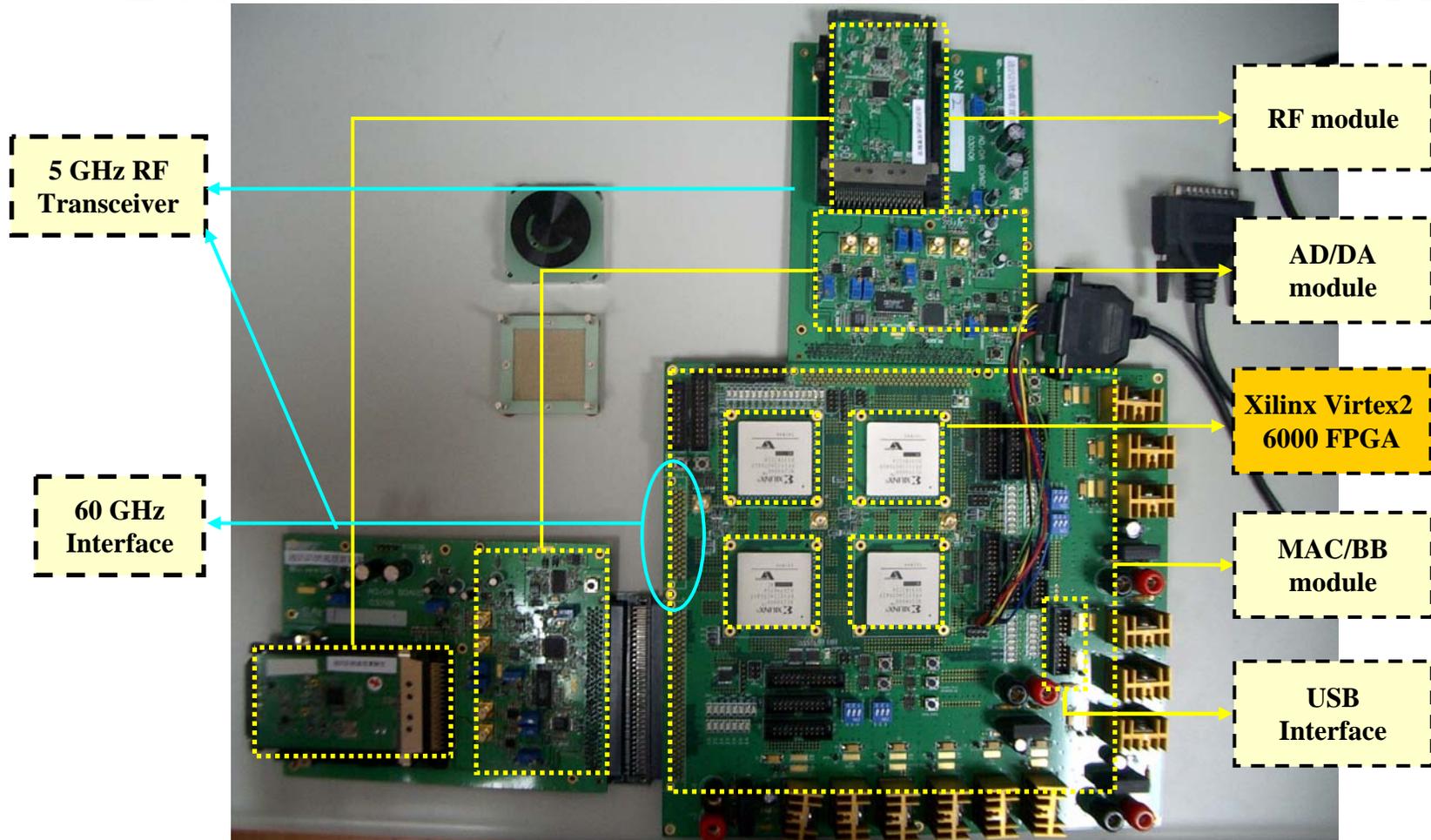


# Functionality Description of High Throughput MIMO-OFDM

- The transmitter is performed in a similar way as it is in MIMO-OFDM system, except that the **CP length is shortened to increase throughput**
- Therefore, ISI and ICI are enhanced such that interference cancellation mechanism is required
- Robust Low-Complexity ISI/ICI Canceller
  - **Matched Filter**: To match the received signal
  - **Blocking Matrix**: To separate the interference part from the received signal
  - **Dimension Reducing & Weighting Matrix**: An adaptive estimation of the combination of ISI and ICI
  - **Robust Mechanism against Channel Mismatch**: A mechanism that guarantees the performance of interference cancellation when channel mismatch is present

# Complete Hardware Platform

- Baseband transceiver consists of four FPGAs



# Description of HW Platform (1)

- **Modules at the platform**
  - **RF Module (MAX 2828)**
    - Specifically designed for single-band IEEE 802.11a applications covering world-band frequencies of 4.9 GHz to 5.875 GHz
  - **AD/DA Module (ADS2807 and DAC2900)**
    - ADS2807 is an analog to digital converter which provides a high bandwidth track-and-hold and gives excellent spurious performance up to and beyond the Nyquist rate.
    - DAC2900 is a digital to analog converter which offers exceptional dynamic performance, and enables to generate very-high output frequencies suitable for “Direct IF” applications

## Description of HW Platform (2)

### – MAC/BB module (FPGA-based)

- Composed of four Xilinx Virtex-II 6000 modules, giving significant improvement in processing speed, size, weight, power, and costs compared to DSP solutions
- Both 5 GHz MIMO-OFDM and 60 GHz SC baseband transceivers are implemented on this module

### – USB Interface module

- USB interface was designed into the platform to provide a convenient input for audio/video signals

# Summary

- ❑ Presented the 60/5 Dual-Mode Broadband and Wireless Network (DMBWN) as a backward compatible system
- ❑ Future works will be devoted to realize the 60 GHz transceiver, and switched beamforming smart antenna, which can be integrated with the developed 5 GHz system.
- ❑ Academically, we will continuously make efforts to develop advanced signal processing algorithms, such as cross-layer signaling, channel estimation and interference cancellation methods, for the proposed dual-band WLAN system.

# Next Step Towards Down Selection

- **A Formal Joint Submission** would be made in **July Meeting in San Francisco**
- **National Taiwan University/ TEEMA** (Taiwan Electrical & Electronic Manufacturers' Association) **has agreed to create a joint submission with COMPA**

**Thank you!**