Project: IEEE P802.15 Working Group for Wireless Personal Area Networks

Submission Title: [An Innovative High Speed Modem Implementation]
Date Submitted: [May 6,2007]
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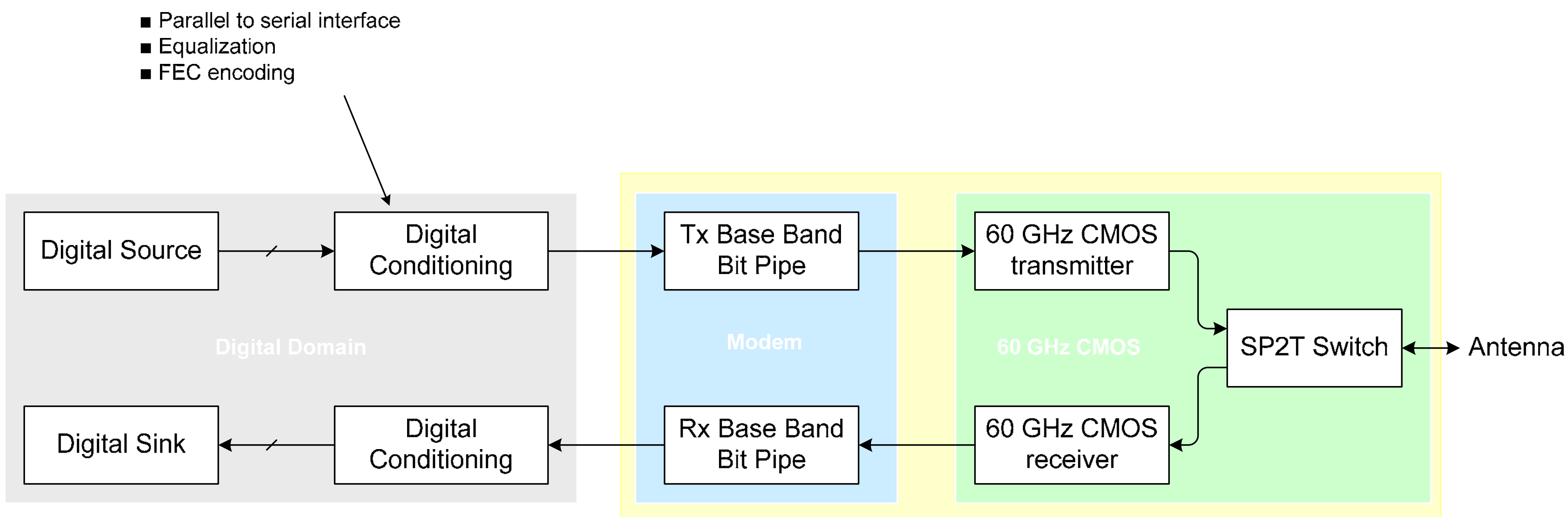
Abstract: [NewLANS proposal]

Purpose: [Contribution to 802.15 TG3c interim in Montreal, Canada]

Scope of Proposal

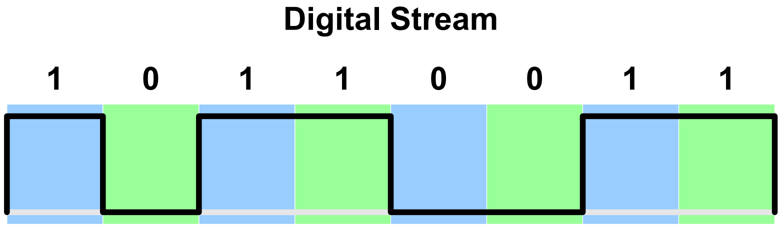
- **Focus on the modem**
- **Objective to work with companies with core competence in 60 GHz MMIC and antenna for an integrated solution**

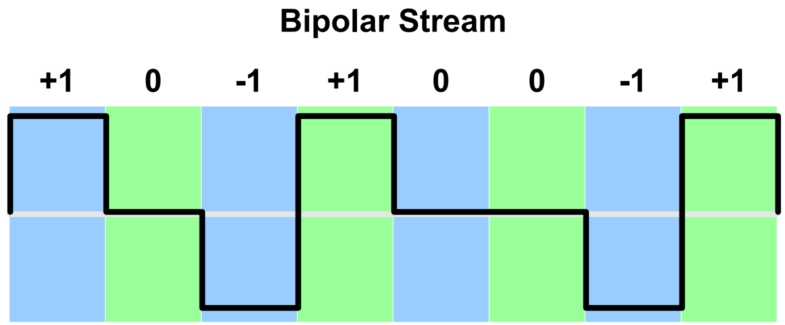


Bipolar Coding Features
Summary

- A synchronous clock encoding technique in PAM transmission
- Three level system
  - Logical 0 is represented by no symbol
  - Logical 1 by pulses of alternating polarity
- Inherent limited error detecting capability
- Zero spectral density at 0 and 1/(2.Baud Period)
- No DC component

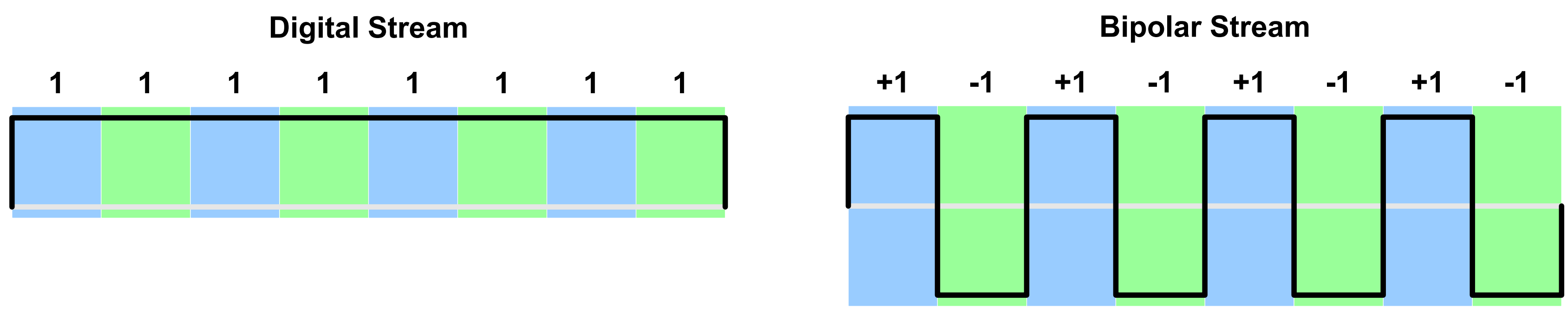
Three Level System
Bipolar Coding





- **Logical 1s represented by alternating polarity**
- **Logical 0 represented by no symbol**

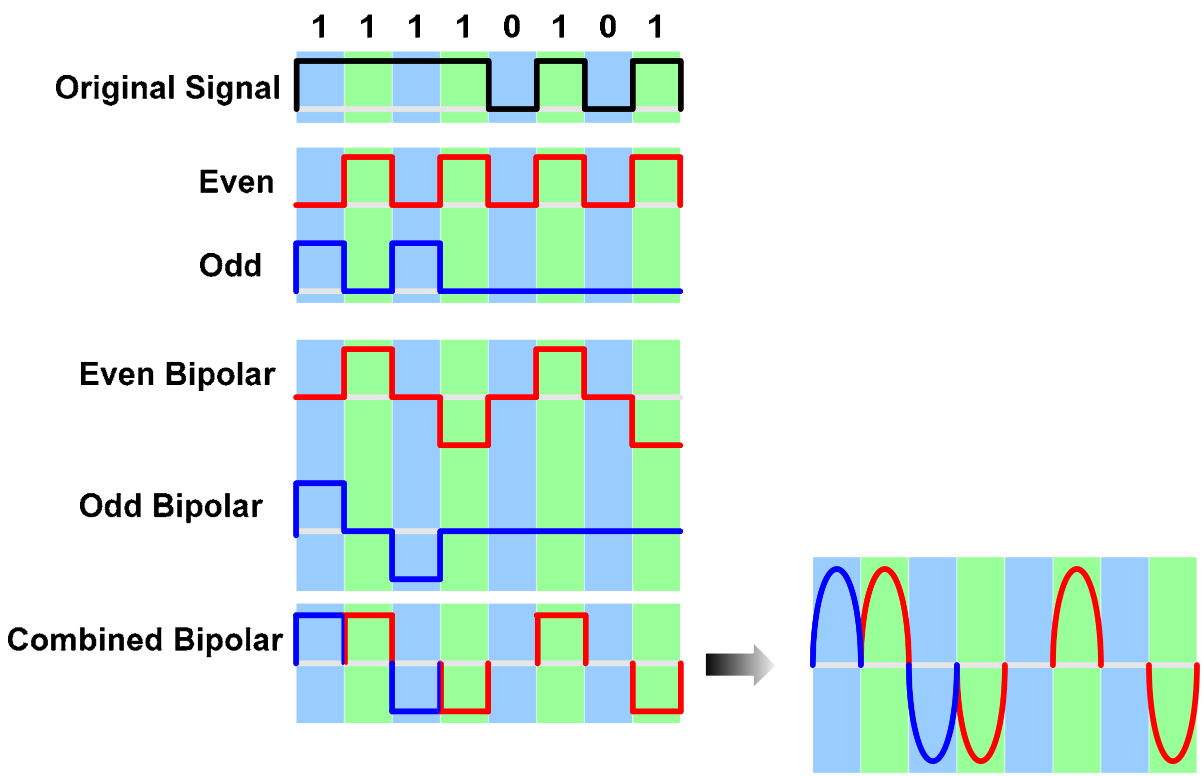
Error Detection
Bipolar Coding



Bipolar Violation

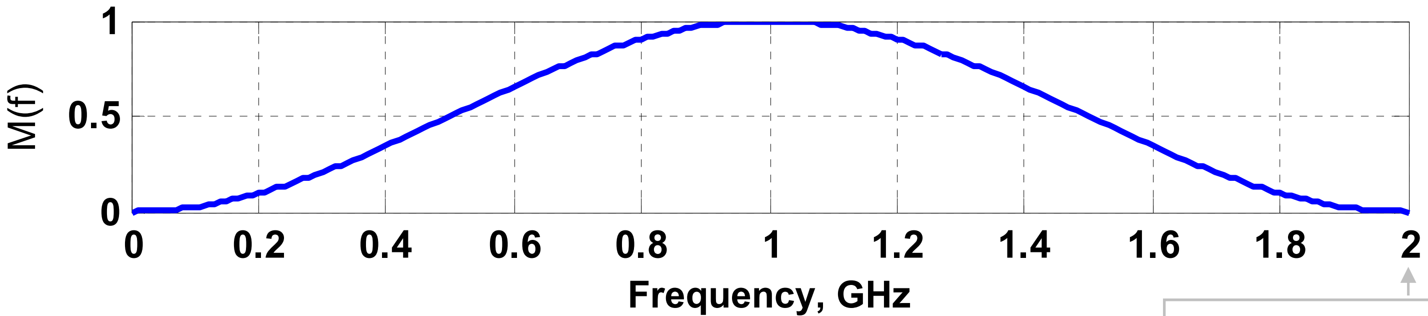
Consecutive pulses cannot have the same polarity

Bipolar Coding With Dual Rail



Scope Capture

Power Density Profile
Bipolar Coding With Dual Rail



1/(2.Baud Period) = 1/(2T)
T = 0.25 ns

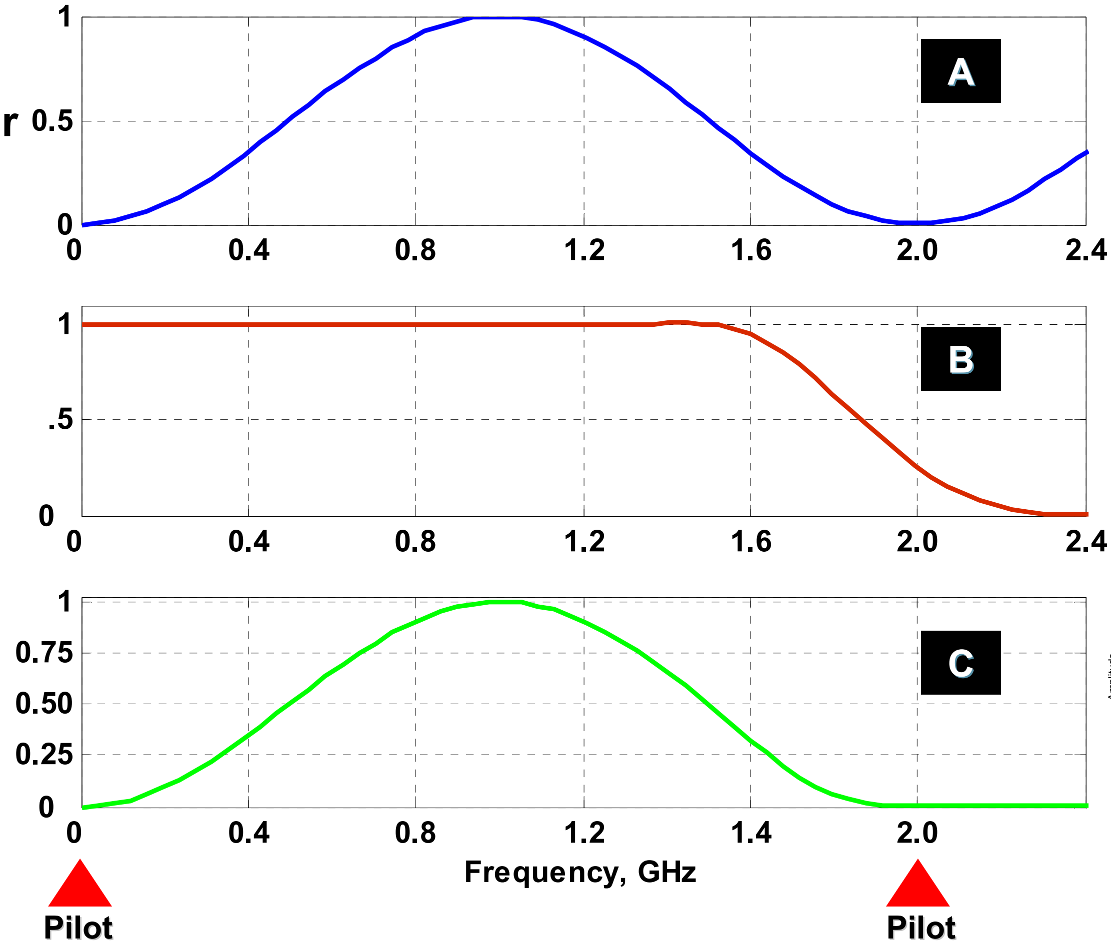
- Zero spectral density at 0 and 1/(2T)
- No DC component

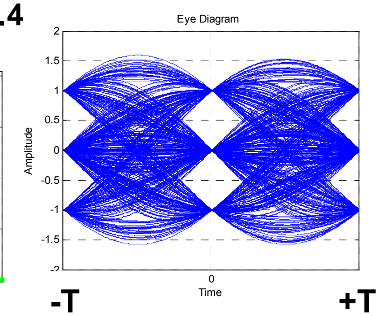
Pulse Shape

Dual Rail Bipolar

Square root raised cosine filter

A * B =



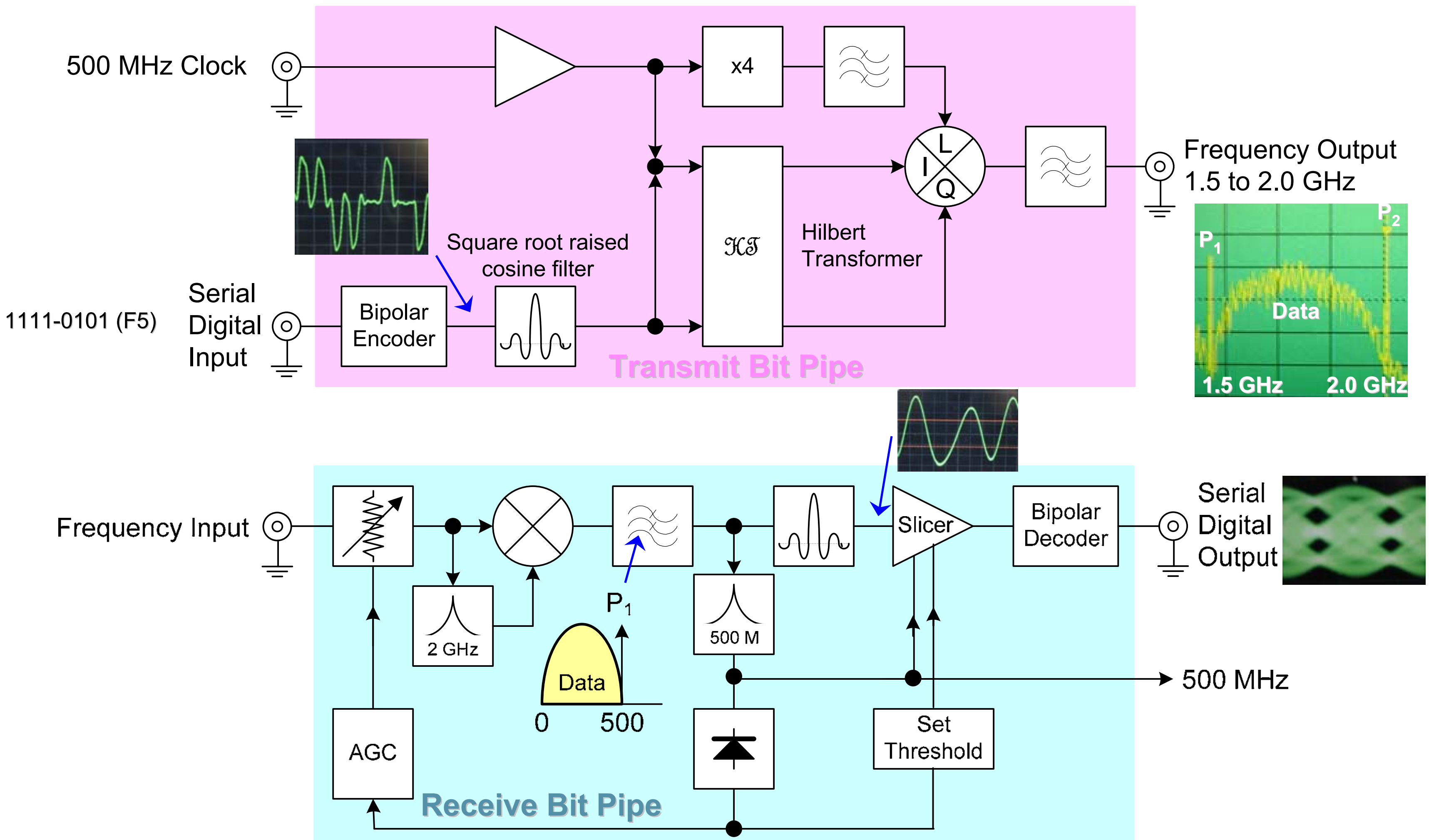


T= 0.25 ns

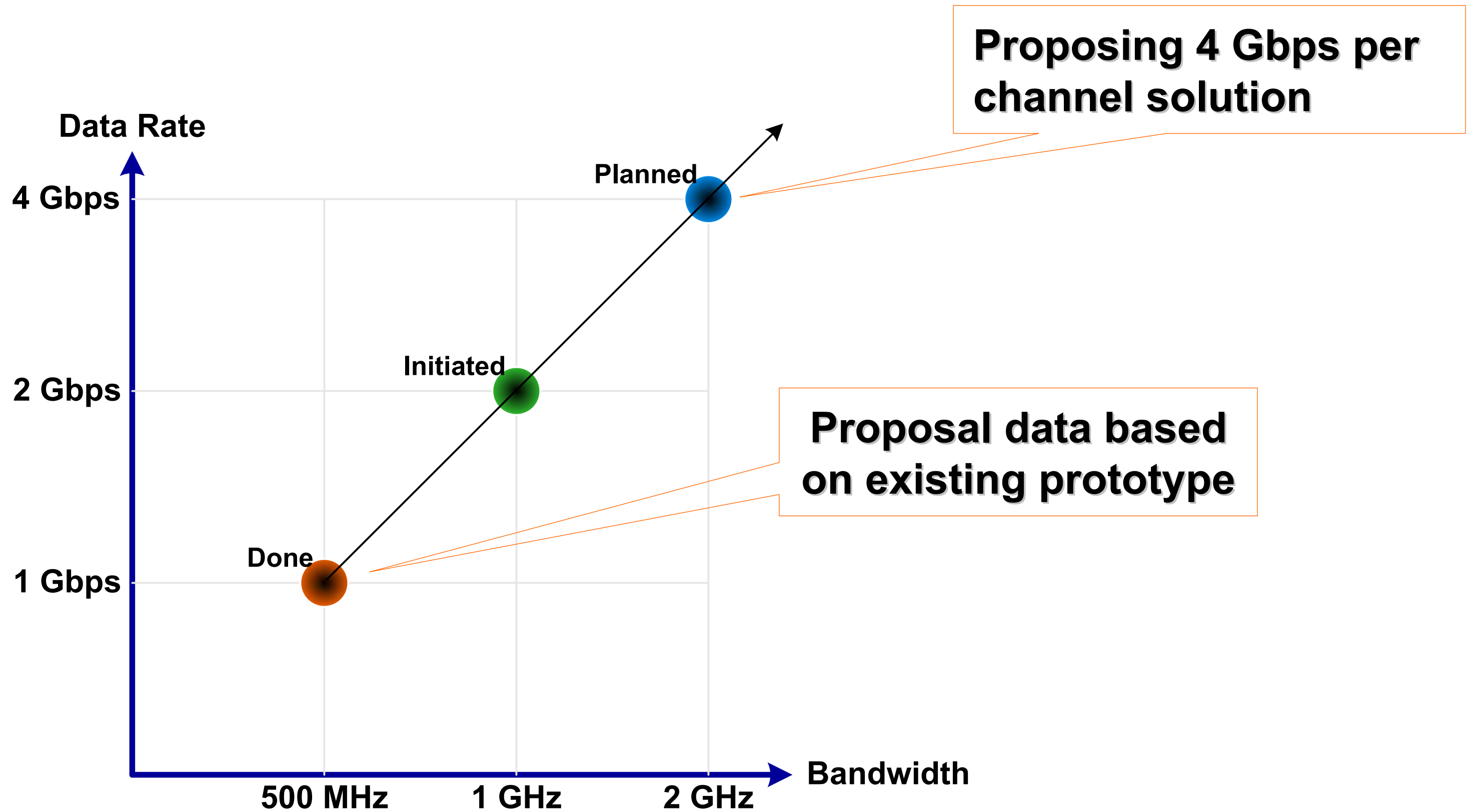
Pilot Tones

- Inserted at 0 and 1/(2T), points of zero power density
  - Minimum effect on peak-to-average-power ratio
- Clock always coherent with data signal
- Features offered
  - Relatively immune to phase noise and frequency errors at 60 GHz
  - Fast data recovery (~100 ns) by virtue of no Costas loop
  - Fast AGC (40 dB dynamic range, 1% of actual value in ~10 μs)

Functional Block Diagram
Existing Prototype (500 MHz, 1 Gbps)



Prototype Schedule



Note

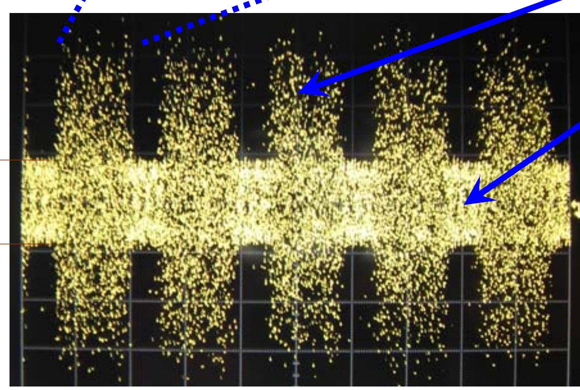
- **Spectral efficiency of 2 bps/Hz**
- **Prototype built on off-the-shelf components**

Transmitted Waveform
Frequency Domain and Time Domain

Frequency Domain

20 dB

Time Domain

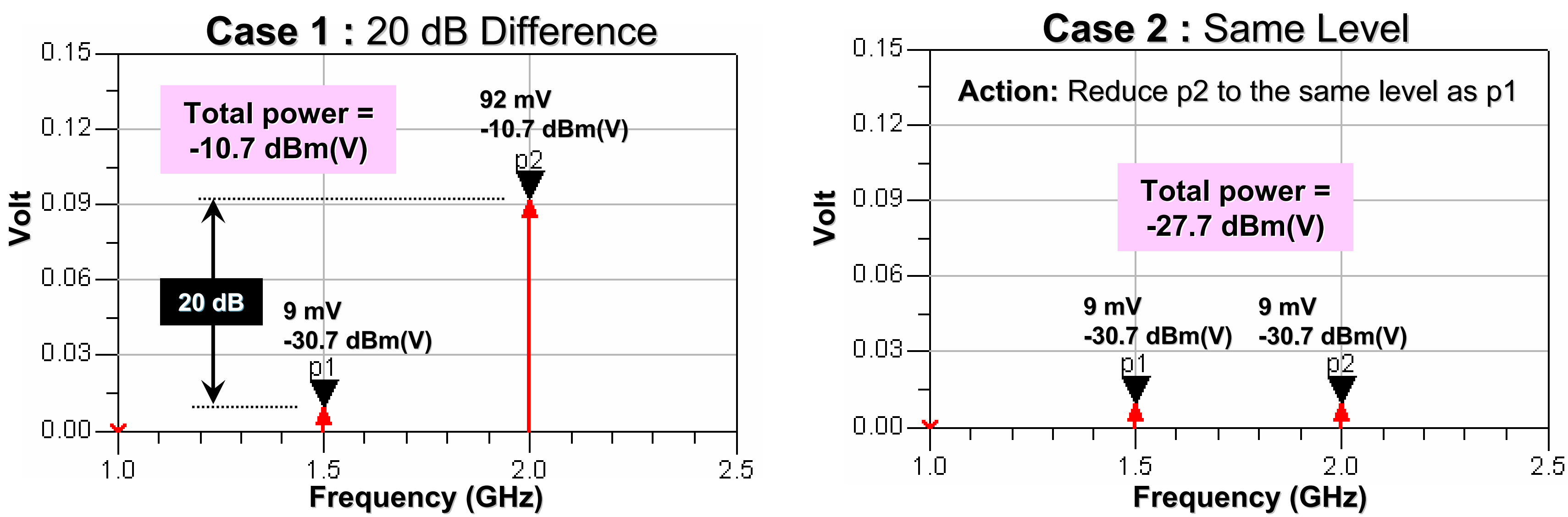


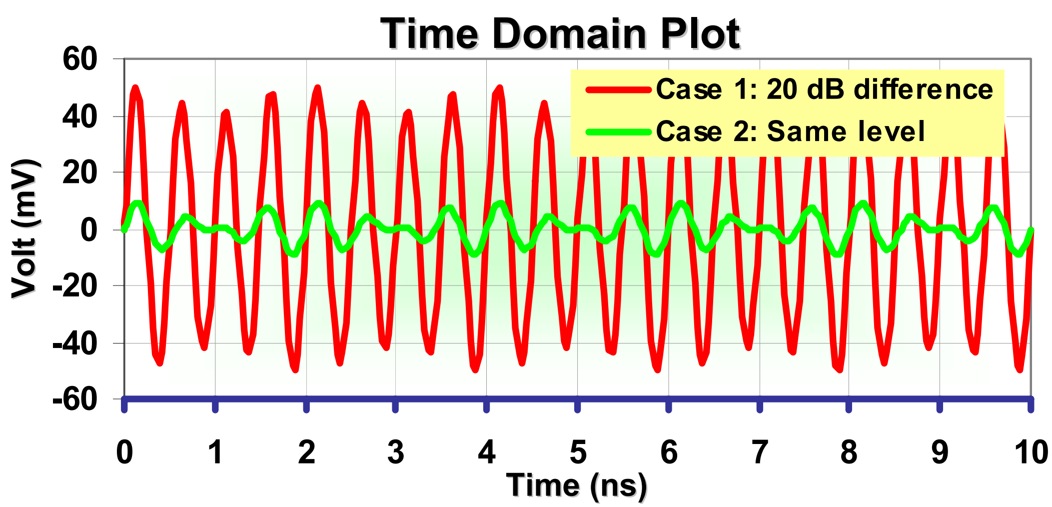
A

Data and pilots

No data, only pilots
- 99% (90%) of power (voltage) is contributed by 2 GHz pilot
- Question - how can 'A' be reduced?

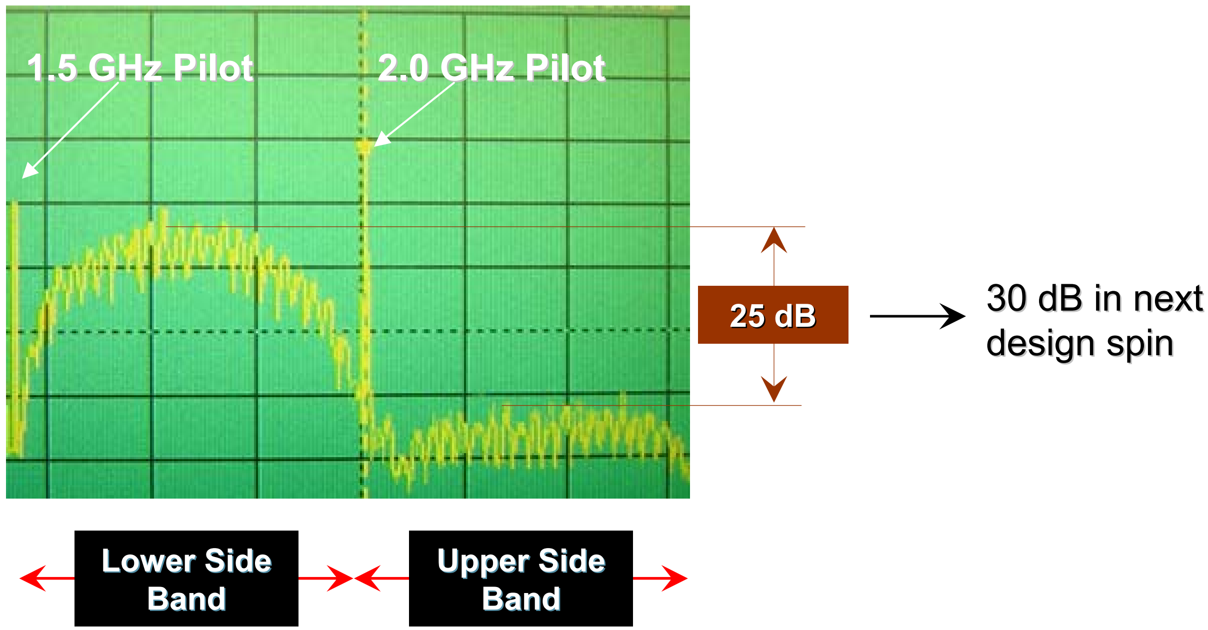
Change in Pilot Level





Drops from 100 mV_{P-P} to 18 mV_{P-P}

Transmitted Waveform
Rejection of Upper Sideband



Note

- Waveform at the output of Tx base band bit pipe
- Lower side band block upconverted to 60 GHz
- Existing 60 GHz millimeter wave transceiver based on GaAs devices

Decoding

- *Partial response maximum likelihood* decoding
- Proven technology – used in disk drives
- Existing prototype
  - Partial response implemented
  - Maximum likelihood not implemented in current design (500 MHz, 1 Gbps) – will implement in next design spin (1 GHz, 2 Gbps)
- Maximum likelihood provides SNR gain of 2 dB
- All implementation in analog domain

Modem Features

- Design that focuses on low cost, high speed and low power
- Flexible architecture – any digital input, with or without coding
- Spectral efficiency of 2 bps/Hz at 25% roll off
- Performance comparable to 2-level PAM
- No DACs or DSPs
- Low power, low latency
- Can operate at 1 dB compression point
- Relatively immune to phase noise and frequency errors at 60 GHz
- Fast data recovery (~100 ns)
- Fast AGC (40 dB dynamic range, 1% of actual value in ~10 μs)
- Fixed data rate and modulation – translates to simplicity
- Up to 12 Gbps

Due to pilot tones

Migration Path

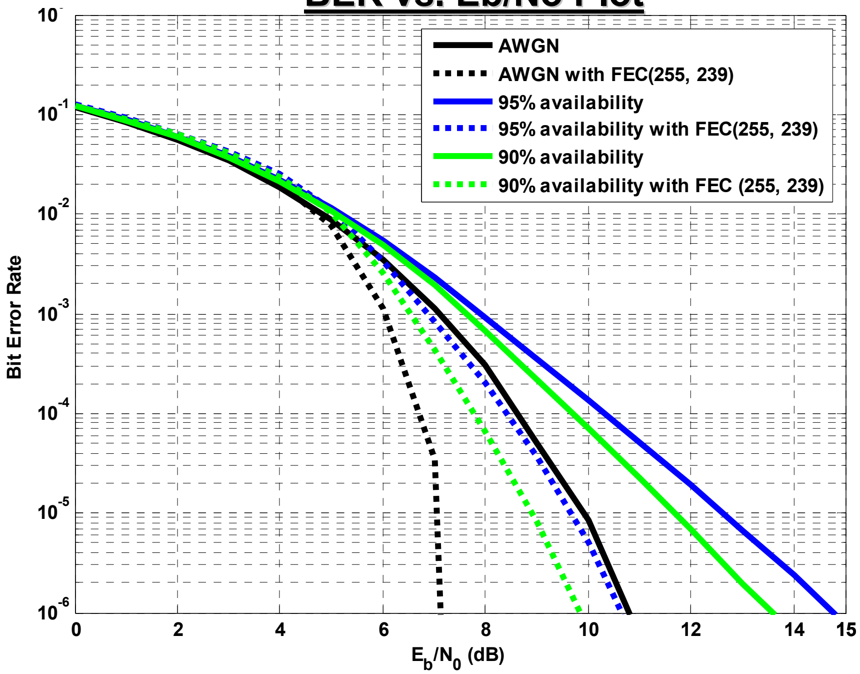
- Current design supports all applications in the usage model and beyond
  - 4 Gbps [2 GHz/channel] will meet most immediate applications
  - [2 GHz/channel] . [3 channels] . [2 bps/Hz] = 12 Gbps
- Two techniques to increase data rate
  - Channel bonding
    - Low power consumption, low complexity
    - Margin drops by 3 dB per channel bonding
  - Base band stacking
    - Maintains margin
    - Power consumption doubles, adds complexity

Channel Model Environments

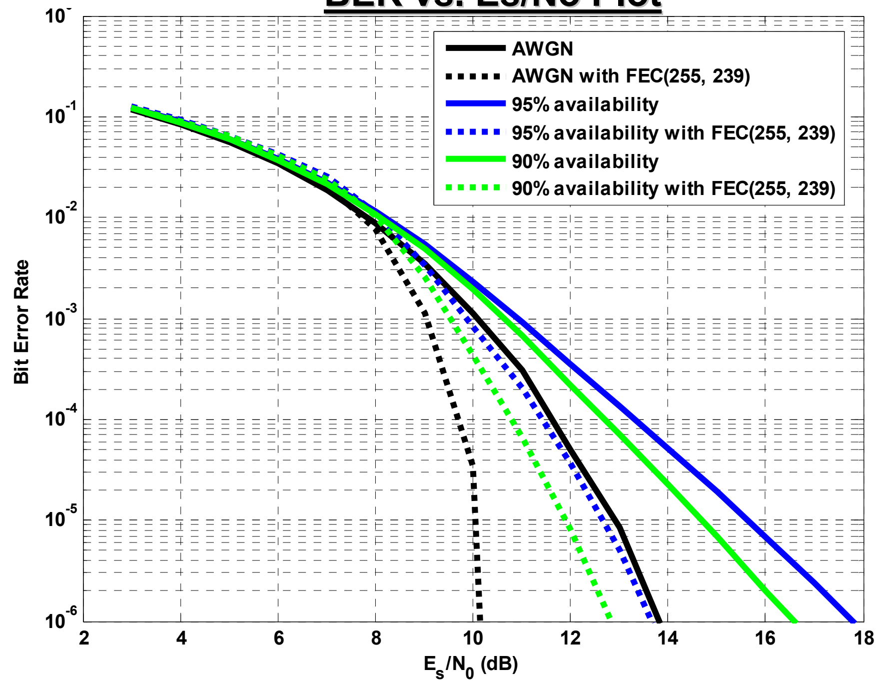
#	Environment	Tx	Rx	Measurement & Analysis	Comments
CM1.2	Residential, LOS	60°	15°	NICT	Simulation based on 30° Rx
CM1.3	Residential, LOS	30°	15°	NICT	▪ Simulation based on 30° Rx ▪ AWGN channel

BER Plot
CM1.2, Tx 30° ► Rx 30°

BER vs. Eb/No Plot



BER vs. Es/No Plot



- **Linear polarization**
- **No equalization**
- **BER 10^{-6} (without FEC)**
  - Eb/No of 11 dB for AWGN
  - Eb/No of 15 dB for 95% availability

Comment

Performance can be improved by about 2 dB by considering circular polarization for LOS applications

Link Analysis
Portable Applications [3 m, 4 Gbps]

AWGN

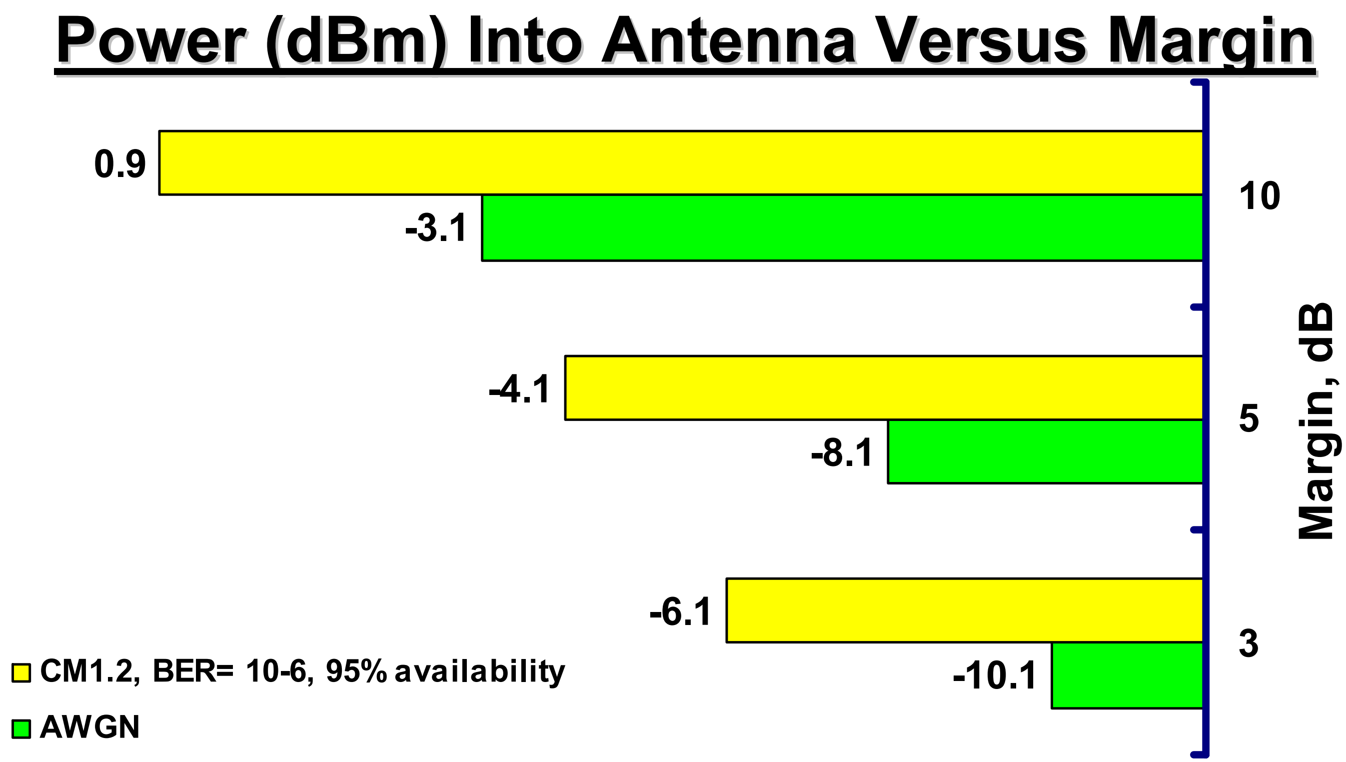
Power in antenna (at 1 dB CP)	-3.1 dBm
Tx antenna gain [30º]	14.9 dBi
Radiated power	11.8 dBm
Free space loss at 3.0 m	77.6 dB
Gaseous attenuation	0.0 dB
Miscellaneous loss	0.0 dB
Attenuation	77.7 dB
Rx antenna gain [30º]	14.9 dBi
Effective power into receiver	-51.0 dBm
KTB [2000 MHz, 290 K]	-81.0 dBm
Receiver noise figure	8.0 dB
Eb/No [BER 10-6]	11.0 dB
FEC gain	0.0 dB
Jitter	1.0 dB
Receiver sensitivity	-61.0 dBm
Margin	10.0 dB

CM1.2 Environment

Power in antenna (at 1 dB CP)	0.9 dBm
Tx antenna gain [30º]	14.9 dBi
Radiated power	15.8 dBm
Free space loss at 3.0 m	77.6 dB
Gaseous attenuation	0.0 dB
Miscellaneous loss	0.0 dB
Attenuation	77.7 dB
Rx antenna gain [30º]	14.9 dBi
Effective power into receiver	-47.0 dBm
KTB [2000 MHz, 290 K]	-81.0 dBm
Receiver noise figure	8.0 dB
Eb/No [BER 10-6, 95% availability]	15.0 dB
FEC gain	0.0 dB
Jitter	1.0 dB
Receiver sensitivity	-57.0 dBm
Margin	10.0 dB

Note: No FEC or equalization

Link Analysis
Portable Applications [3 m, 4 Gbps]



Note

- Refer to the previous slide for details on receiver sensitivity
- Add about 2 dB for insertion loss in SP2T switch to determine power out of 60 GHz amplifier

Link Analysis
Fixed Application [10 m, 4 Gbps]

AWGN

Power in antenna (at 1 dB CP)	10.0 dBm
Tx antenna gain [30º]	14.9 dBi
Radiated power	24.9 dBm
Free space loss at 10.0 m	88.1 dB
Gaseous attenuation	0.2 dB
Miscellaneous loss	0.0 dB
Attenuation	88.2 dB
Rx antenna gain [30º]	14.9 dBi
Effective power into receiver	-48.4 dBm
KTB [2000 MHz, 290 K]	-81.0 dBm
Receiver noise figure	8.0 dB
Eb/No [BER 10-6, 95% availability]	11.0 dB
FEC gain	0.0 dB
Jitter	1.0 dB
Receiver sensitivity	-61.0 dBm
Margin	12.5 dB

CM1.2 Environment

Power in antenna (at 1 dB CP)	10.0 dBm
Tx antenna gain [30º]	14.9 dBi
Radiated power	24.9 dBm
Free space loss at 10.0 m	88.1 dB
Gaseous attenuation	0.2 dB
Miscellaneous loss	0.0 dB
Attenuation	88.2 dB
Rx antenna gain [30º]	14.9 dBi
Effective power into receiver	-48.4 dBm
KTB [2000 MHz, 290 K]	-81.0 dBm
Receiver noise figure	8.0 dB
Eb/No [BER 10-6, 95% availability]	15.0 dB
FEC gain	0.0 dB
Jitter	1.0 dB
Receiver sensitivity	-57.0 dBm
Margin	8.5 dB

Note: No FEC or equalization

Require ≥ 20 dB margin for AGC to operate to mitigate shadowing effects

Link Analysis - Modified
Fixed [10 m, 4 Gbps]

Increased Antenna Gain

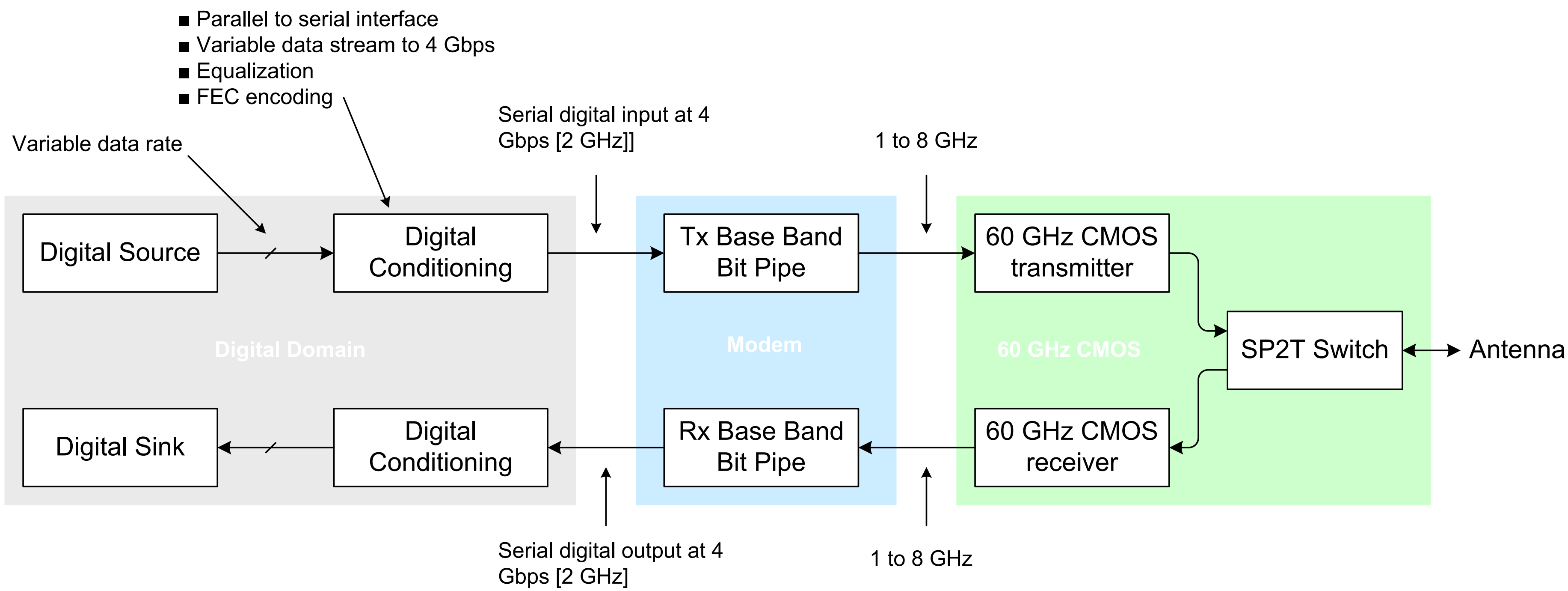
Power in antenna (at 1 dB CP)	10.0	dBm
Tx antenna gain [15º]	**21.0**	**dBi**
Radiated power	31.0	dBm
Free space loss at 10.0 m	88.1	dB
Gaseous attenuation	0.2	dB
Miscellaneous loss	0.0	dB
Attenuation	88.2	dB
Rx antenna gain [15º]	**21.0**	**dBi**
Effective power into receiver	-36.2	dBm
KTB [2000 MHz, 290 K]	-81.0	dBm
Receiver noise figure	8.0	dB
Eb/No [BER 10-6, 95% availability]	15.0	dB
FEC gain	0.0	dB
Jitter	1.0	dB
Receiver sensitivity	-57.0	dBm
Margin	20.7	dB

Increased Antenna Gain + FEC

Power in antenna (at 1 dB CP)	10.0	dBm
Tx antenna gain [15º]	**21.0**	**dBi**
Radiated power	31.0	dBm
Free space loss at 10.0 m	88.1	dB
Gaseous attenuation	0.2	dB
Miscellaneous loss	0.0	dB
Attenuation	88.2	dB
Rx antenna gain [15º]	**21.0**	**dBi**
Effective power into receiver	-36.2	dBm
KTB [2000 MHz, 290 K]	-81.0	dBm
Receiver noise figure	8.0	dB
Eb/No [BER 10-6, 95% availability]	15.0	dB
FEC gain	**4.0**	**dB**
Jitter	1.0	dB
Receiver sensitivity	-61.0	dBm
Margin	24.7	dB

Note: No equalization

Estimated Power Consumption
Block Diagram & Assumptions



Base Band Bit Pipe

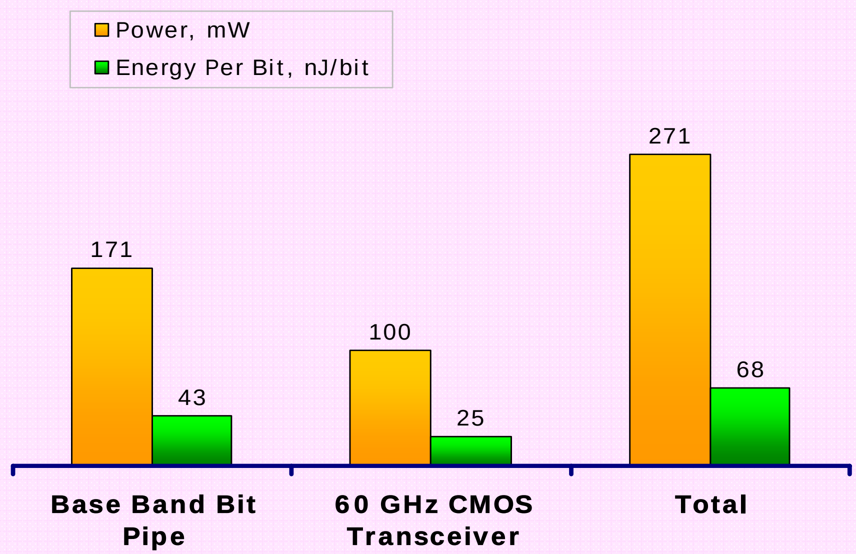
- Based on existing prototypes with off-the-self components
- No sharing of functionality between Tx and Rx band bit pipe modules
- 130 nm CMOS implementation

60 GHz CMOS

- 100 mW maximum for 60 GHz output power of 5 dBm maximum

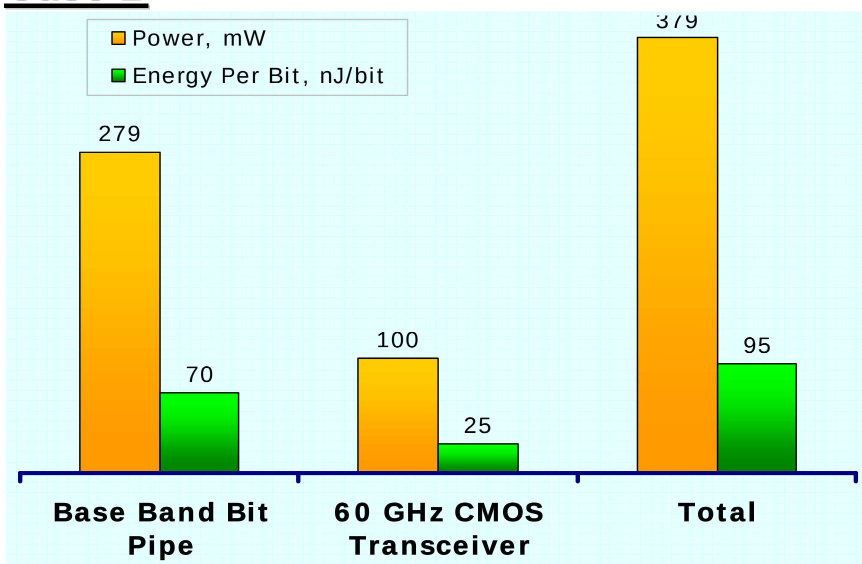
Estimated Power Consumption

Case A



- 2 Gbps/2 GHz channel – 50% duty cycle
- All active components in modulator sleeps
- Only slicer in demodulator sleeps
- 60 GHz transceiver at 100% duty cycle

Case B



- 4 Gbps/2 GHz channel – 100% duty cycle

Conclusion

- Out-of-the-box design optimized for fast clock recovery and AGC, and low power consumption
- Flexibility in design
  - Current design based on analog signal processing
  - Incorporate DACs and DSPs when they mature
- Proven hardware implementation