Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: [RF impairment models for 60GHz-band SYS/PHY simulation]
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Abstract: [This contribution describes RF impairment models for 60GHz-band SYS/PHY simulation.]

Purpose: [Contribution to mmW TG3c meeting.]

RF impairment models for 60GHz-band SYS/PHY simulation

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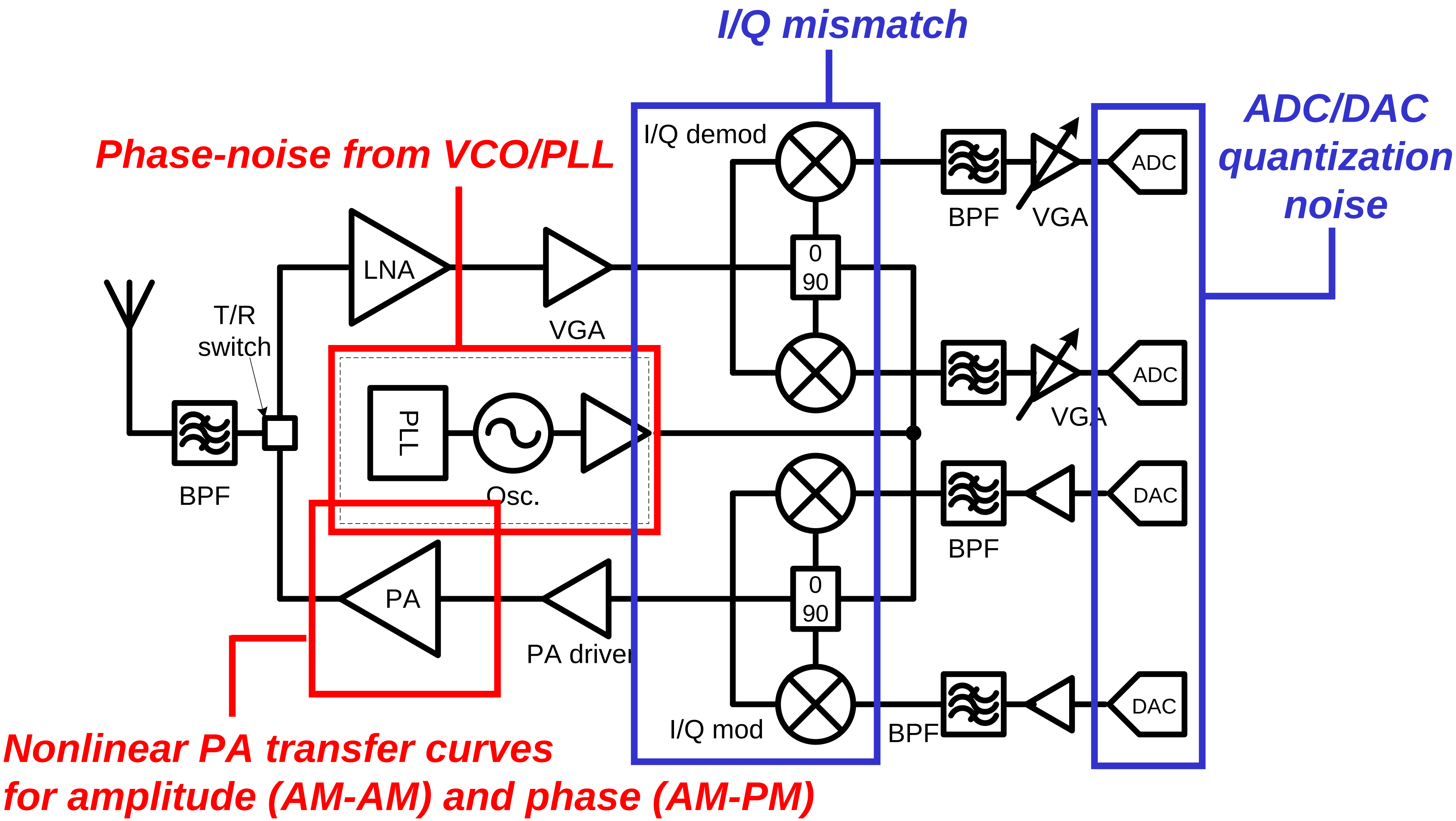
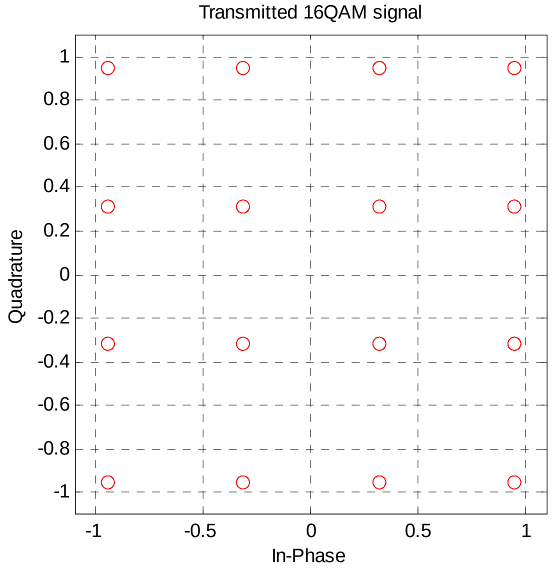
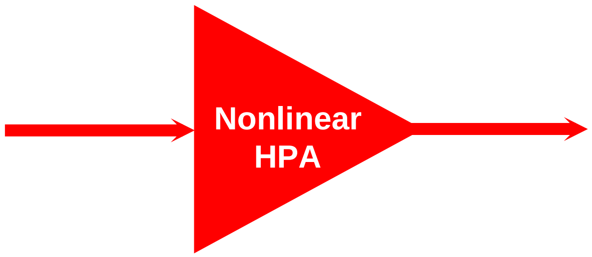
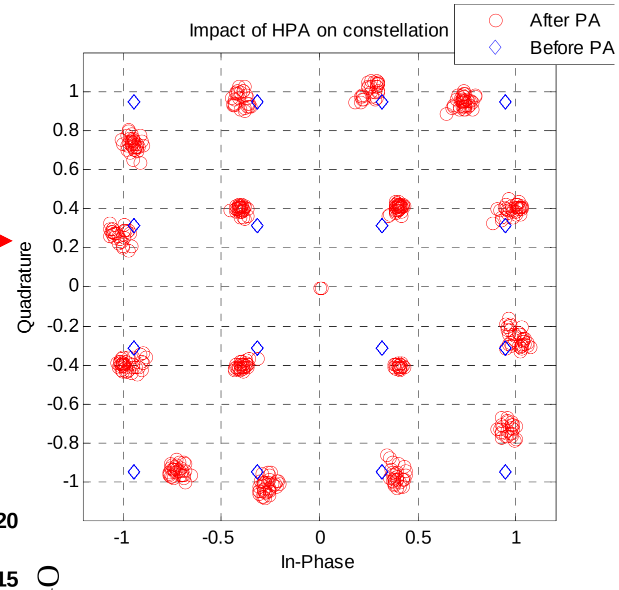
Background: RF impairments to be considered

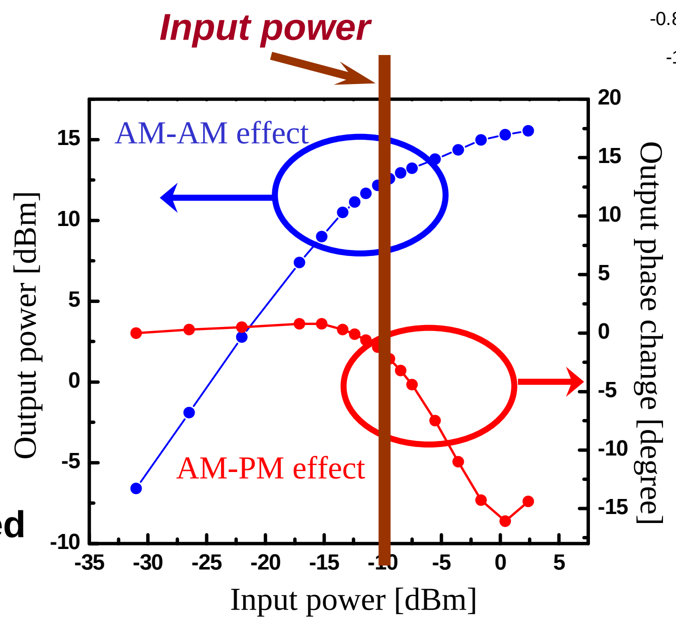


Effects of HPA nonlinearity









- HPA nonlinear relationship between output power and input power (AM-AM effect) and output phase and input power (AM-PM effect)

- Ghorbani model was suggested in Melbourne meeting

- GaAs pHEMT 60GHz power amplifier
- Refer to 15-06-0396-01-003c

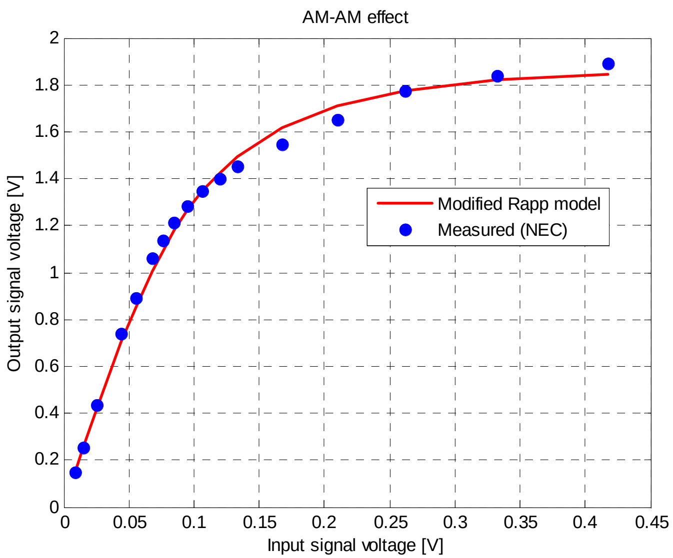
Power amplifier model for TG3c: Modified Rapp model

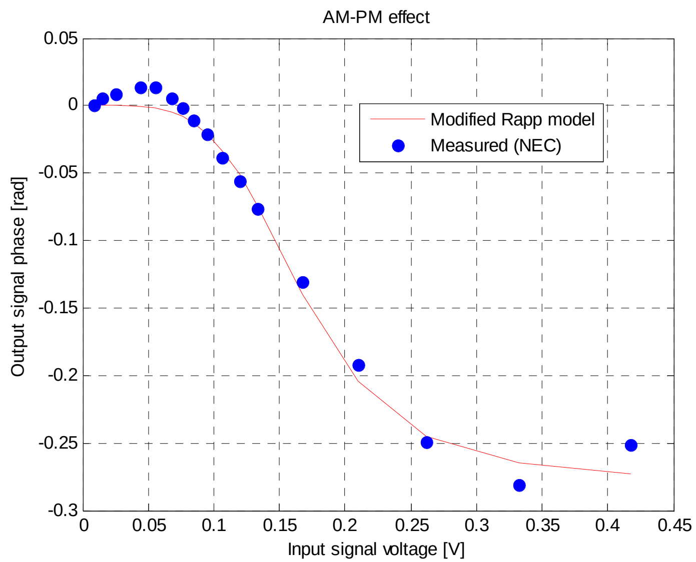
AM-AM

$$F_{AM-AM}(y) = \frac{Gx}{\left(1+\left(\frac{Gx}{V_{sat}}\right)^{2p}\right)^{\frac{1}{2p}}}$$

AM-PM

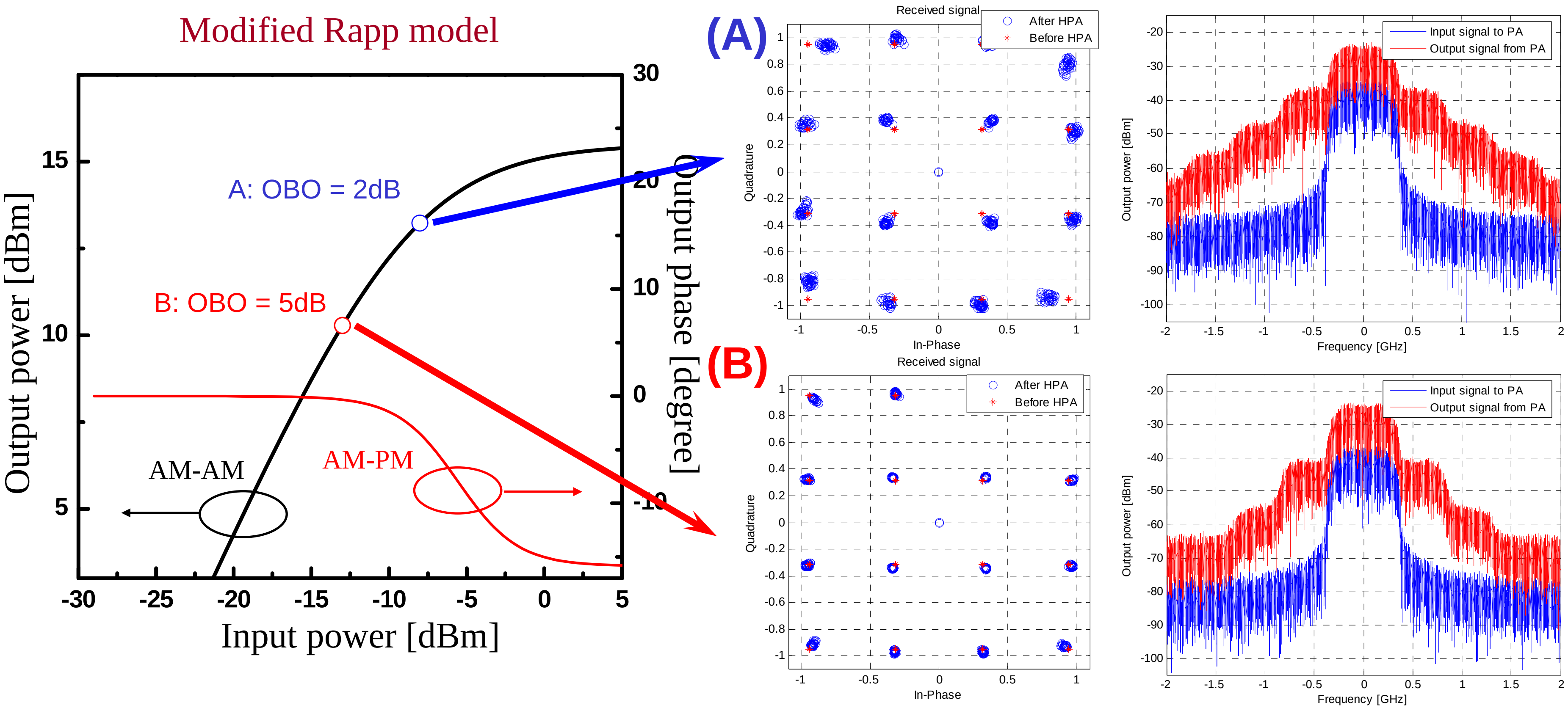
$$F_{AM-PM}(\theta) = \frac{Ax^q}{\left(1+\left(\frac{x}{B}\right)^q\right)}$$





- **Rapp model has been used for IEEE standardization (ex. 802.11a, 11n)**
- **Rapp model is convenient for setting parameters, Saturation (V_{sat}) and Gain (G)**
- **Suggested the equation to express AM-PM effect = Modified Rapp model**

What parameter should we use for PA simulation?
Output BACKOFF



- **Output backoff affects system performance and adjacent channel power ratio**
- **higher backoff, higher linearity**

Effect of output BACKOFF on BER and power efficiency

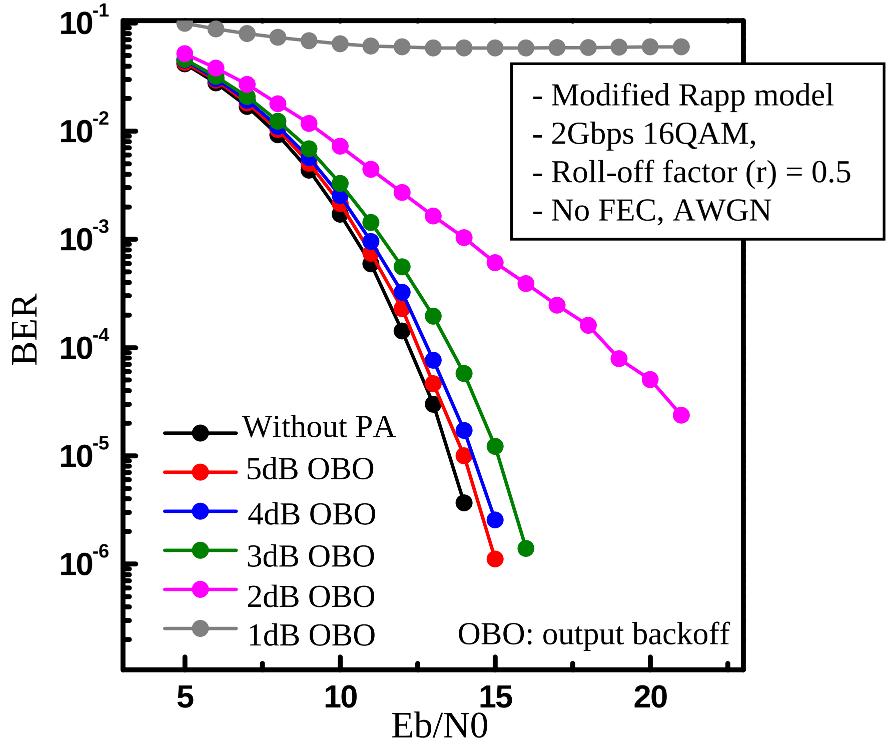


Fig.1: Impact of output backoff on 16QAM transmission

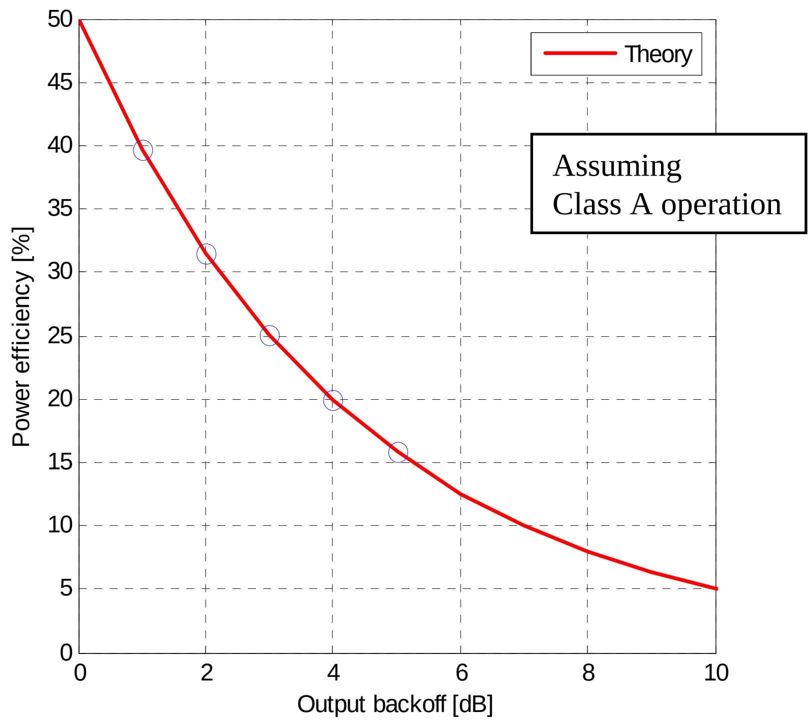
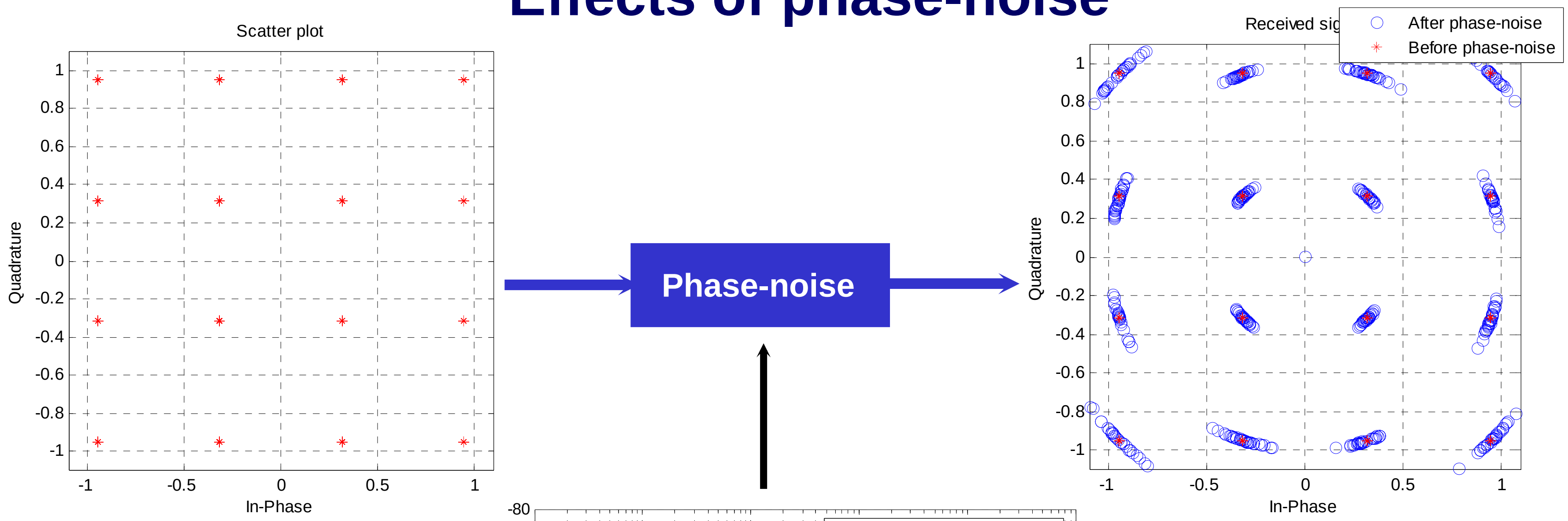
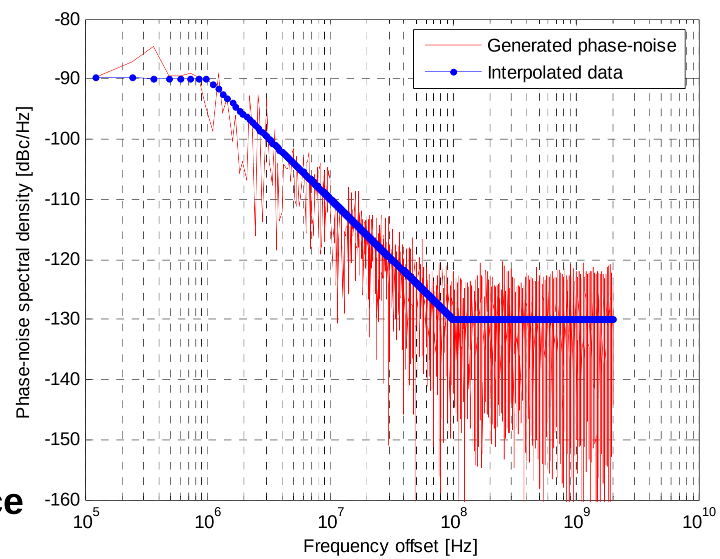


Fig.2: Power efficiency vs. output backoff

- Higher backoff, higher linearity, but lower power efficiency (trade-off)
- Backoff is critical parameter to decide power consumption and nonlinearity
- Let's use this parameter with modified Rapp model for PA simulation

Effects of phase-noise





- Interpolation data between adapted phase-noise data from reference [1] (0.13um CMOS-based 60GHz VCO)

- Assuming 1MHz PLL loop bandwidth

- **Phase-noise significantly affects system performance**

Phase-noise model for TG3c: PLL/VCO and its model

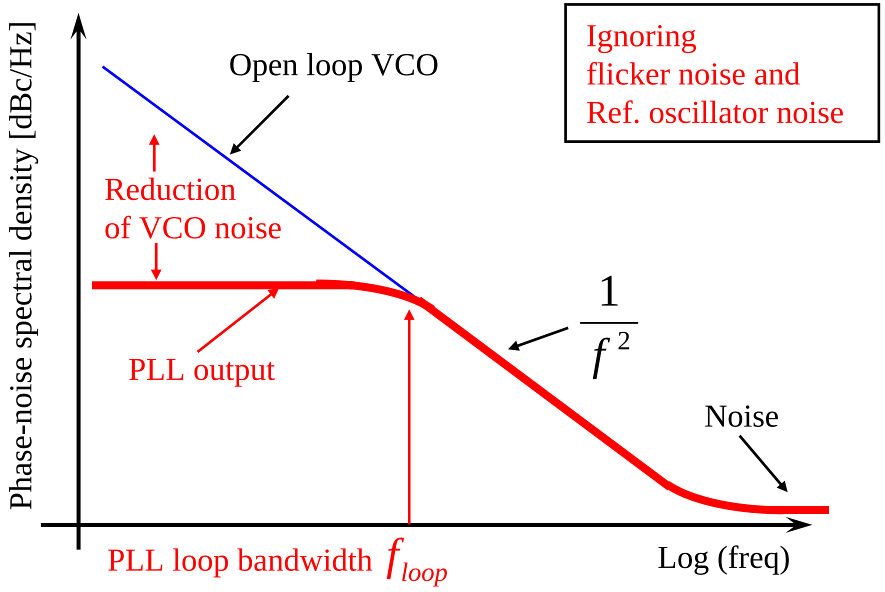


Fig.1: Phase-noise characteristics for VCO and PLL

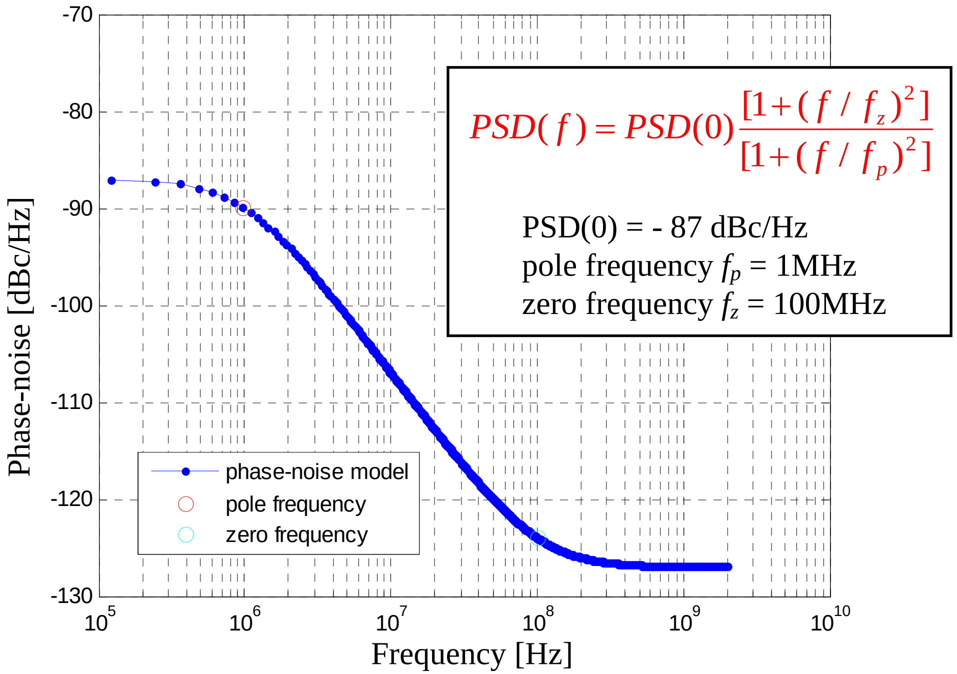


Fig.2: Proposed phase-noise model for TG3c

- **PLL effectively suppresses low frequency noise of VCO, making it possible to transmit phase-modulated data signal.**
- **Proposed model is well expressing this PLL phase-noise characteristic.**

Effect of phase-noise parameters on performance

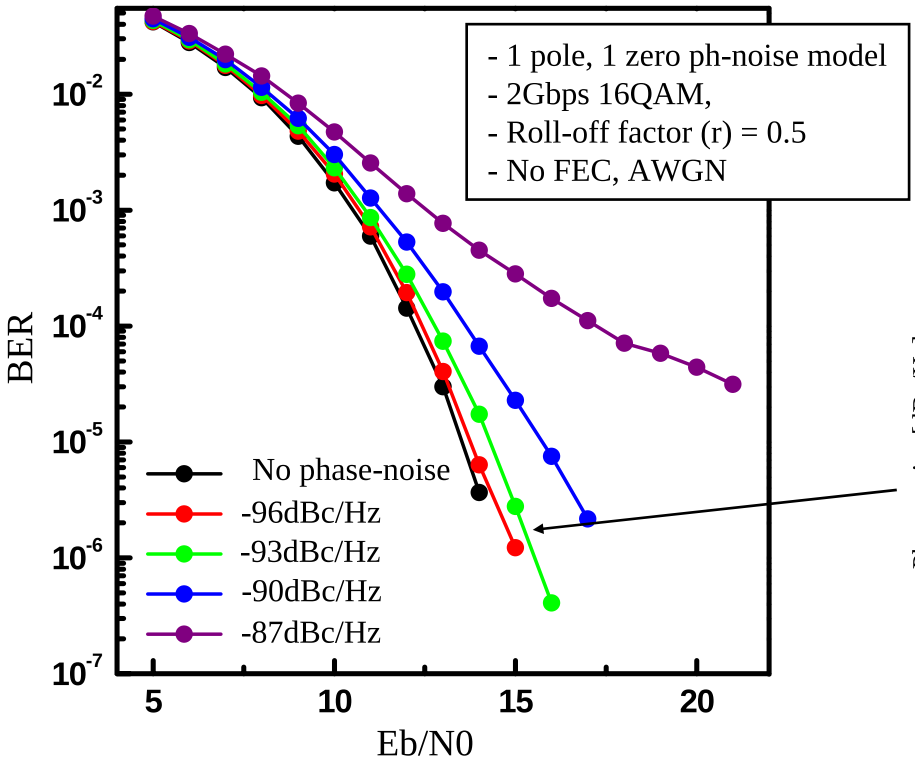
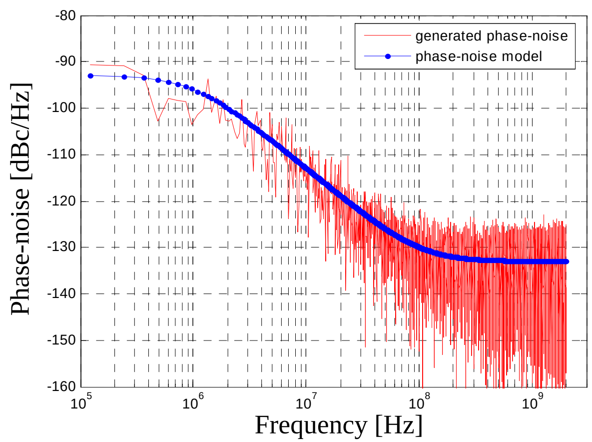


Fig.1: Impact of phase-noise at low frequency on 16QAM transmission

$$PSD(f) = PSD(0)\frac{[1+(f/f_z)^2]}{[1+(f/f_p)^2]}$$

pole frequency f_p = 1MHz
zero frequency f_z = 100MHz



PSD(0) = -93dBc/Hz

Fig.2: Generated phase-noise based on the model

- Phase-noise also affects the system performance, significantly.
- What values are we going to use for PHY simulation?

Available 60GHz-band VCO/PLL

Fabrication, material	Osc. Freq.	Phase noise [dBc/Hz] @1MHz offset	Supply vol.
0.13um CMOS VCO [1]	59 GHz	-89dBc/Hz	1.5V
0.25um CMOS VCO [2]	63 GHz	-85dBc/Hz	1.5V
0.09um CMOS VCO [3]	64 GHz	-110dBc/Hz @ 10MHz offset	1V
0.09um SOI CMOS VCO [4]	60 GHz	-94dBc/Hz	1.2V
SiGe PLL with tripler [5]	~60GHz	-95 ~ -100dBc/Hz	1.5/2.7V
SiGe:C 0.25um BiCMOS PLL [6]	~60GHz	-90 ~ -95 dBc/Hz	3V

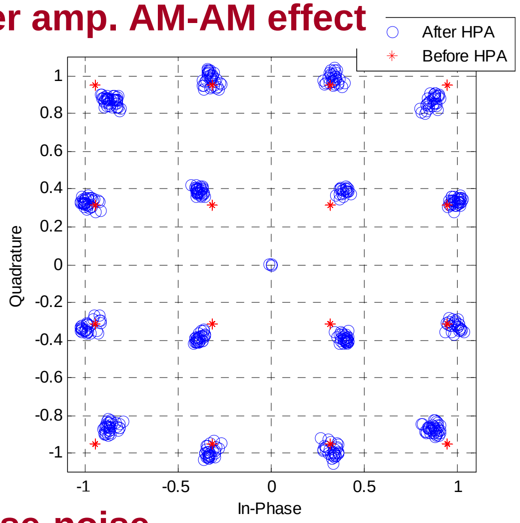
- Si-based VCO/PLL is reasonable due to its integrability and power consumption

- 85 – 90dBc/Hz is suitable for low-frequency phase-noise below 1MHz

Effect of RF impairment on system performance: HPA, phase-noise, and I/Q imbalance

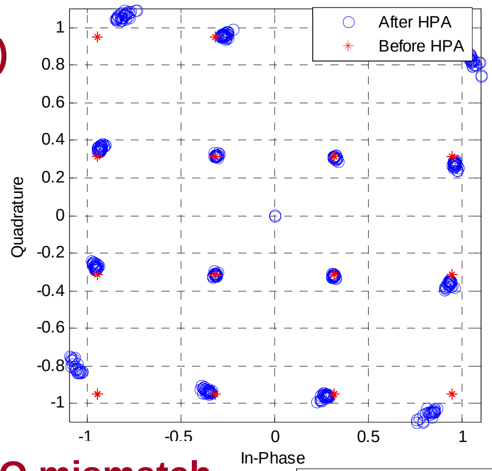
Power amp. AM-AM effect

(A)



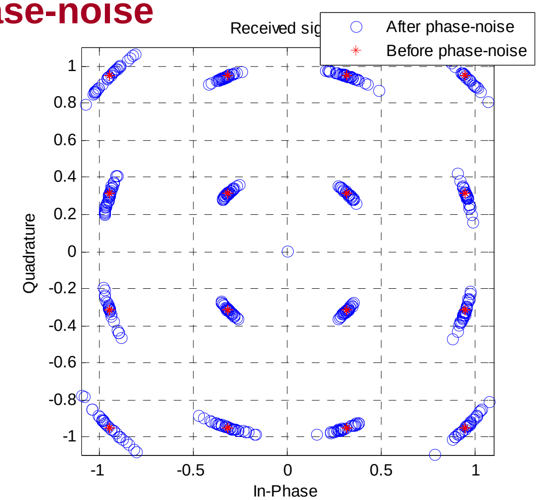
Power amp. AM-PM effect

(B)



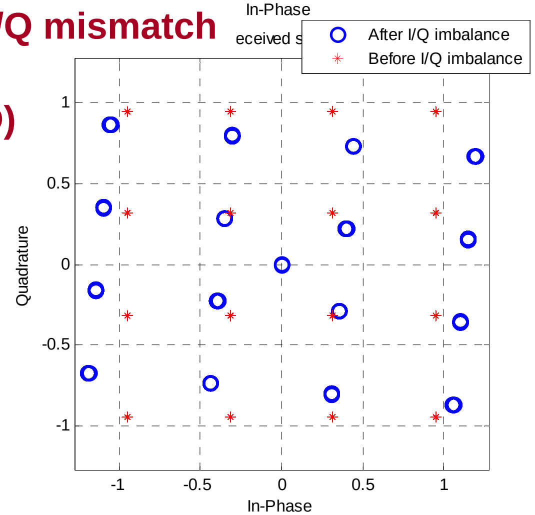
Phase-noise

(C)



I/Q mismatch

(D)



RF impairment model consideration (suggestion)

HPA, phase-noise: mandatory

I/Q mismatch, DAC/ADC: optional

Conclusion

- Power amplifier and phase-noise model should be considered for accurate PHY evaluation
- Modified Rapp model was suggested for expressing PA nonlinearity
- Phase-noise model was suggested for expressing PLL/VCO
- Reasonable parameters for suggested PA and phase-noise model

Without fixing parameters in proposed model,
we cannot match these models to actual 60GHz component measurement results

References

1. C. Cao, et al., “Millimeter-wave voltage controlled oscillator in 0.13um CMOS technology,” IEEE JSSC, vol. 41, no. 6, Jun. 2006.
2. R.-C. Liu, et al., “A 63GHz VCO using standard 0.25um CMOS process,” IEEE ISSCC 2004.
3. L. M. Franca-Neto, et al.,”64GHz and 100GHz VCO in 90nm CMOS using optimum pumping method,” IEEE ISSCC 2004.
4. F. Ellinger, et al.,”60GHz VCO with wideband tuning range fabricated on VLSI SOI CMOS technology,” IEEE MTT-S, 2004.
5. B. Floyd, et al.,”A silicon 60GHz receiver and transmitter chipset for broadband communications,” IEEE ISSCC 2006.
6. W. Winkler, “A fully integrated BiCMOS PLL for 60GHz wireless applications,” IEEE ISSCC 2005.

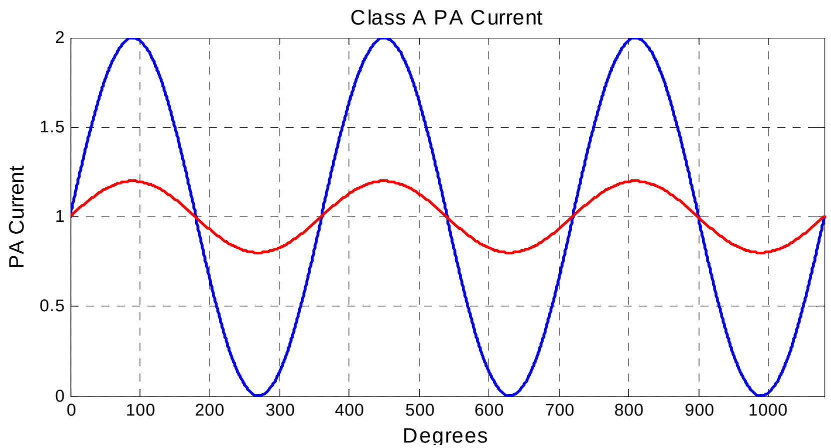
IEEE 802.11n comparison criteria

Number	Name	Definition	Status of this IM
IM1	PA non-linearity	Simulation should be run at an oversampling rate of at least 4x. Use RAPP power amplifier model as specified in document 00/294 with p = 3. Calculate backoff as the output power backoff from full saturation: PA Backoff = -10 log10(Average TX Power/Psat). Total TX power shall be limited to no more than 17 dBm. Disclose: (a) EIRP and how it was calculated, (b) PA Backoff, and (c) Psat per PA. Note: the intent of this IM is to allow different proposals to choose different output power operating points. Note: the value Psat = 25dBm is recommended.	

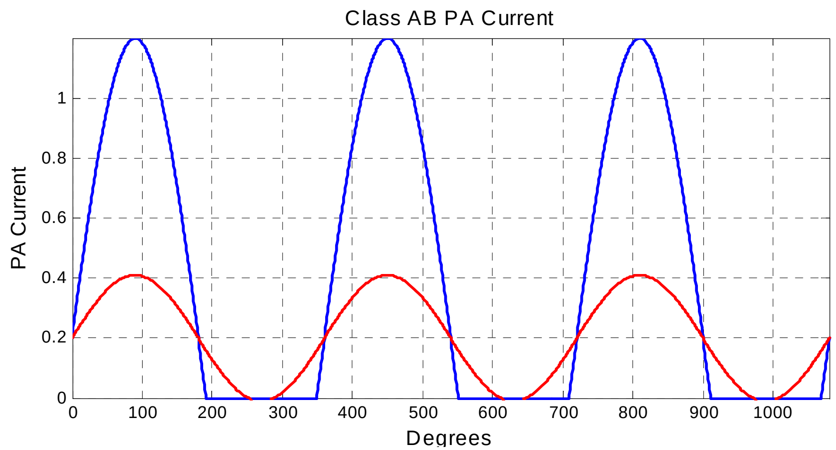
IM4	Phase noise	The phase noise will be specified with a pole-zero model. $PSD(f) = PSD(0)\frac{[1+(f/f_z)^2]}{[1+(f/f_p)^2]}$ PSD(0) = -100 dBc/Hz pole frequency f_p = 250 kHz zero frequency f_z = 7905.7 kHz Note, this model results in PSD(infinity) = -130 dBc/Hz Note, this impairment is modeled at both transmitter and receiver.	

Adapted from IEEE 802.11-03/814r31

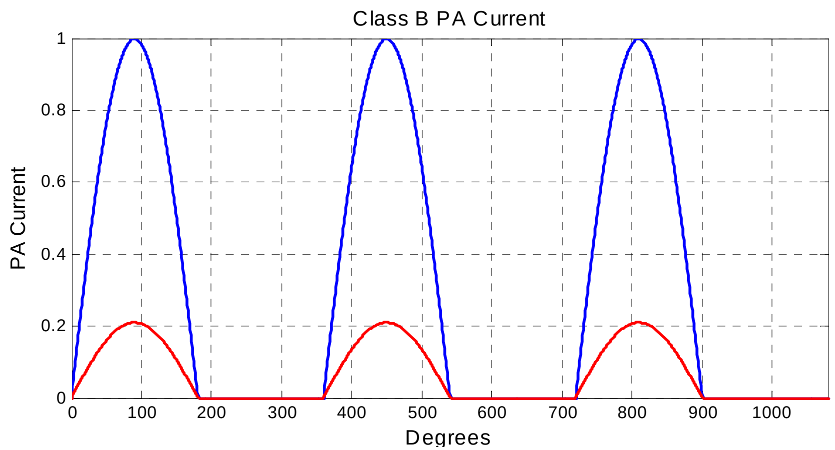
Classes of high power amplifier



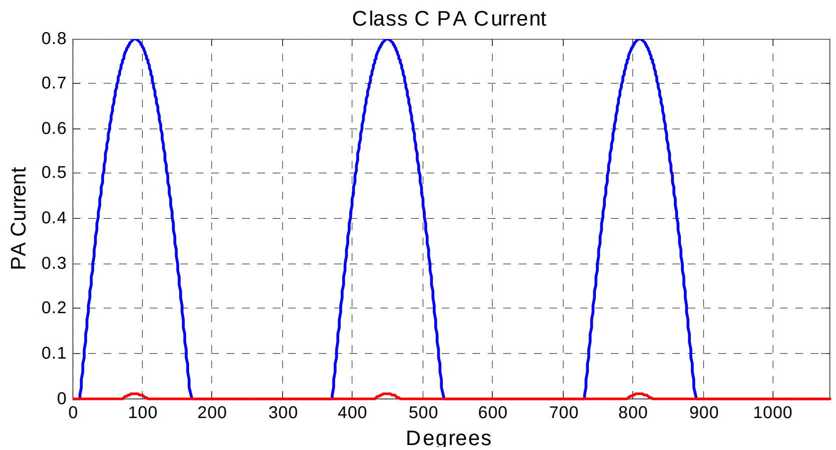
Class A: Max. power efficiency: 50%



Class AB: Max. power efficiency: 50-78%

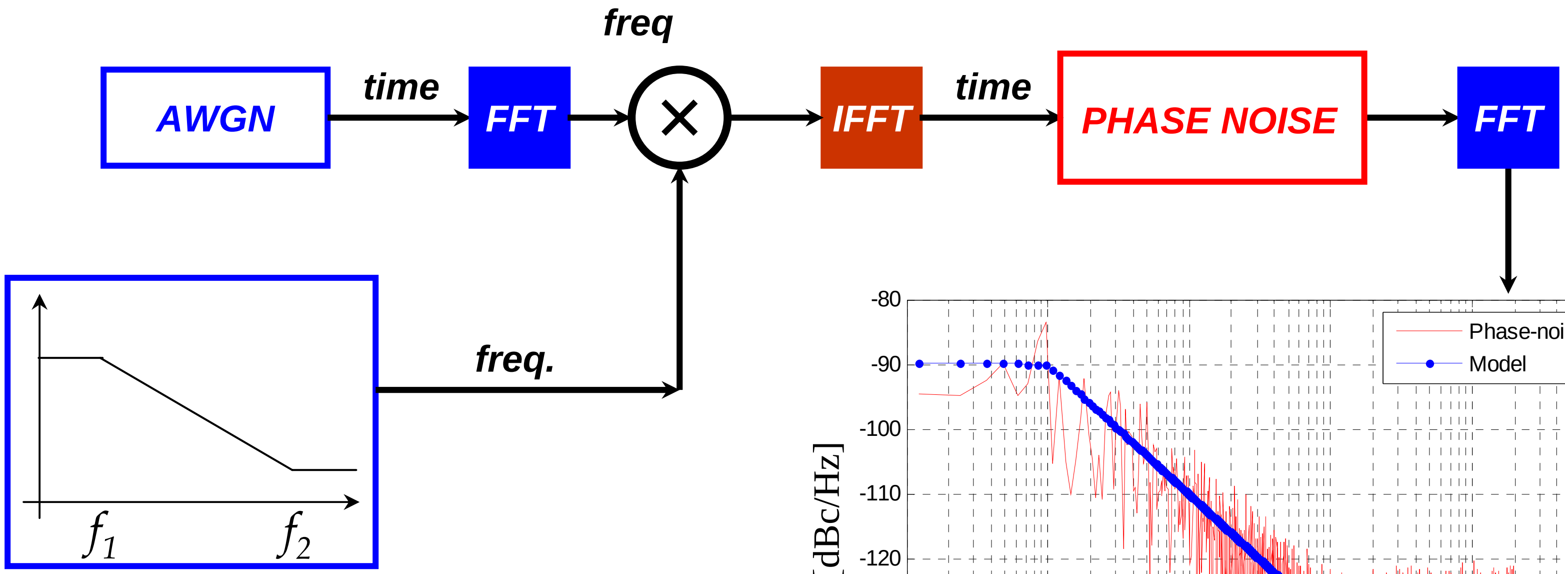


Class B: Max. power efficiency: 78%

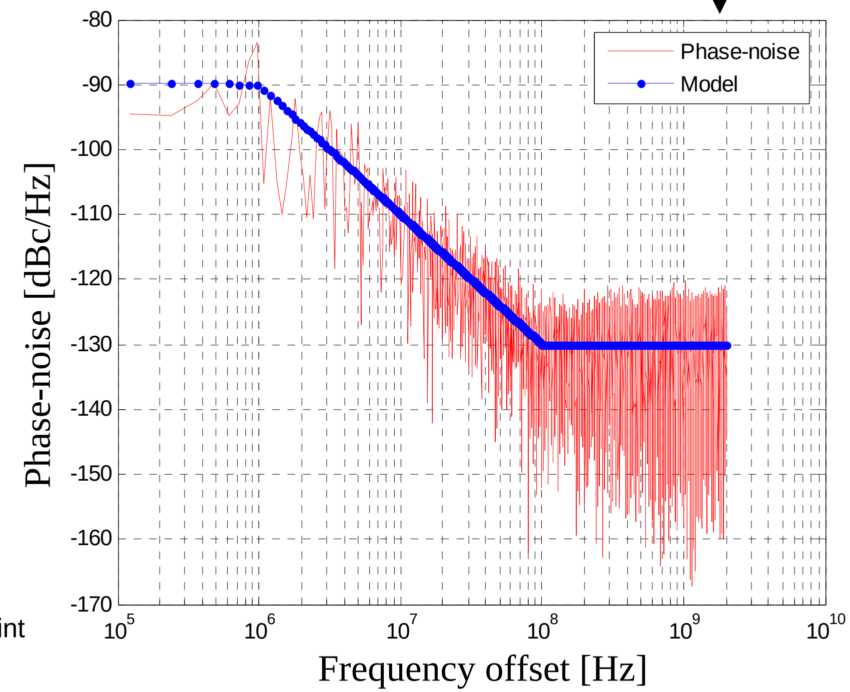


Class C: Max. power efficiency: 100%

How to generate phase-noise



Phase-noise characteristics



128k FFT point