Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: [Millimeter-wave CMOS RFIC]
Date Submitted: [15 November, 2006]
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Re: []

Abstract: [Description of the current status of CMOS RFIC development]
Purpose: [Contribution to TG3c at November 2006 meeting.]

Millimeter-wave CMOS RFIC

Tian-Wei Huang

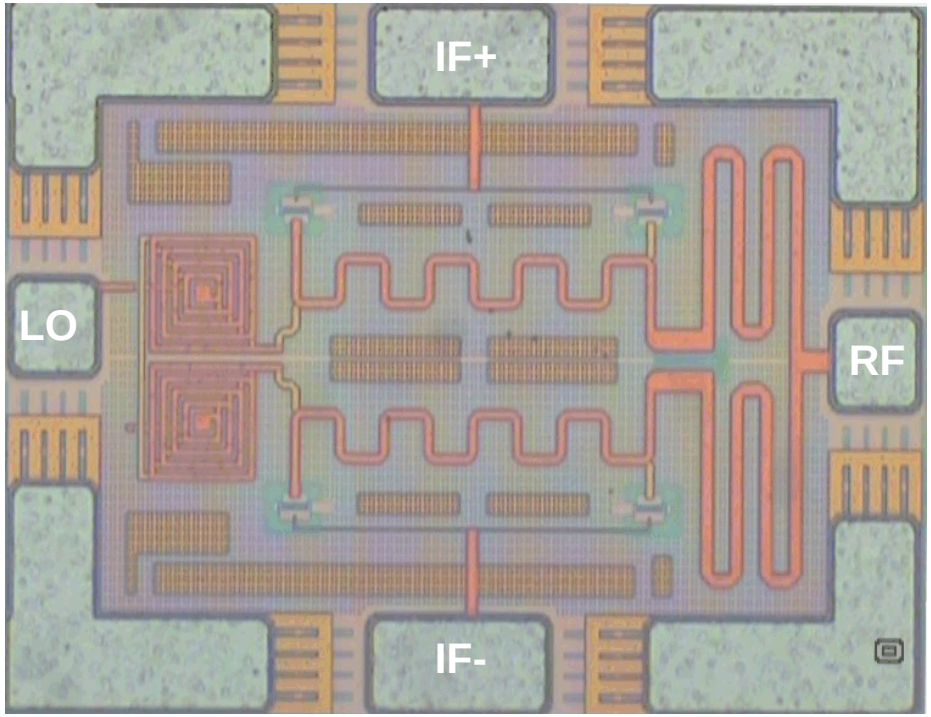
National Taiwan University

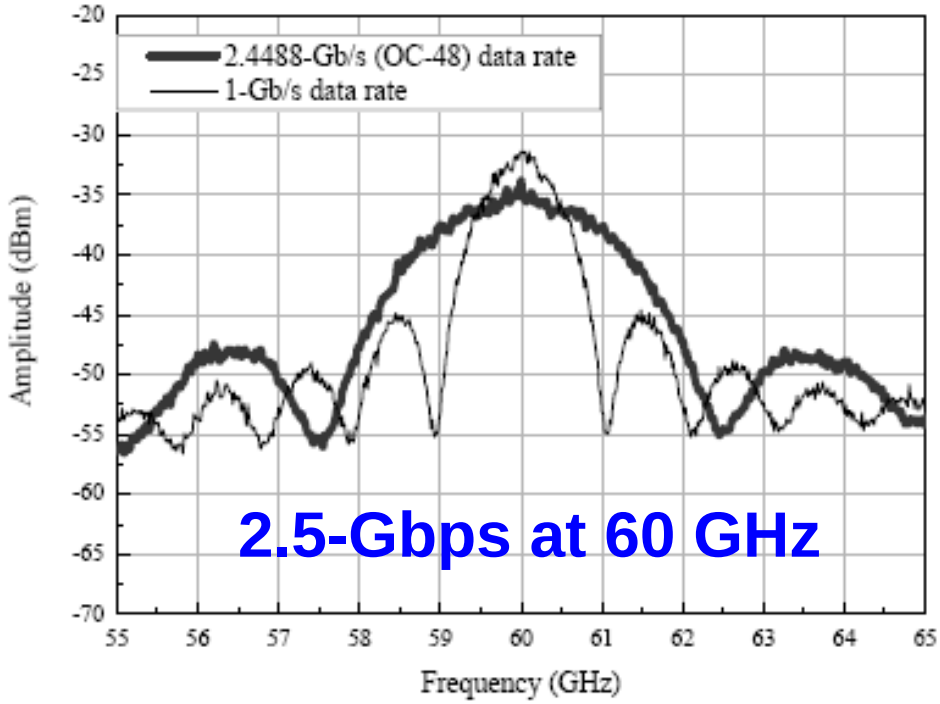
November 15, 2006

Agenda

- Gbps CMOS Modulator/Transmitter
- CMOS Low-Noise Amplifier
- CMOS Active Mixer and VCO
- SiGe 60-GHz Transmitter with Integrated Antenna

A 60-GHz 2.5-Gbps CMOS BPSK Modulator



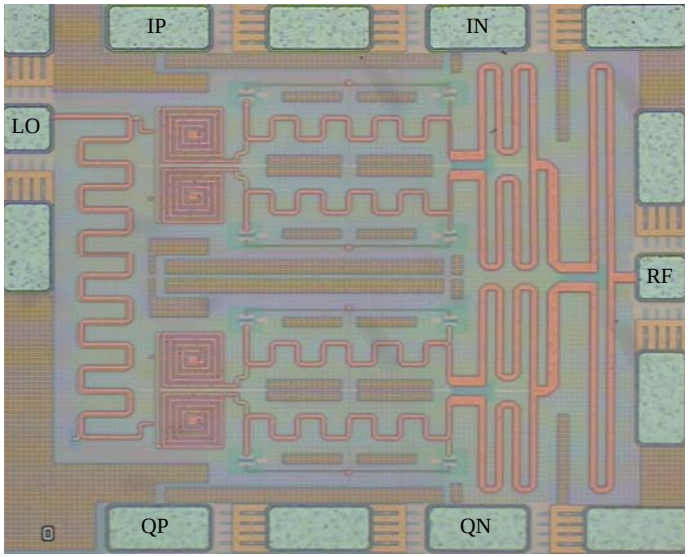


- Modified reflection-type
- 0.13 μm CMOS technology
- Chip size : 0.5 × 0.35 mm^2

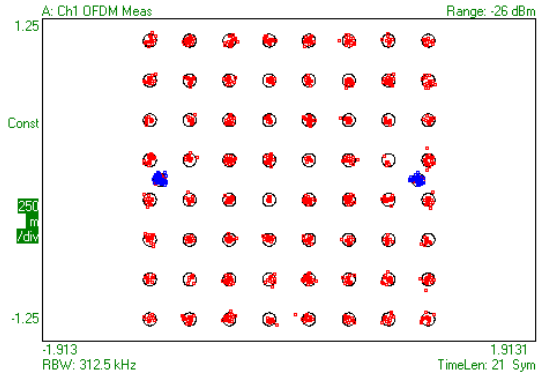
- Frequency: 15-75 GHz
- Phase Imbalance < 3°
- Amplitude Imbalance < 0.5 dB
- Modulation bandwidth > 1 GHz

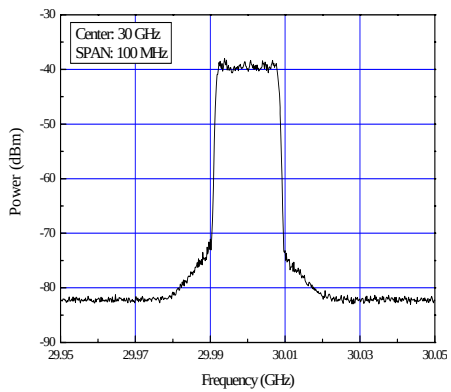
Hong-Yeh Chang, Pei-Si Wu, Tian-Wei Huang, Huei Wang, Yung-Chih Tsai, and Chun-Hung Chen "An ultra compact and broadband 15-75 GHz BPSK modulator using 0.13-μm CMOS process," *2005 IEEE MTT-S IMS Digest*, Long Beach, CA, June 2005.

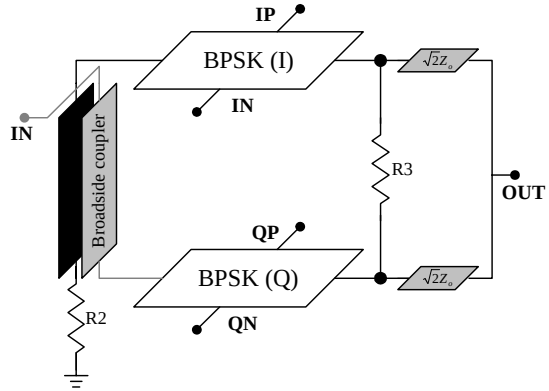
CMOS MMW IQ Modulator



- TSMC 0.13-μm CMOS Process
- Chip Size: 0.65 × 0.58 mm^2
- Modified Reflection-type Modulator
- Frequency: 20-40 GHz
- Sideband Suppression > 20 dB
- LO Suppression > 30 dB
- Spurs Suppression > 30 dB
- P_{1dB} > -5 dBm
- Conversion Loss < 13 dB
- Modulation bandwidth > 1 GHz

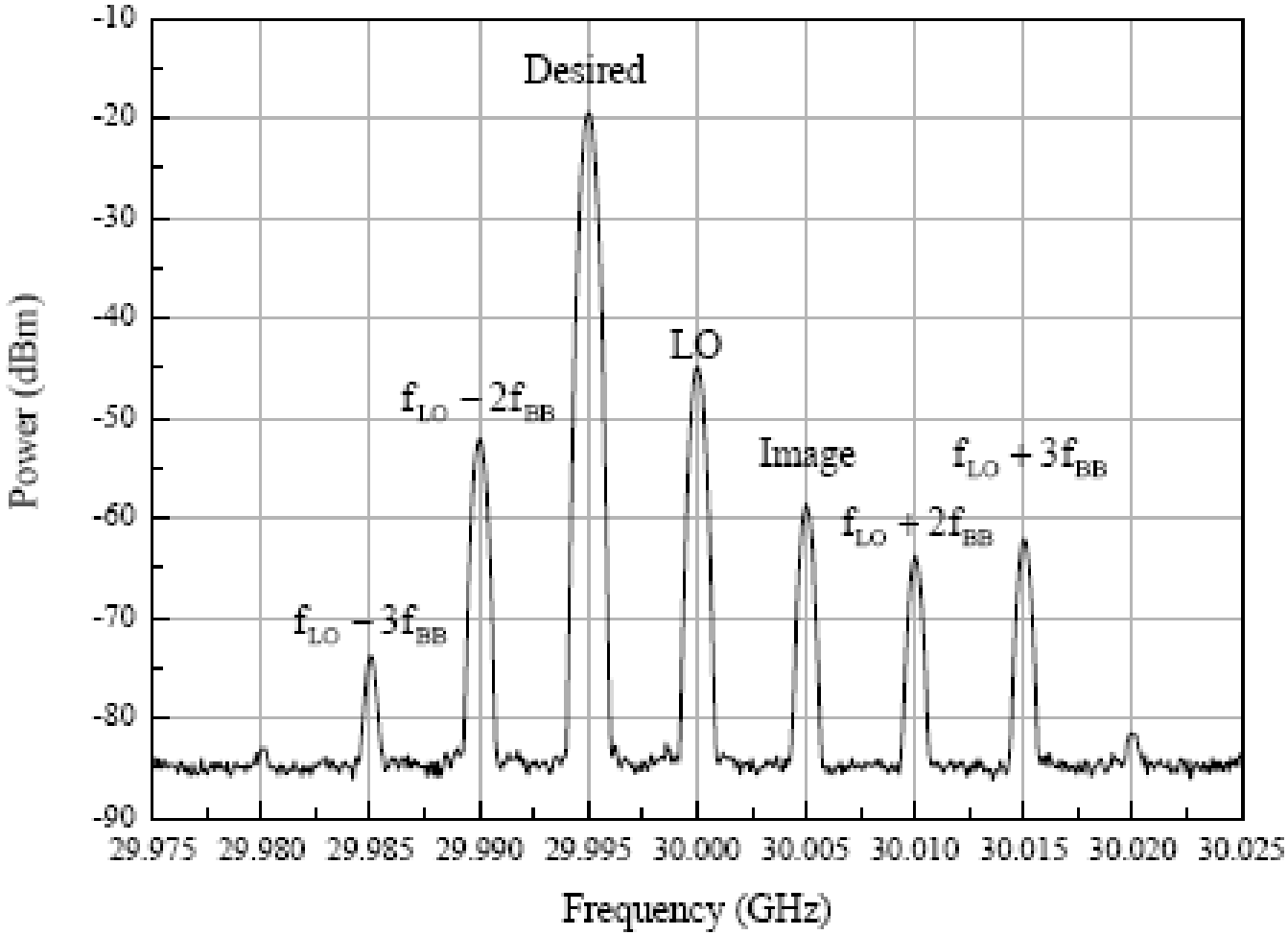




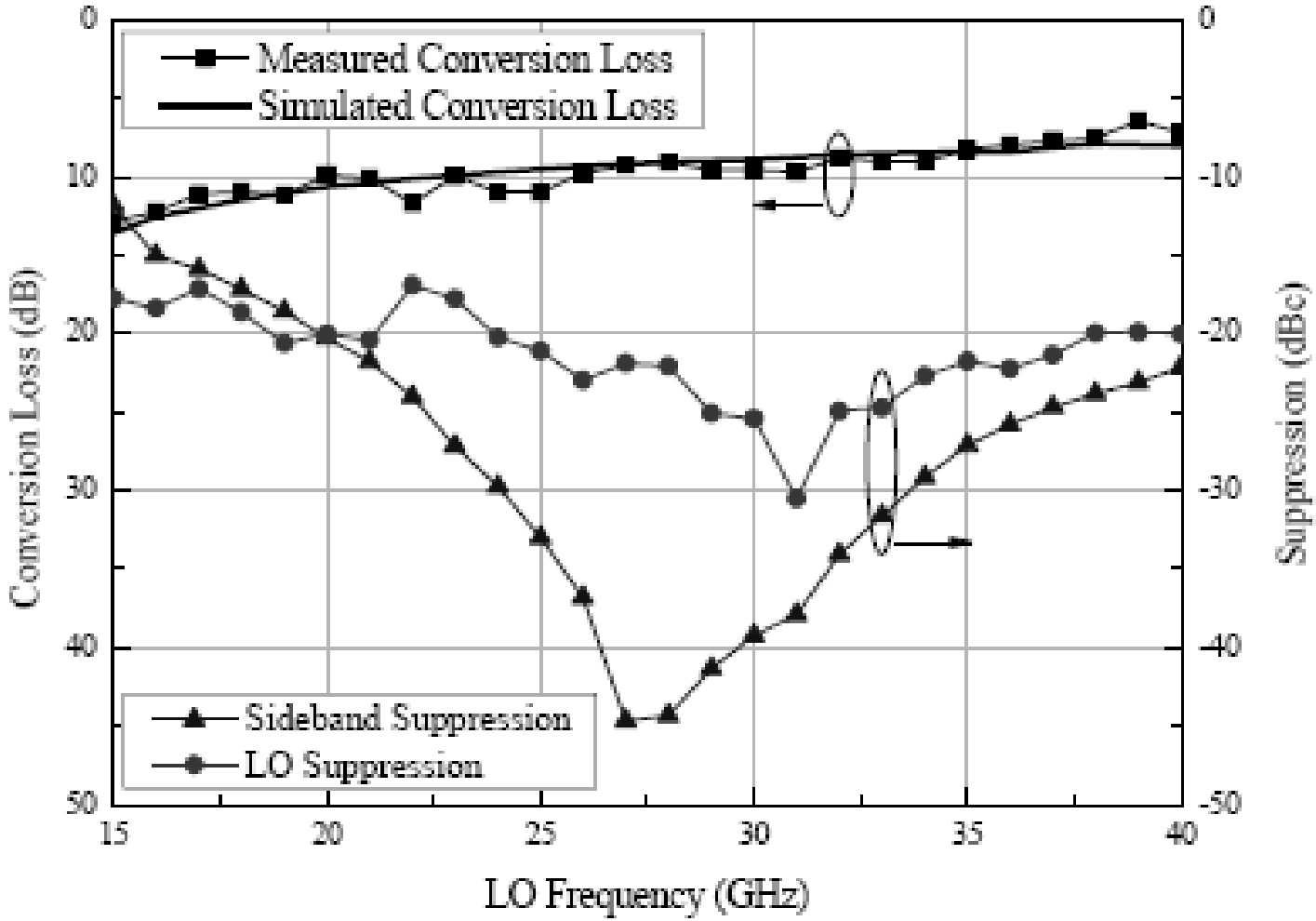


Hong-Yeh Chang, and et al, "Design and analysis of CMOS broad-band compact high-linearity modulators for gigabit microwave/millimeter-wave applications," *IEEE Transactions on Microwave Theory and Techniques*, Jan. 2006.

Measured output spectrum of the IQ modulator

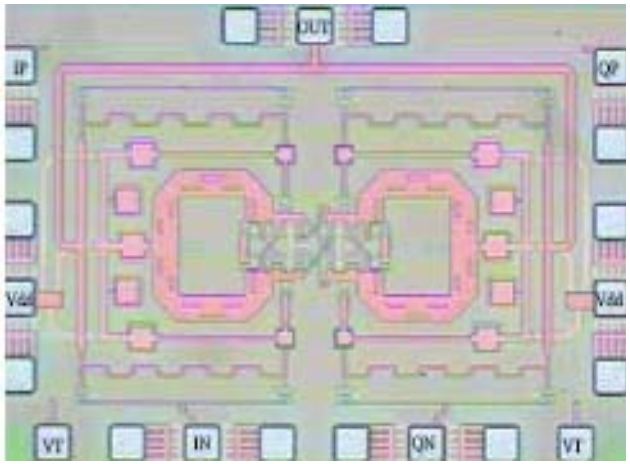


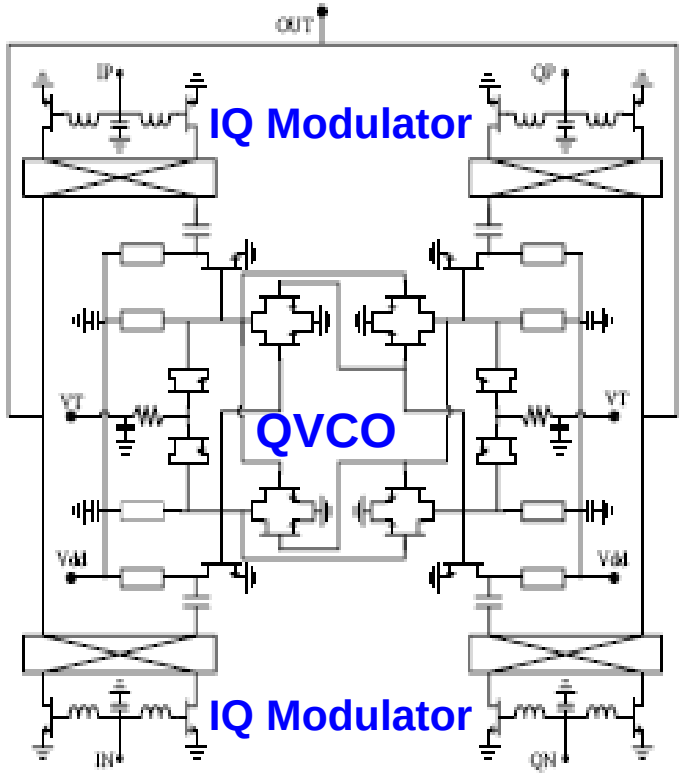
Conversion loss and LO suppression



A 0.13-μm mmW CMOS Transmitter

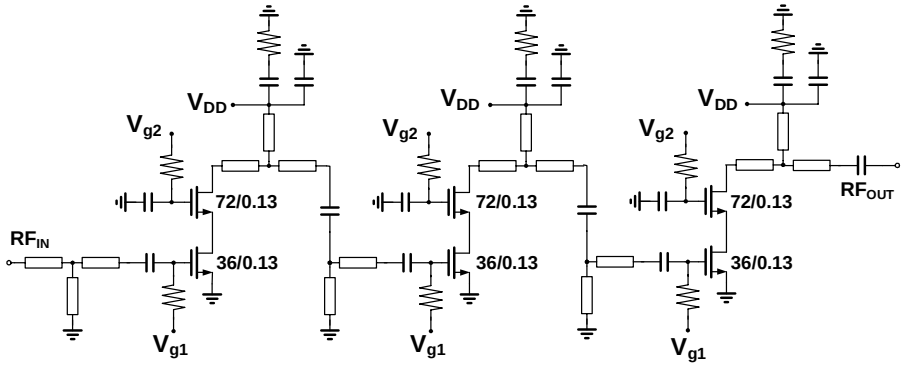
- Technology: 0.13 μm CMOS technology
- Chip size: 0.85 x 0.6 mm^2
- Frequency: 44.8-45.8 GHz,
- Phase Imbalance < 1.8°,
- Amplitude Imbalance < 0.7 dB
- DC power consumption: 40mW



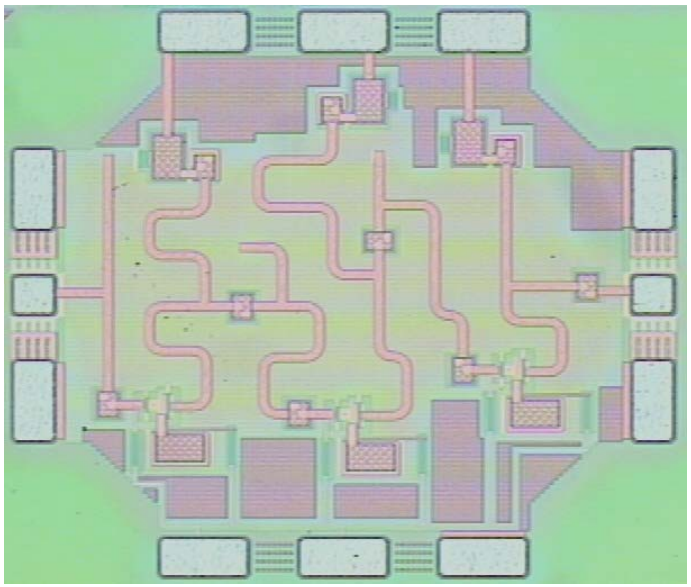


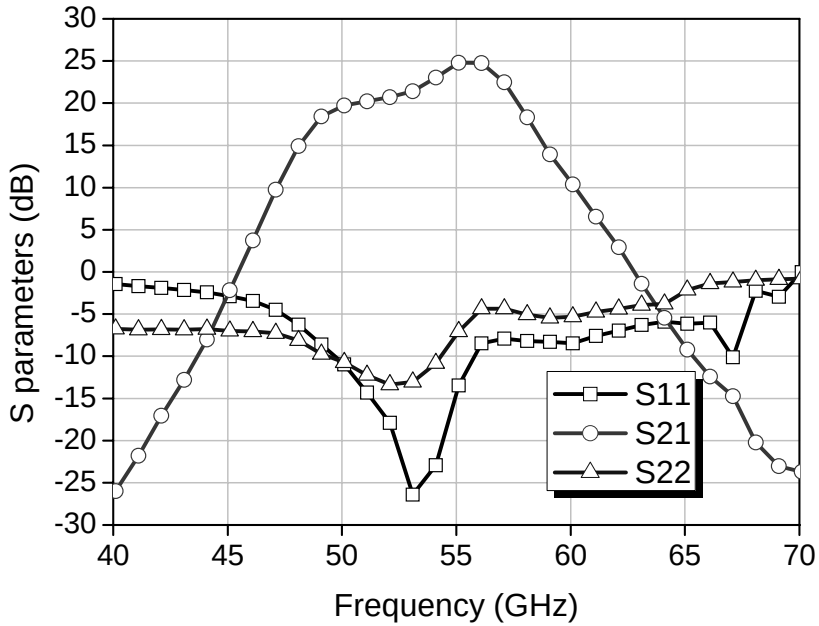
Hong-Yeh Chang, Tian-Wei Huang and Huei Wang, "A 45-GHz quadrature voltage controlled oscillator with a reflection-type IQ modulator in 0.13-μm CMOS technology," 2006 *IEEE MTT-S International Microwave Symposium Digest*, San Francisco, CA, June 2006.

V-band 3-Stage Cascode LNA (0.13μm CMOS)



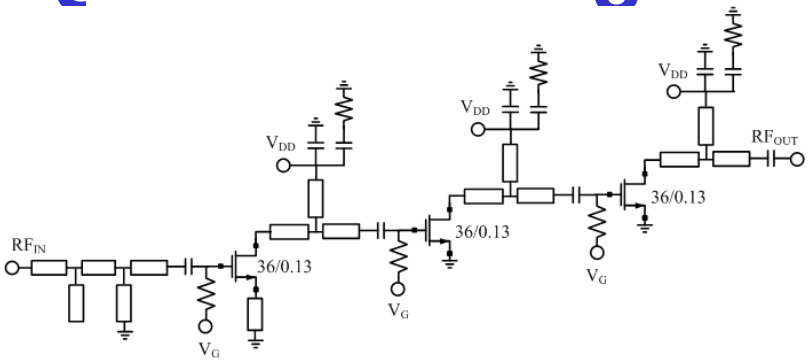
- Gain > 20 dB from 51 to 57.5 GHz
- NF < 8 dB from 50 to 57 GHz
- Input P_{1dB} : -22 dBm
- IIP3 : -12 dBm at 56 GHz





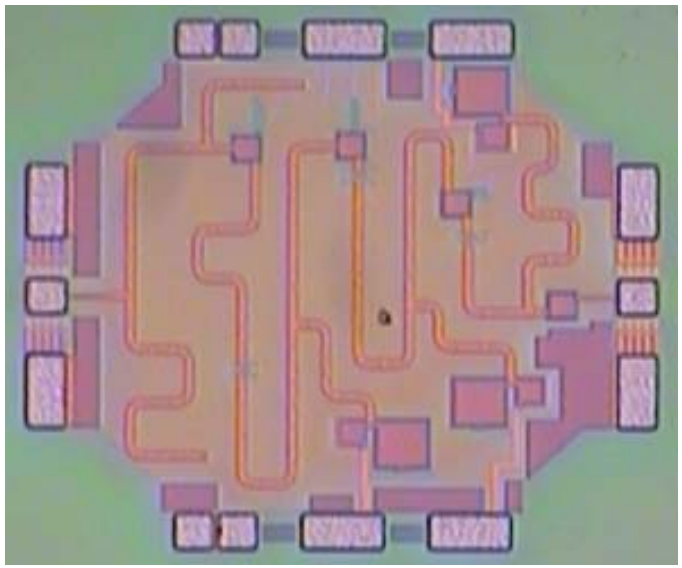
Chieh-Min Lo, Chin-Shen Lin, and Huei Wang, "A Miniature V-band Three-Stage Cascode Low Noise Amplifier in 130nm CMOS Technology," *ISSCC 2006*, San Francisco, Feb. 2006.

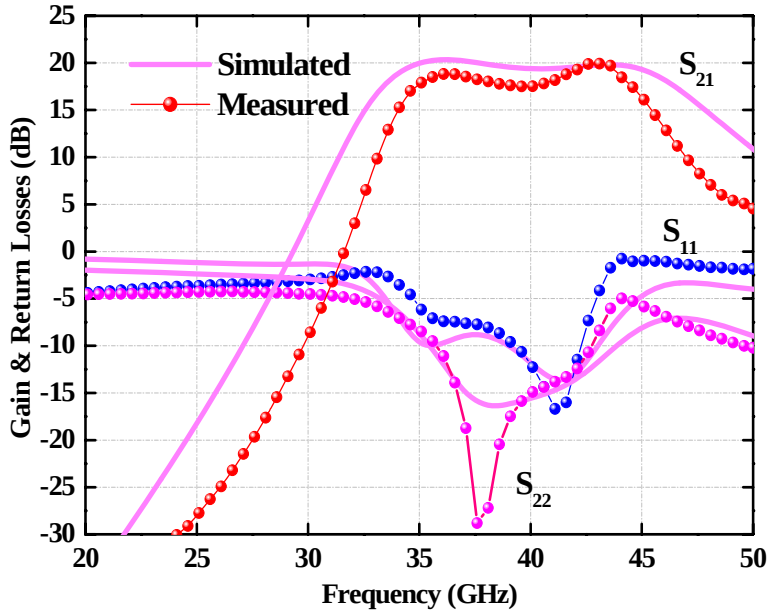
Q-band 3-Stage LNA (0.13μm CMOS)



- Gain > 17 dB from 34 to 44 GHz
- NF < 7 dB from 40 to 42 GHz
- OP_{1dB} : +4 dBm (Psat: +7dBm)
- OIP3 : +14.5 dBm
- Power dissipation: 24 mA at +1.5 V

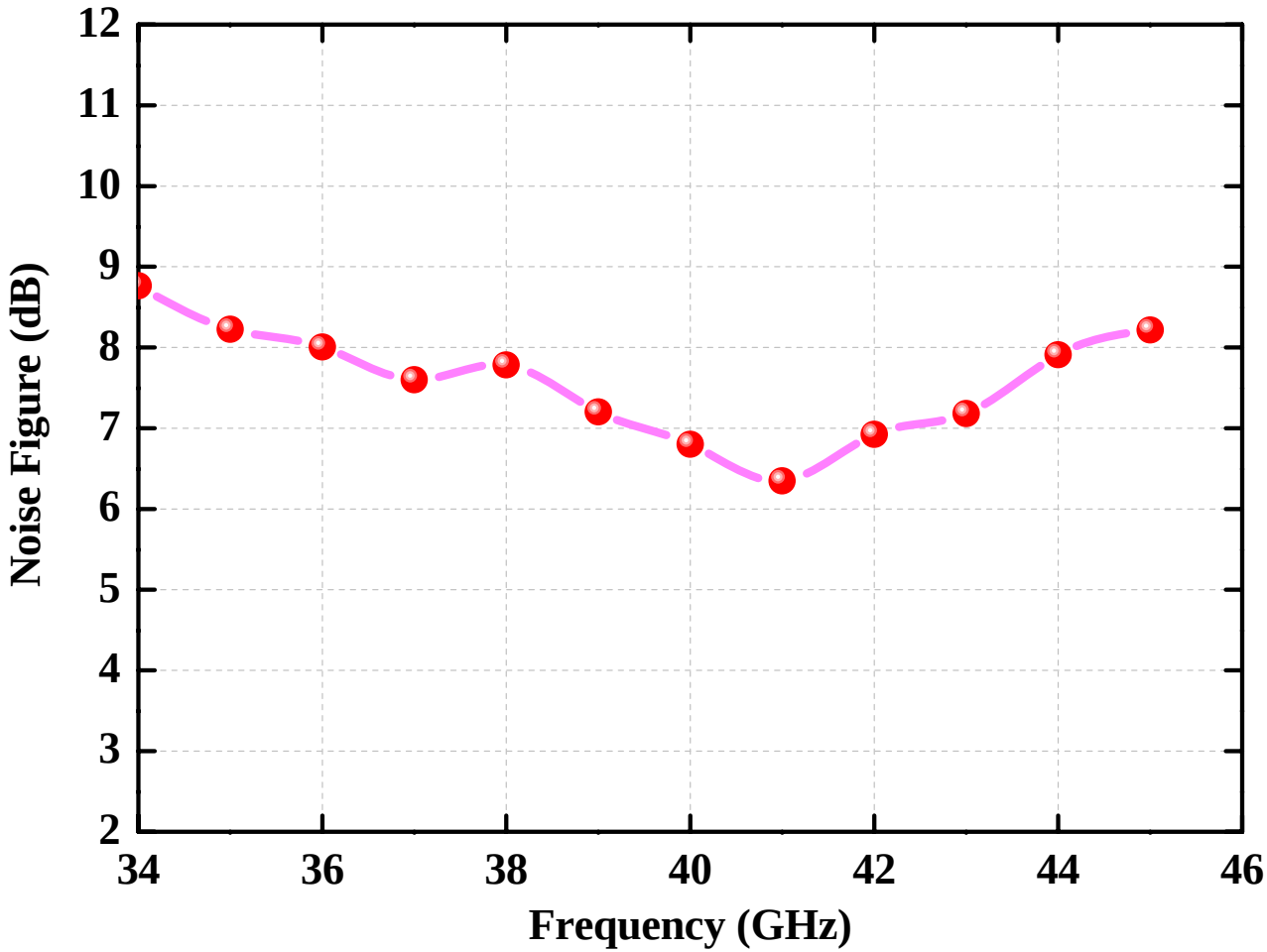
0.75 mm x 0.7 mm



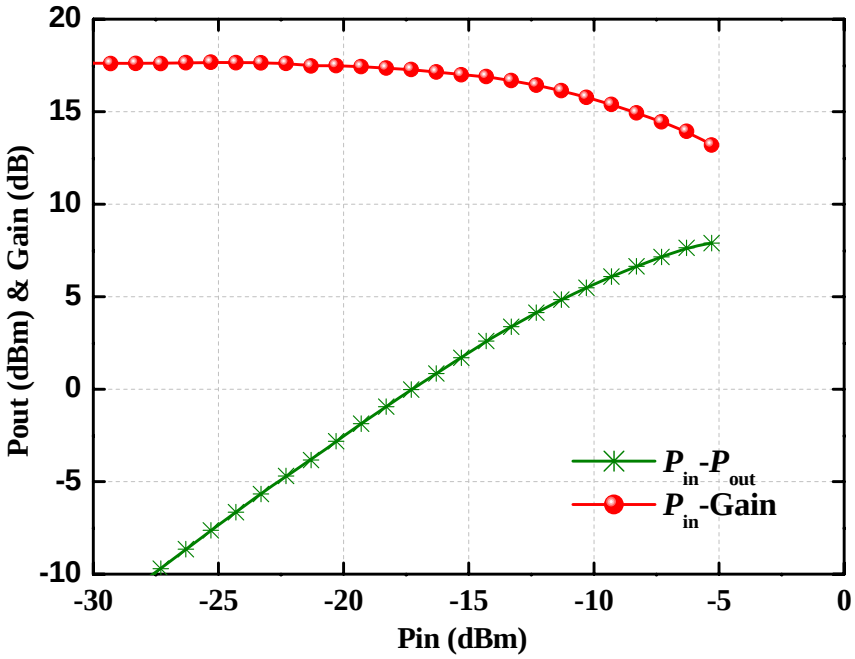


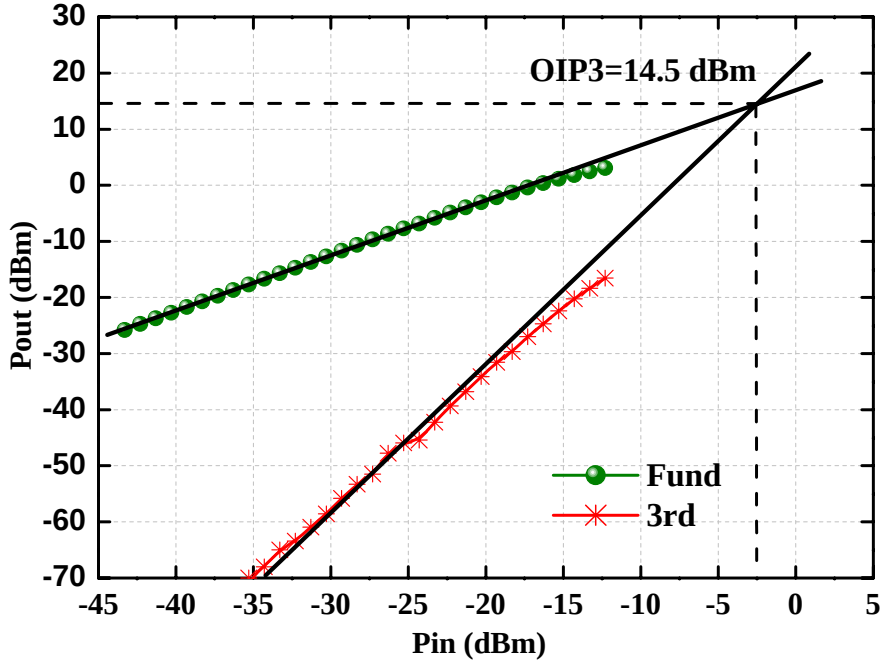
Jeng-Han Tsai, Wei-Chien Chen, To-Po Wang, Tian-Wei Huang, and Huei Wang, " A Miniature Q-band Low Noise Amplifier Using 0.13-mm CMOS Technology," *IEEE Microwave and Guided Wave Letters*. Vol. 16, No. 6, pp. 327-329, June 2006.

Q-band 3-Stage LNA (Noise Figure)



Q-band 3-Stage LNA (AM-AM & IP3)



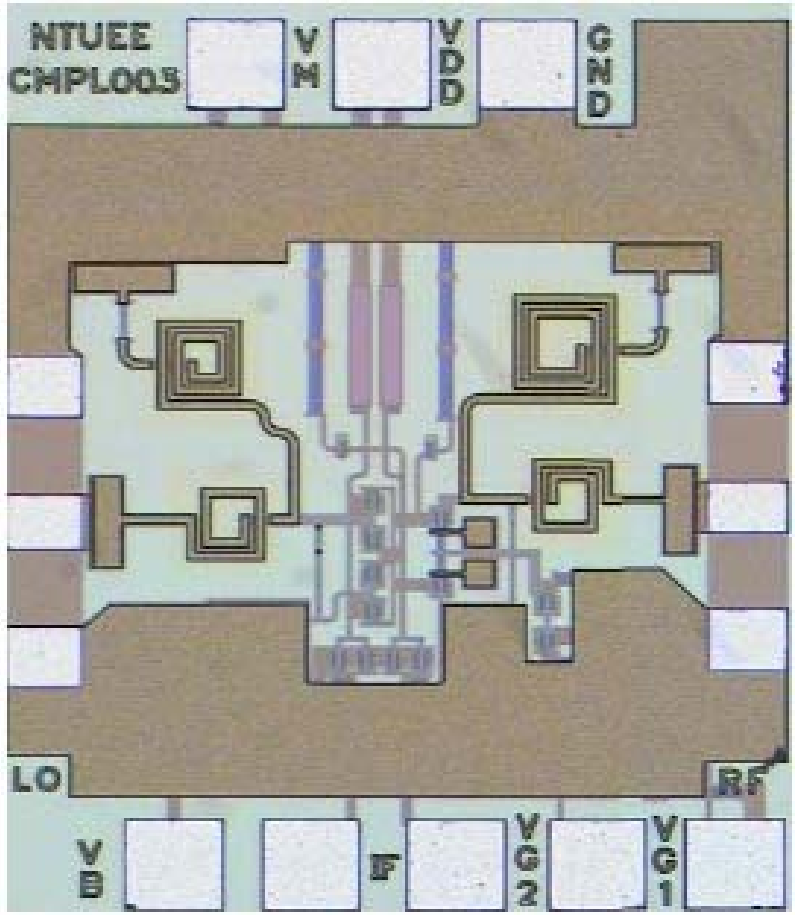


Q-band CMOS LNA (Comparison)

Ref.	This work	[5]	[3]	[4]	[2]
Process	0.13µm CMOS	0.13µm CMOS	0.18µm CMOS	90nm CMOS	90nm SOI
Circuit Topology	3-stage common source	3-stage cascode	3-stage cascode	2-stage common source	1-stage cascode
3-dB BW (GHz)	10 (34-44)	10 (34-44)	5 (37-42)	14 (32-46)	16 (26-42)
Peak Gain (dB)	20 @43GHz	19 @40GHz	7 @40GHz	7.3 @35GHz	11.9 @35GHz
Chip Area (mm^2)	0.525	1.43	2.04	N/A	0.18
Power dissipation	24mA @1.5V	24mA @1.5V	100mA @3V	7mA @1.5V	17mA @2.4V
NF (dB)	6.3 @41GHz	N/A	N/A	N/A	3.6 @35GHz
OP1dB (dBm)	4	-0.9	5	-5.75	4
OIP3 (dBm)	14.5	11.6	N/A	7	N/A

0.3-25 GHz CMOS Gilbert-Cell Mixer

- 0.18-μm CMOS
- Gilbert-cell mixer with LC ladder matching network
- Conversion Gain: +11 dB from 0.3-25 GHz
- Isolation between LO and RF: > 20 dB
- LO power: -1 dBm
- IF: 10 MHz

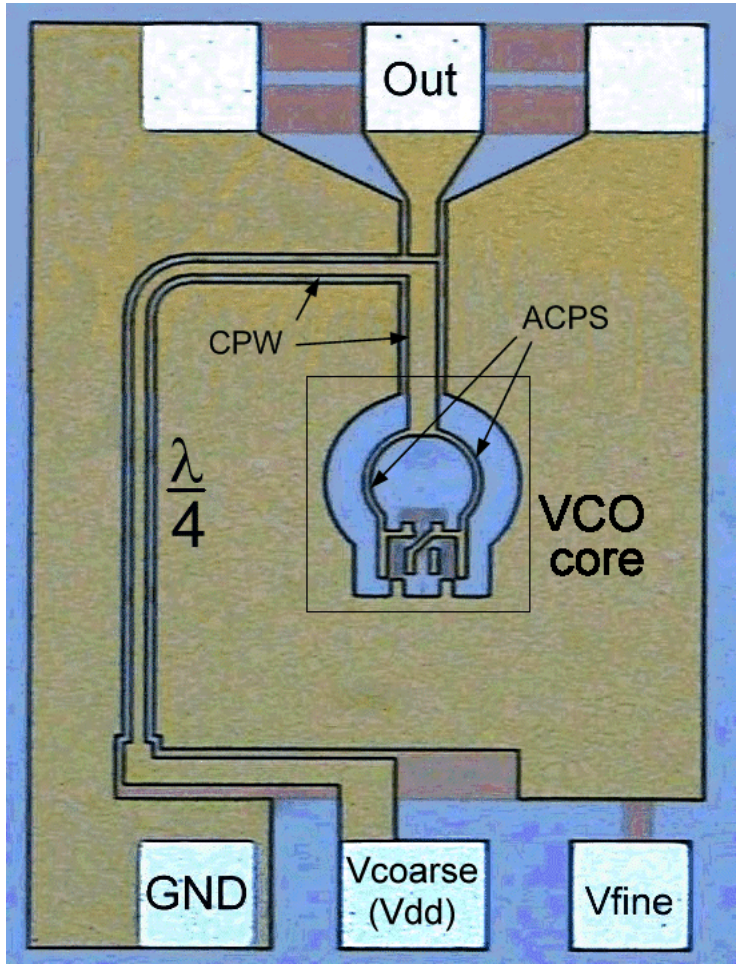


0.8 mm x 1.0 mm

Ming-Da Tsai and Huei Wang, "A 0.3-25-GHz ultra-wideband mixer using commercial 0.18-μm CMOS technology," *IEEE Microwave and Wireless Component Letters*, vol. 14, no. 11, pp. 522-524, Nov. 2004.

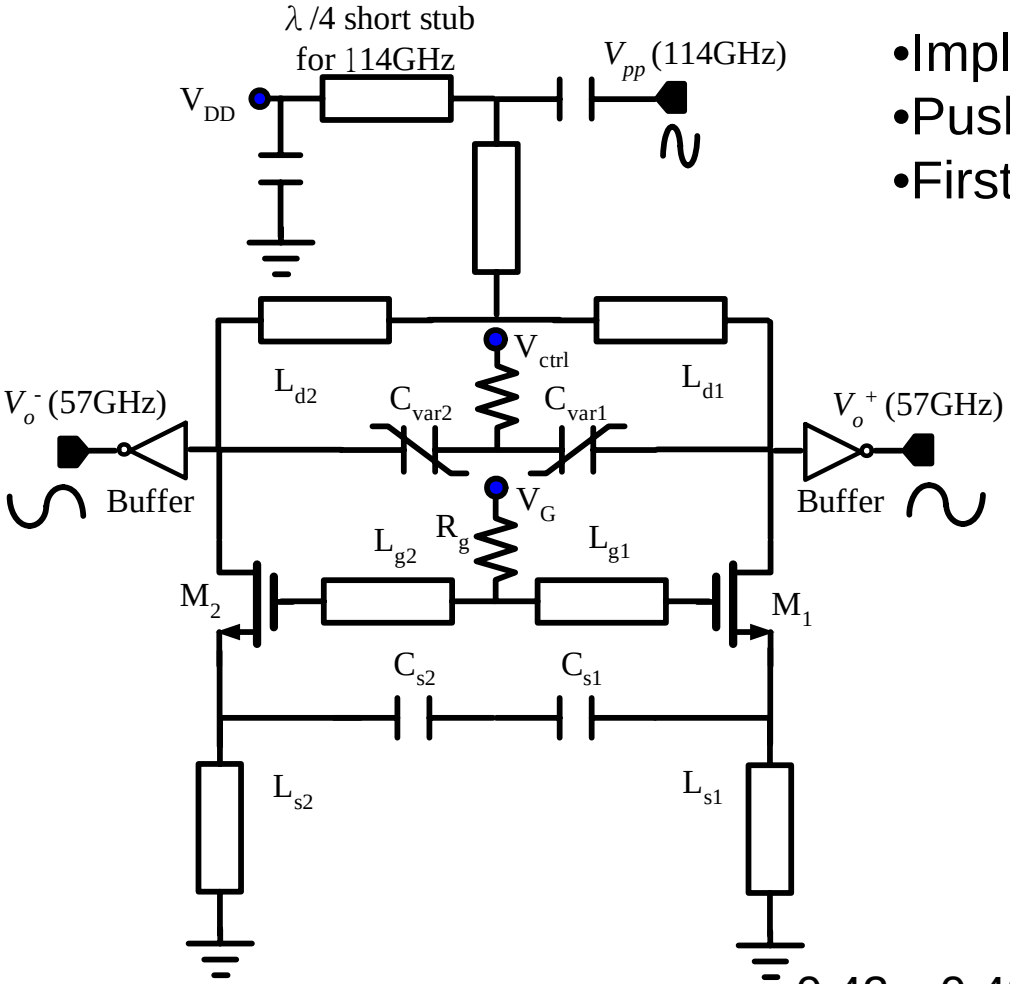
63 GHz CMOS VCO

- 0.25-μm bulk CMOS
- Push-push design using cross-couple pair
- 63 GHz output extracted through 50 ohm CPW and blocking capacitor
- V_{dd} fed through λ/4 line
- Chip size: 0.45 x 0.7 mm^2
- -85 dBc/Hz @ 1 MHz offset
- Output frequency from 62 to 64.5 GHz
- Better than 25 dB rejection
- -4 dBm max. output power

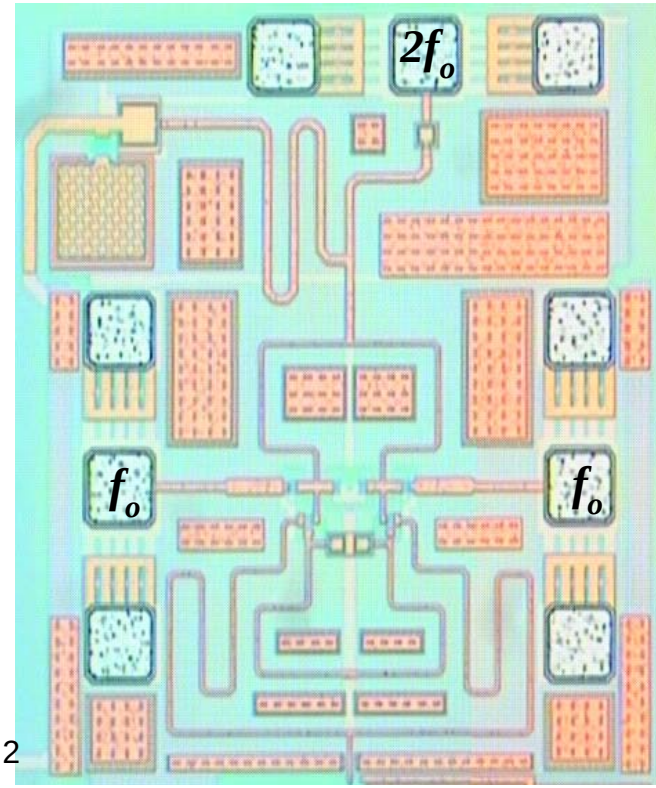


Ren-Chieh Liu, Hong-Yeh Chang, Chi-Hsueh Wang, and Huei Wang, "A 63-GHz VCO using a standard 0.25-μm CMOS process," *2004 International Solid-State Circuit Conference (ISSCC)*, pp. 446-447, San Francisco, Feb., 2004.

114-GHz CMOS VCO



- Implemented in TSMC 0.13-μm CMOS
- Push-Push topology
- First CMOS VCO above 100 GHz

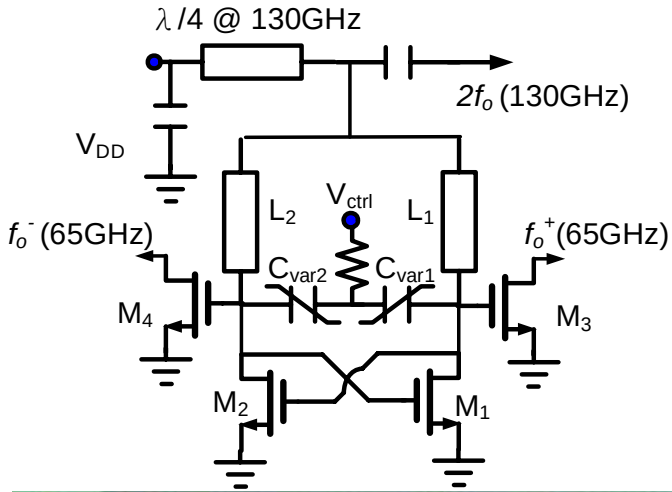


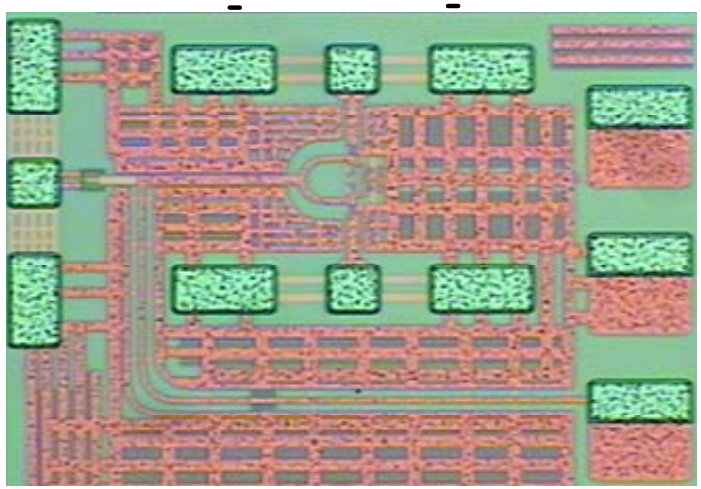
0.42 x 0.48 mm²

Ping-Chen Huang, Ming-Da Tsai, Huei Wang, Chun-Hung Chen, and Chih-Sheng Chang, "A 114GHz VCO in 0.13μm CMOS technology," *2005 International Solid-State Circuit Conference (ISSCC)*, pp. 404-405, San Francisco, Feb. 2005.

131-GHz VCO Using 90-nm CMOS

- 90-nm bulk CMOS technology
- Cross-coupled topology
- Coplanar waveguide (CPW) & asymmetric coplanar slot (ACPS)
- 0.55 x 0.65 mm^2
- 1.2 V / 27.6 mW (core)
- Output power: -11.4 dBm
- Phase noise: -108.4 dBc/Hz @ 10 MHz offset (estimated)
- Tuning range: 2.2 GHz

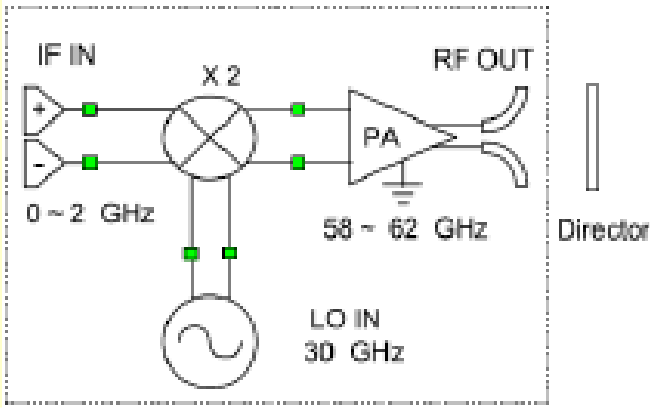


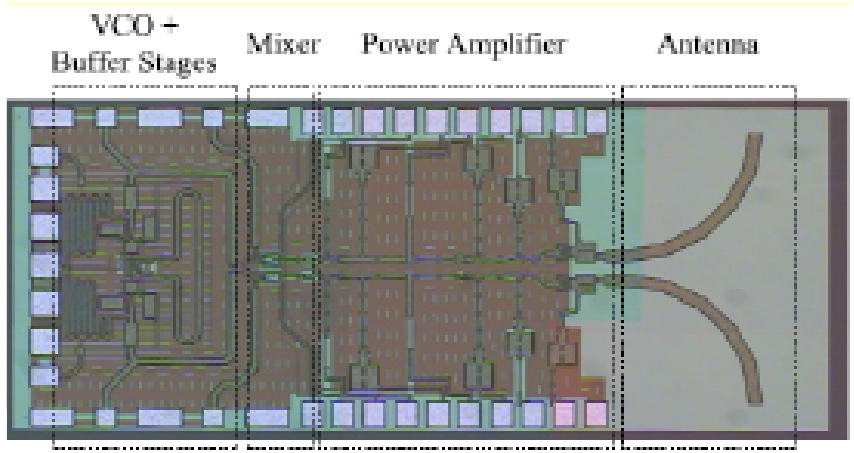


Ping-Chen Huang, Ren-Chieh Liu, Hong-Yeh Chang, Chin-Shen Lin, Ming-Fong Lei, Huei Wang, Chia-Yi Su, and Chia-Long Chang, "A 131-GHz push-push VCO in 90-nm CMOS technology," *2005 IEEE RFIC Symposium Digest*, pp. 613-616, Long Beach, CA, June 2005.

60-GHz Transmitter with Integrated Antenna

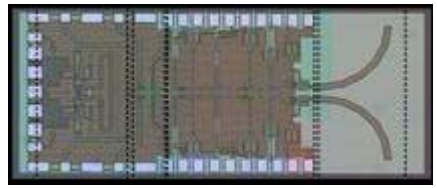
- Technology: 0.18- μ m SiGe BiCMOS process
- Chip size: 1.3 x 0.8 mm^2
- Conversion gain: 20.2 dB
- Output power: 15.8 dBm
- DC power consumption: 281 mW



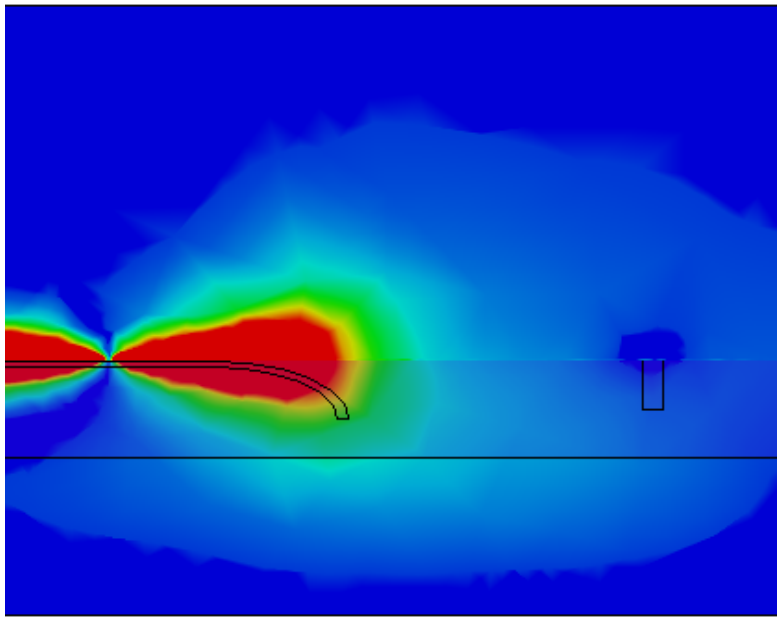


Chi-Hsueh Wang, Yi-Hsien Cho, Chin-Shen Lin, Huei Wang, Chun-Hsiung Chen, Dow-Chih Niu, John Yeh, Chwan-Ying Lee, and John Chern,"A 60-GHz transmitter with integrated antenna in 0.18-mm SiGe BiCMOS technology," 2006 *International Solid-State Circuit Conference (ISSCC),* San Francisco, CA, Feb. 2006.

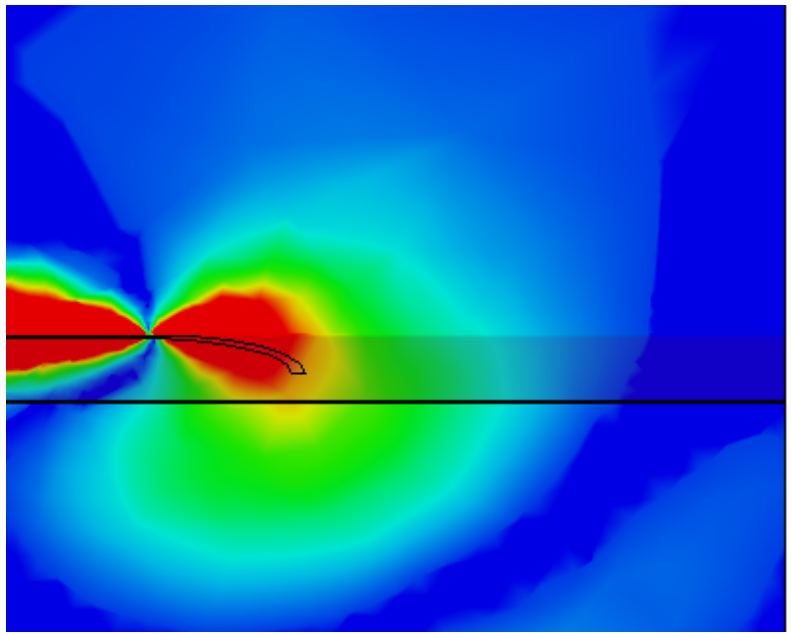
Antenna Design



With antenna director

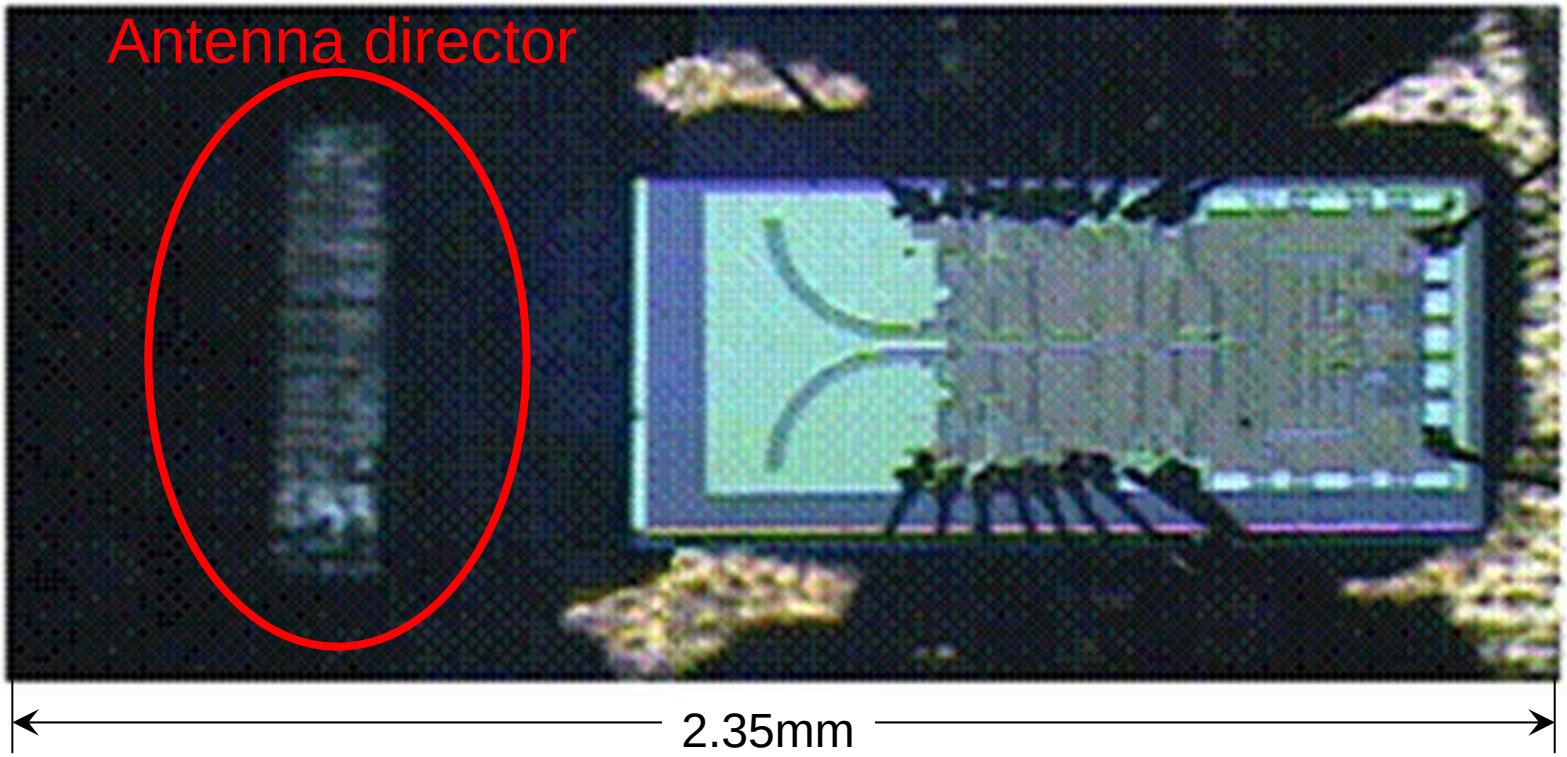


Without antenna director



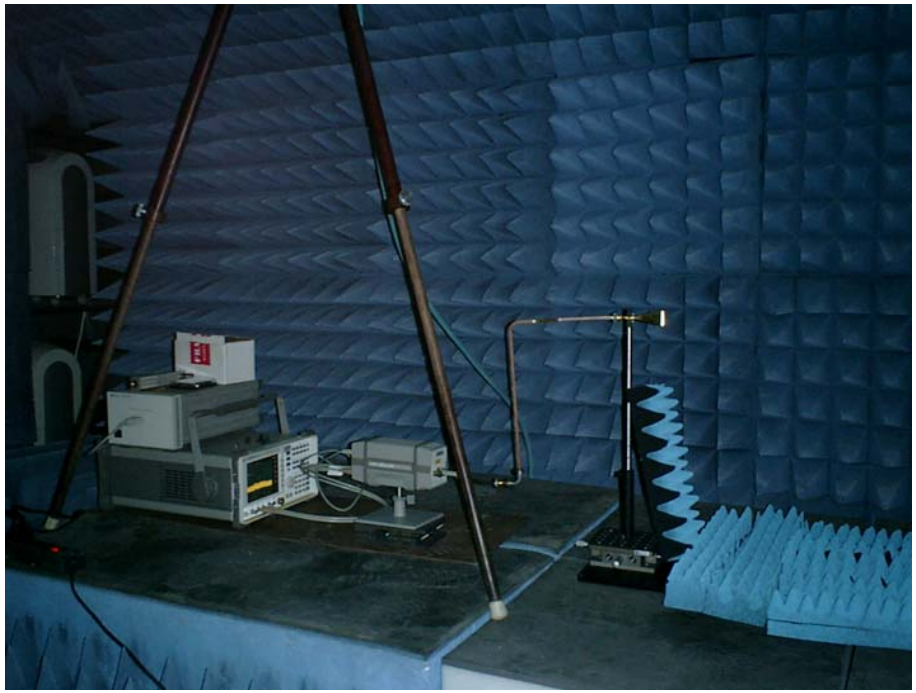
- E field mostly confined at surface
- Antenna gain increased: -10 dBi → 0 dBi (simulated)
- Results in narrow bandwidth

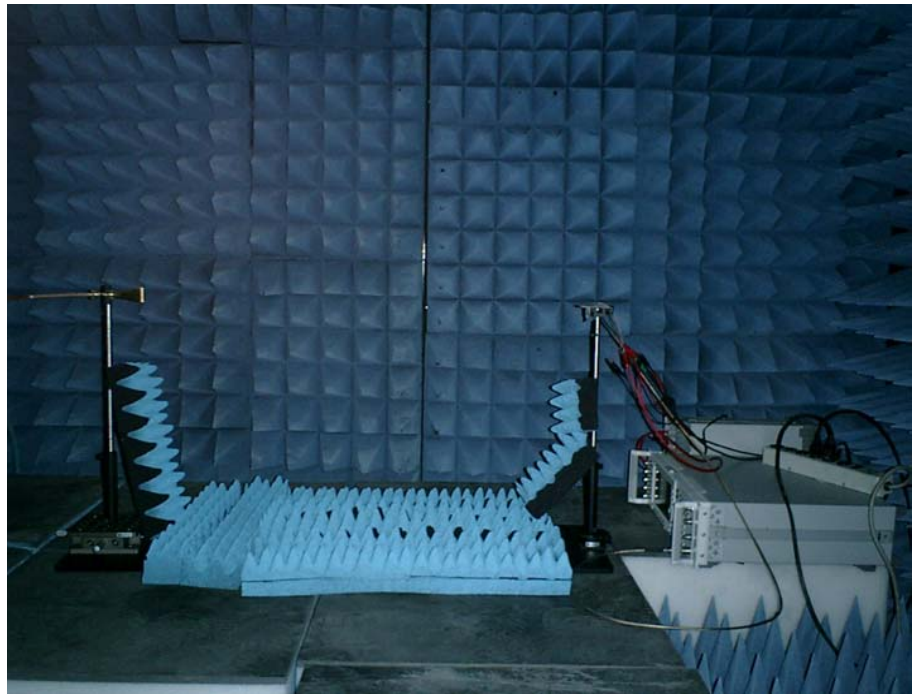
60GHz Transmitter Module



- Antenna director fabricated using Duroid 5880
- Director placed at ~ half wavelength (at 60 GHz) away from taper-slot antenna

Measurement Setup

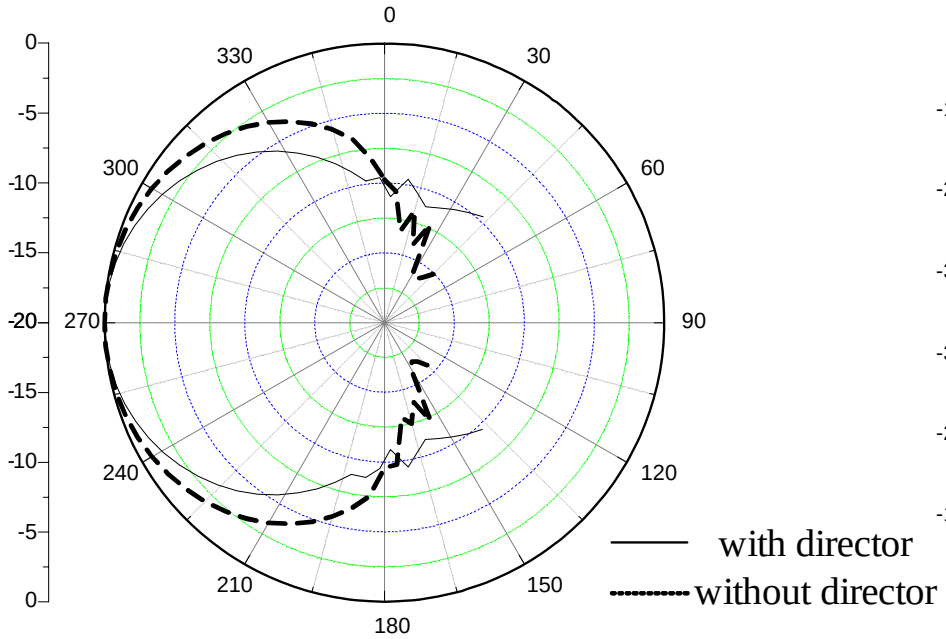




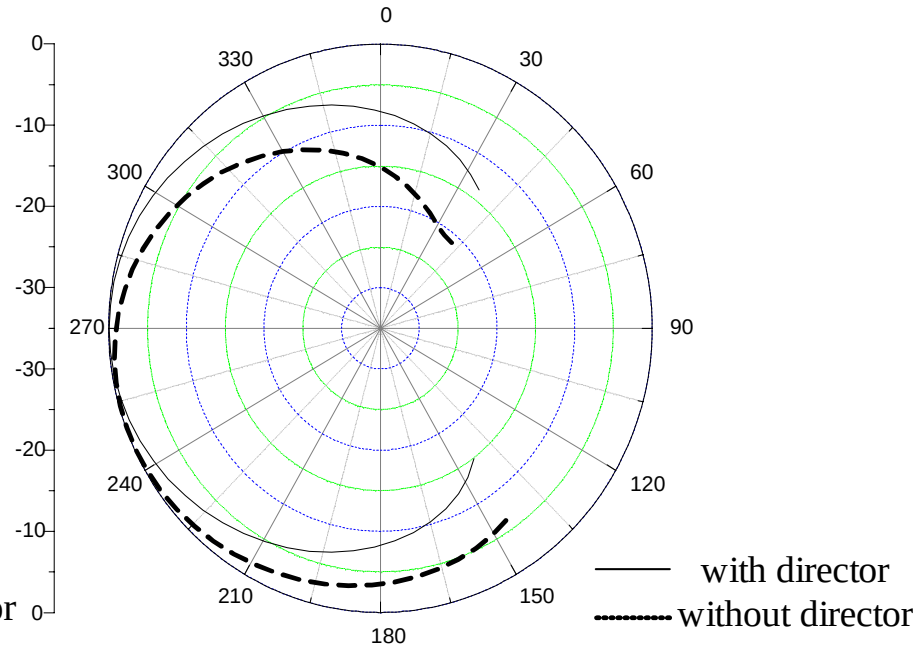
- Transmitted IF signal generated using Agilent E4438C
- Receiver consists of
  - Standard horn antenna with 24dB gain
  - Agilent 8565EC spectrum analyzer
  - Agilent 11974V pre-selection harmonic mixer

Radiation Pattern

E-plan (co-polar)



H-plan (co-polar)



- Antenna gain improved by off-chip director
- Taper-slot antenna gain ~ -2 dBi with director
  ~ -15 dBi without director
- SSB isotropic conversion gain ~ 20.2 dB

Summary

- The mmW CMOS modulator/LNA/mixer/VCO are presented.
- A mmW CMOS broadband/compact (low-cost) direct-conversion digital transmitter is demonstrated. The 60-GHz CMOS transceiver is under development.
- A 60-GHz SiGe HBT transmitter with integrated antenna is measured with gain enhancement techniques.

Thank you!