Project: IEEE P802.15 Study Group for Wireless Personal Area Networks (WPANs)

Submission Title:	PSSS proposal – Parallel reuse of 2.4 GHz PHY for the sub-1-GHz bands
Date Submitted:	**3nd** May 2005
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Re:	PSSS mode for more even chiprates, simpler filter, and 250 kbit/s in 868 MHz and new less complex preamble.
Abstract:	Ballot comments received indicated interest in the TG4b task group to modify the PSSS mode for 868 MHz to have the same 250 kbit/s bitrate as the 2.4 GHz and the PSSS 915 Mhz modes. Offering also simpler preamble.
Purpose:	Response to ballot comments to discuss potential modifcation of PSSS draft specification
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Highlights of Proposed Changes

- PSSS 250-400
  - Increases data rate from 200 kbps to 250kps
  - Reduces chip rate from 440 kcps to 400 kcps
  - Increases number of sequences from 15 to 20
  - Changes shift between sequences from 4 sub-chips to 3 sub-chips
  - Reduces pulse shaping filter requirement

- New preamble
  - Uses PSSS code 0 instead of Barker sequence
    - Allows reuse of HW for sync.
  - 32 chip vs Barker seq. length of 26
  - Repeated 4 times for 868 MHz and 16 times for 915 MHz
    - Equal time of 320 μs for both

- New SFD
  - Uses code 0 inverted one time
    - Allows reuse of HW for detection

Discussion: 250 kbit/s PSSS for 868 MHz

Key Considerations

- Comments indicated interest in the TG4b task group to provide 250 kbit/s for bot 868 and 915 MHz
  - Marketing benefit of having homogenous bit rate in all bands
- Discussion of implementation complexity due to uneven chip rates
  - Clarifications from chip vendors have shown that 440 kcps is not truly a concern – will not increase implementation size
  - Simply changing to 400 kcps rate in current PSSS specification is not attractive due to bitrate < 200 kbit/s (OEM concern)
  - Modifiation of PSSS mode to 400 kcps rate at 250 kbit/s possible
- Modified PSSS mode for 250 kbit/s in 868 MHz will even decrease filter complexity
  - Implementation complexity on Tx side[1] (of both COBI and PSSS) is clearly driven by compliance to ETSI PSD mask in 868 MHz

1: Key driver for implementation complexity on Rx side is need to withstand interference (dynamic range, linearity of Rx frontend)

The PSSS mode for 868 MHz could be modified to 250 kbit/s while even *decreasing* implementation complexity

	PSSS 206-440[1] 868 Mhz	**PSSS 250-400[1] 868 Mhz**	**PSSS 250-1600 915 MHz**
Bandwidth	600 kHz	600 kHz	2,400 kHz[2]
Chiprate	440 cps	400 cps	1,6000 cps[2]
Bitrate	206 kit/s	250 kit/s	250 kbit/s
Spectral efficiency[3]	15/32 bit/s/Hz	20/32 bit/s/Hz	5/32 bit/s/Hz
Spreading	15x 32-chip seq.	20x 32-chip seq.	5x 32-chip seq.
RF backward compatibility	Single BPSK / ASK radio	Single BPSK / ASK radio	Single BPSK/ASK radio
Comments	*Original PSSS mode*	*Enhanced original PSSS mode*	

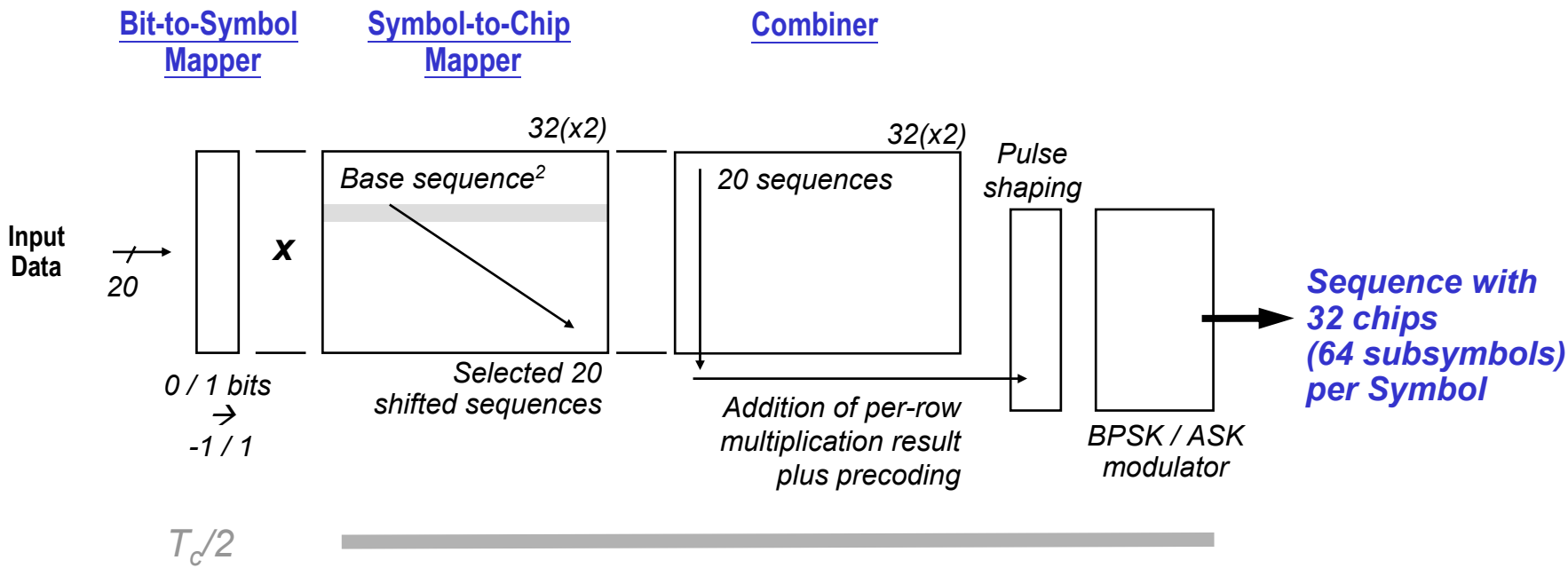
1: Changed names of modes to be consistent <bit rate>"-"<chip rate>
2: Complies to 915 MHz PSD mask specified in IEEE802.15.4-2003
$|f-f_c|$ > 1.2 Mhz: Relative limit -20 dB; Absolute limit -20 dBm
2: Coding level

PSSS 250-400 868 MHz Coding Table: Shifting of sequences by 3 instead of 4 subchips enables addition of sequences to achieve 250 kbit/s and 400 kcps

Sequence number	Chip number																															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1
1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1
2	-1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1
3	-1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1
4	-1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	
5	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1
6	-1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	
7	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1
8	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	
9	-1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1
10	-1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	
11	-1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1
12	-1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	
13	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1
14	-1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	
15	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1
16	-1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	
17	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1
18	-1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	
19	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1
	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64																															
	Subchip number																															

- *2 sub-chips per chip – basic chip rate of coding scheme is unchanged*
- *Addition per sub-chip for multivalue encoding – no other changes of PSSS model*

No modification of the basic PSSS model: PSSS 250-400 868 MHz – BPSK/ASK (20/32 bit/s/Hz)



- ***No increase of Tx complexity in real-world implementation –***
  - Oversampling used for baseband filtering to achieve PSD compliance anyhow
  - No change in number of chips per symbol – no increase in coding table sizes
- ***Simpler baseband filter sufficient due to lower chiprate, see PSD at Appendix.***
- ***No change in Rx processing required***
- ***Similar performance, see Appendix.***

Signal Flow

- The preamble (eight times repeated c_0) and the SFD (one time inverted c_0), are BPSK modulated.
- The Phy header and PHY payload are PSSS encoded and ASK modulated.
- Both signals have same chip duration and passes same pulse shaping.

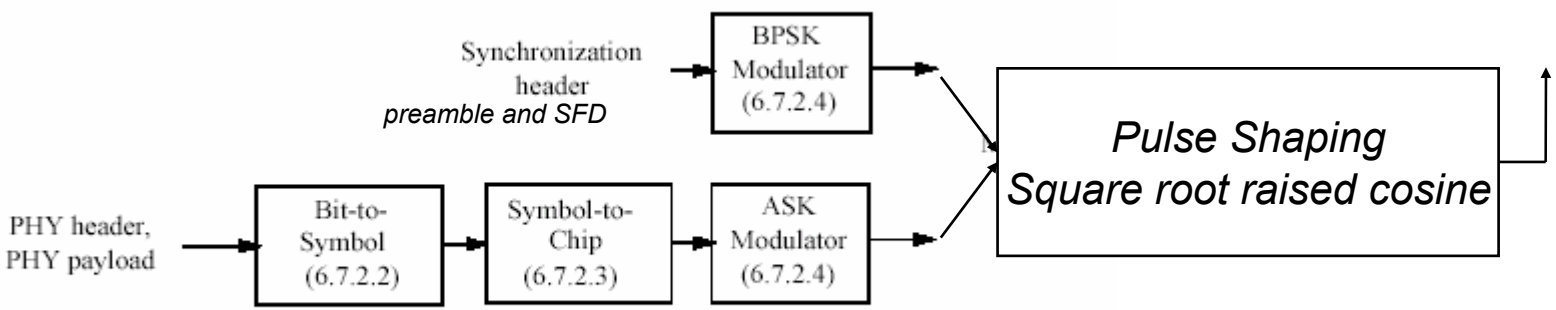


Figure 22—Modulation and spreading functions

PSSS Codes form Coding Table in Draft Standard for Preamble

- We propose to use Sequence 0 = c_0, 4/16 times repeated for 868/915 MHz, instead of the barker code.
- Preamble will then be more similar to the other Phys.

Table 27—PSSS Code table used in Symbol-to-Chip mapping for 868 MHz

Sequence number	Chip number																														
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1
1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1
2	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1
3	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1
4	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1
5	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	1	1
6	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1
7	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1
8	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1
9	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1
10	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1
11	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1
12	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1
13	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1
14	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1

Comparision Actual/New Proposed Preamble Length of Proposed Preamble

	Barker Code	Sequence 0
DC free	**yes**	**yes**
32 Chip long	**no**	**yes**
# of needed FIR in Rx	**2**	**1**

- The Sequence 0 is repeated 4/16 times for 868/915 MHz. Same duration of 320µs for both preambles.

	Code length	# of codes	# of repeating	preamble # of chips
Barker Code	**13**	**2**	**8**	**208**
Sequence 0 for 868 MHz	**32**	**1**	**4**	**128**
Sequence 0 for 915 MHz	**32**	**1**	**16**	**512**

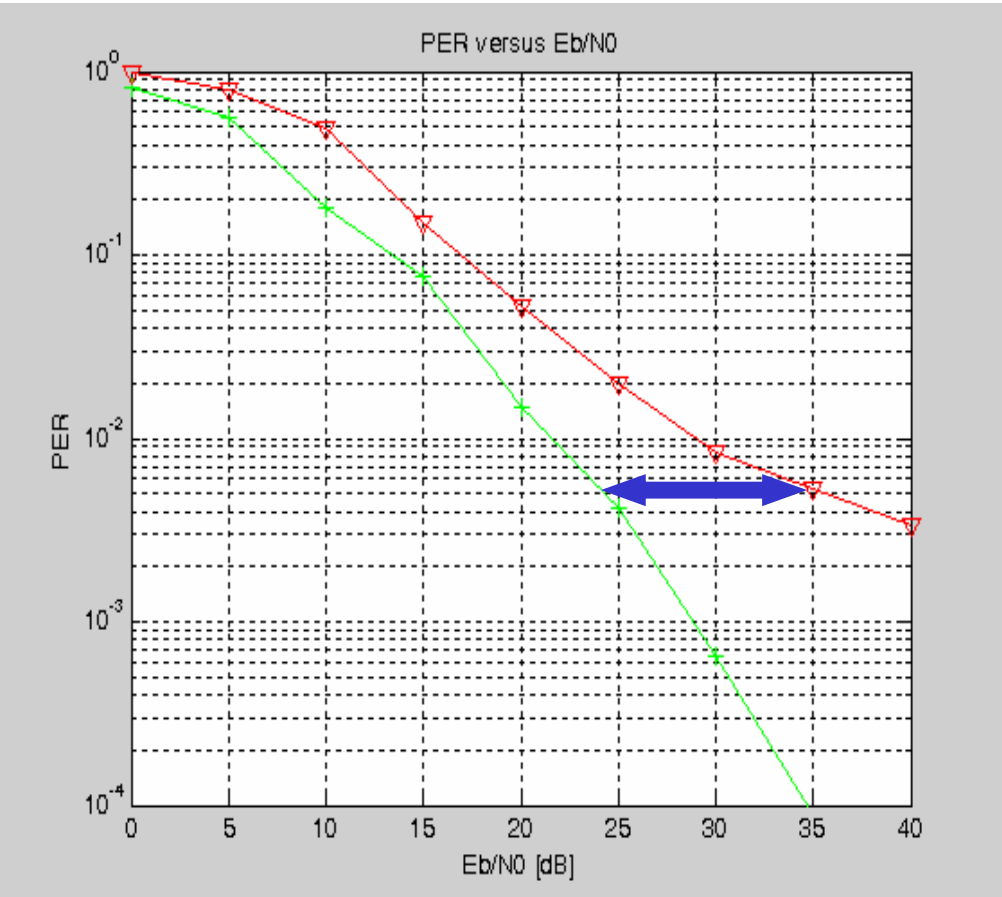
Summary

- We propose to use PSSS 250-400 instead of PSSS 206-440 for ETSI.
- We propose also to use the new preamble base on Sequence C_0 for similar design compared to the other Phys.

Appendix

- PER versus E_b/N_0 PSSS 206-440
- PER versus E_b/N_0 PSSS 250-400
- PSD PSSS 250-400
- Correlative detection of current Barker code based preamble
- Correlative detection of new proposed preamble

PER Performance PSSS 206-440 868 MHz (BPSK/ASK) – Discrete Exponential Channel, 250ns RMS Delay Spread

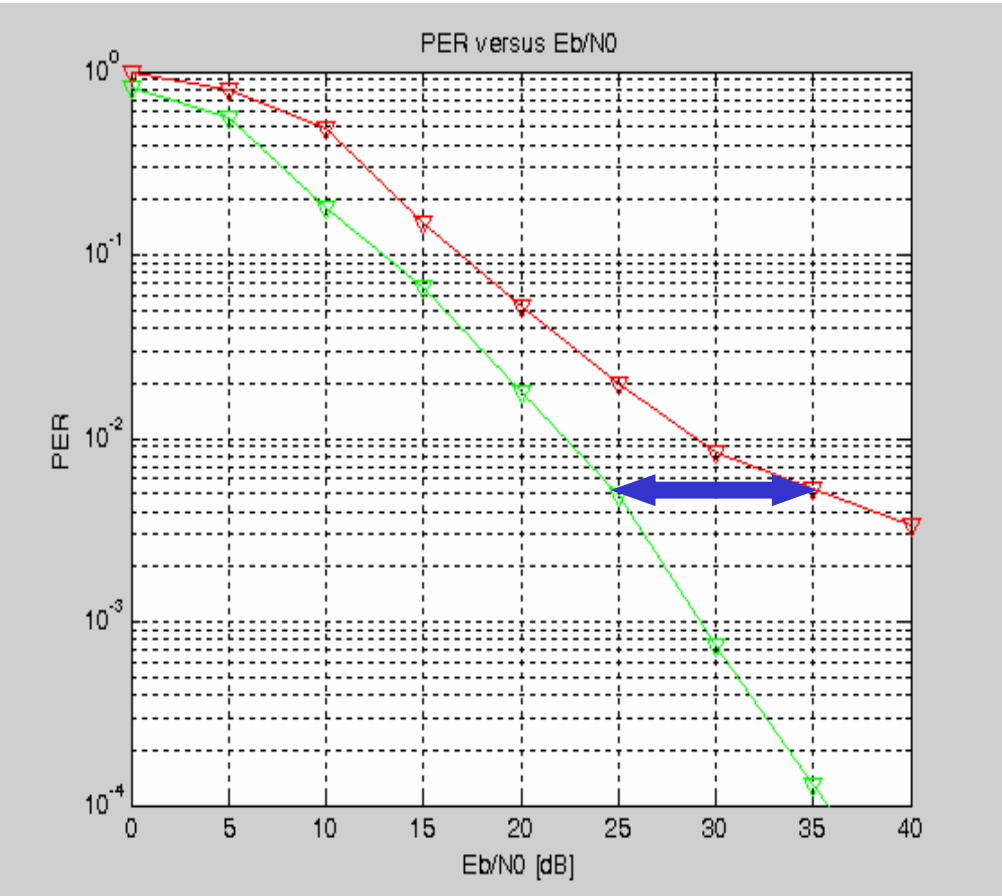


Comparison to COBI:

- Over 11 dB performance benefit over COBI16+1
  - Expected even higher performance benefit against COBI16
- Estimated 15-18 dB performance benefit over COBI8
  - Little if any performance benefit over 868MHz FSK chips for COBI8

– PSSS 206 kbit/s – COBI16+1 235 kbit/s *> 10000 Channel, no Rake receivers*

PER Performance PSSS 250-400 868 MHz (BPSK/ASK) – Discrete Exponential Channel, 250ns RMS Delay Spread

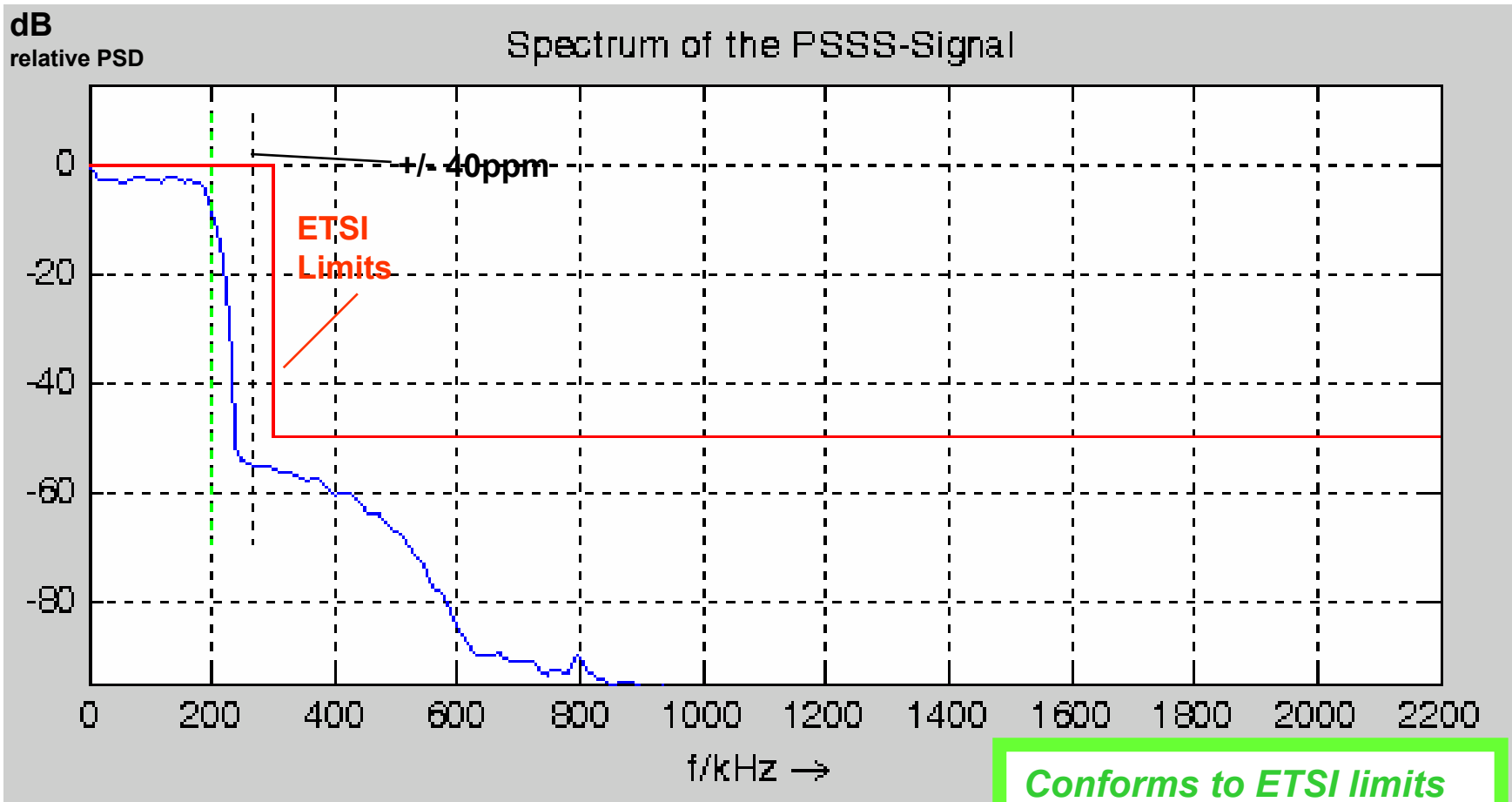


Comparison to PSSS 206-440 868 MHz

- No visible degradation of performance

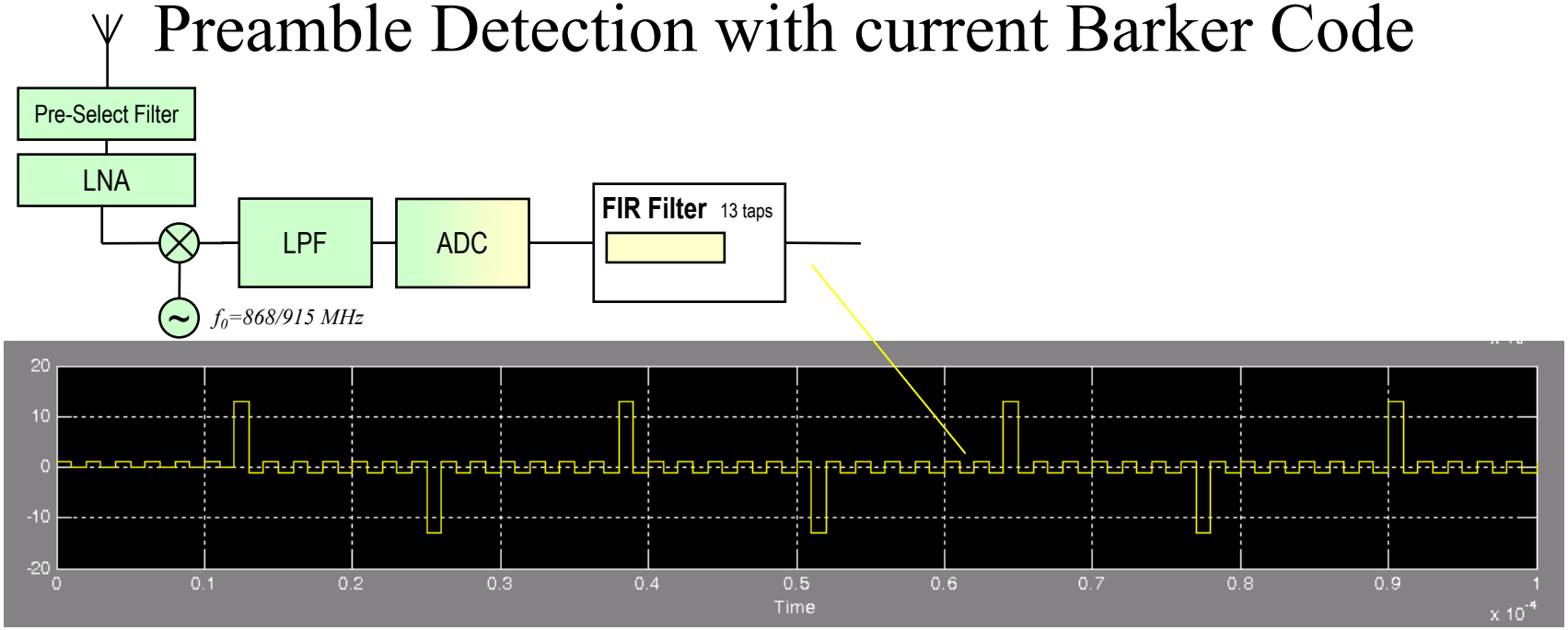
– PSSS 250 kbit/s – COBI16+1 235 kbit/s *> 10000 Channel, no Rake receivers*

PSD for PSSS 250-400 868 MHz (in 600 KHz channel) Baseband pulse shaping non-linear "Real World PA"



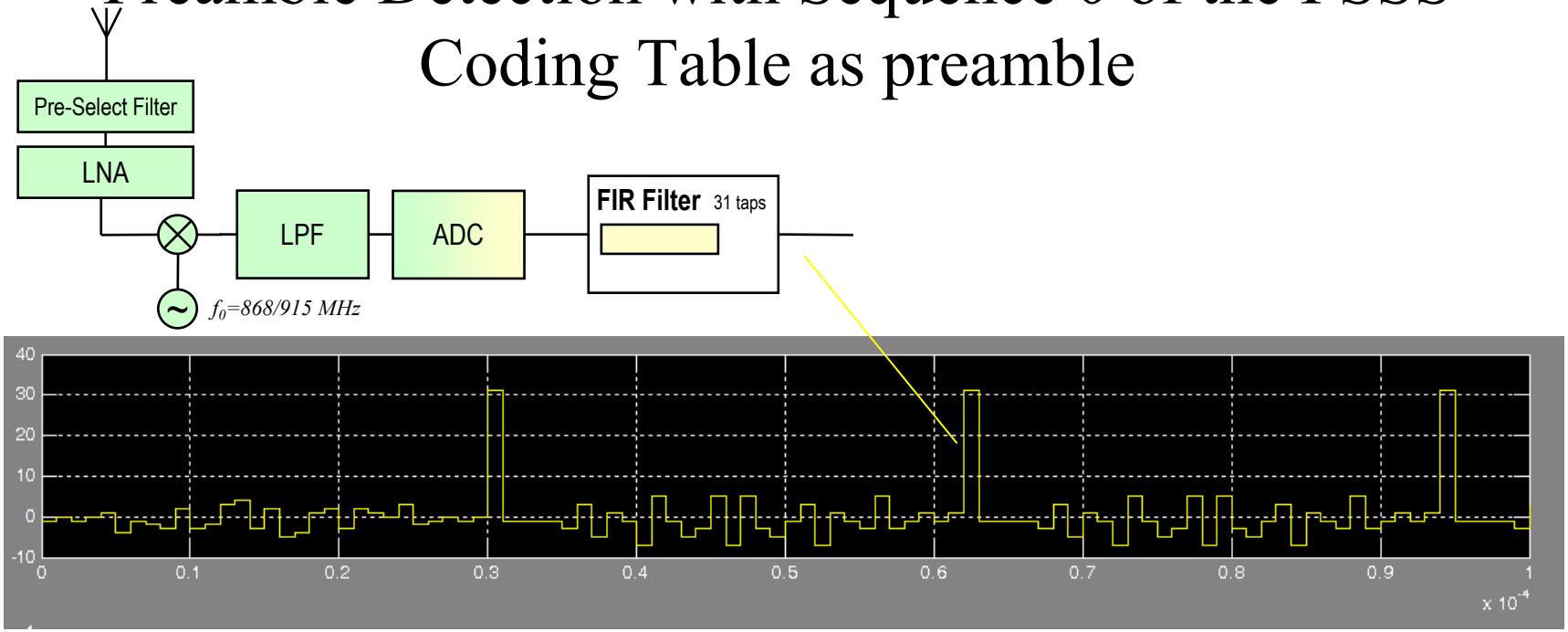
Simulations of the relative PSD in dB for the PSSS 250-400 signal: With precoding, at 400 kchip/s, 250 kbit/s, +/- 40ppm, 50% PA drive, square root raised cosine filter with r = 0.2

Preamble Detection with current Barker Code



- When detecting the current barker code based preamble with FIR filter, the signal coming out of the FIR filter has side slopes limited to +/- 1.
- Advantages:
  - DC free
- Disadvantages:
  - **Two FIR filters needed**, one for preamble detection (13 chip barker code), one for PSSS decoding (31 chip m-sequence).
  - **Not multiple of symbol duration**

Preamble Detection with Sequence 0 of the PSSS Coding Table as preamble



- When detecting the preamble, base on repeated sequence 0 with FIR filter, the signal coming out of the FIR filter has side slopes limited to +5/-6.
- Advantages:
  - Use of just one FIR filter or correlator for preamble detection and PSSS decoding.
  - **32 chip long preamble code.= multiple of symbol duration and similar to other phys**.
  - DC free