Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: [DBO-CSK Proposal for IEEE802.15.4a]
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Re: [Response to Call for Proposal by IEEE802.15.4a]

Abstract: [This document has been submitted for an official proposal in January 2005. DBO-CSK Technology is proposed]

Purpose: [Proposal for the IEEE802.15.4a standard]

Differentially Bi-Orthogonal Chirp-Shift-Keying (DBO-CSK)

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Orthotron Co., Ltd.

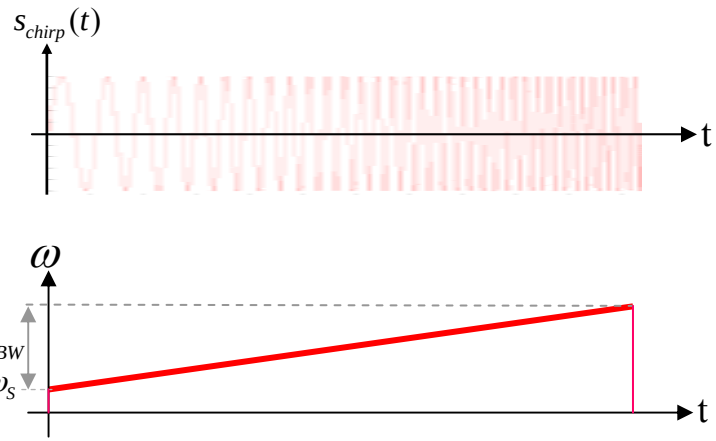
CONTENTS

1. INTRODUCTION

- **Low Power Consumption:** Digital Tx 0.65mW, Rx 61.6mW
- **Signal Robustness:**
  - Orthogonal / Quasi-Orthogonal Signal Set
  - Robustness: Heavy Multi-path, SOP,
  - Low Correlation with Existing Air-Interfaces
- **Feasibility:** 2.4GHz ISM Band
  - Existing commercial RF Solutions
- **Ranging:** Based on Chirp Signal (TDOA)
  - Precision: less then 1 m @ Eb/No > 22dB (Standard Deviation)
- **Size & Form Factor:** Less than SD-Memory size
- **Low Cost / Low Complexity:** Tx + Rx Baseband Digital (54K gates)
- **Advanced Sleep/Wake-up Capability**

2. M-ary DBO-CSK TECHNOLOGY

Chirp Signal

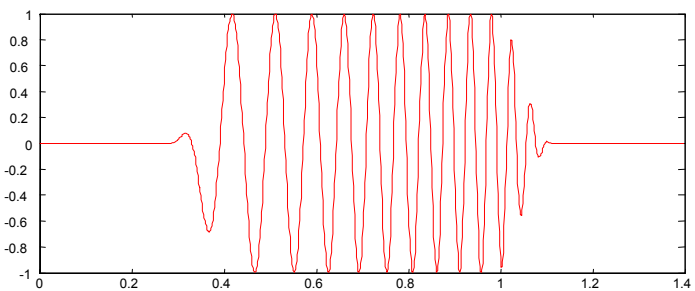


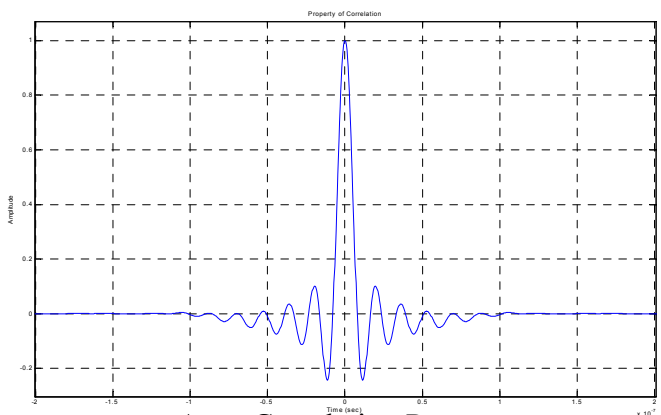
Linear Chirp: Rectangular Window

$$s_{chirp}(t) = \mathrm{Re}\left[\exp[(\omega_s + \frac{\omega_{BW}}{2T_{chirp}} t)t + \theta_0] \times [u(t) - u(t - T_{chirp})] \right]$$

Linear Chirp: Raised-Cosine Window

$$s_{chirp}(t) = \mathrm{Re}\left[\exp[(\omega_s + \frac{\omega_{BW}}{2T_{chirp}} t)t + \theta_0] \times p_{RC}(t - T_{chirp}) \right]$$

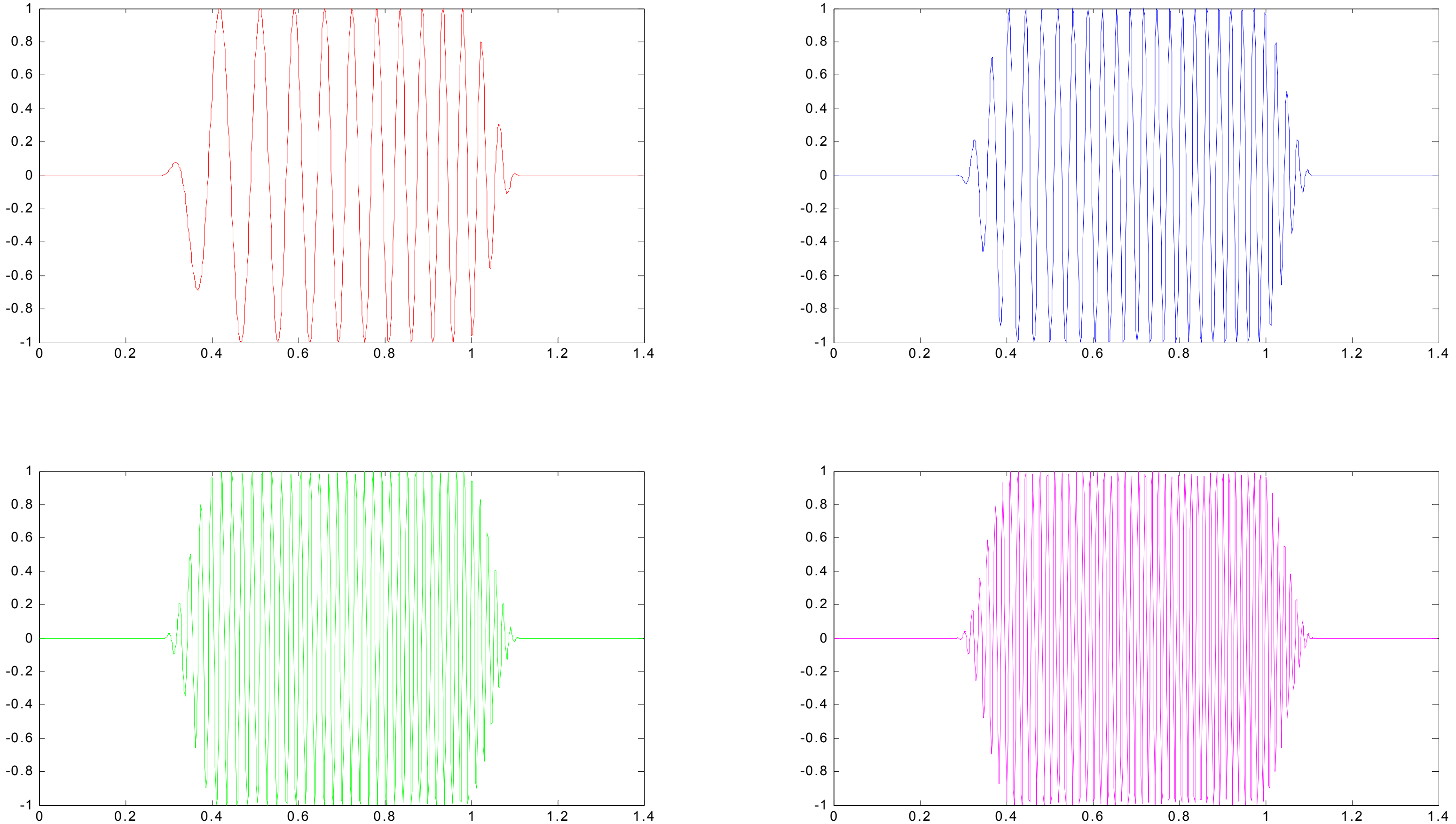




Auto-Correlation Property

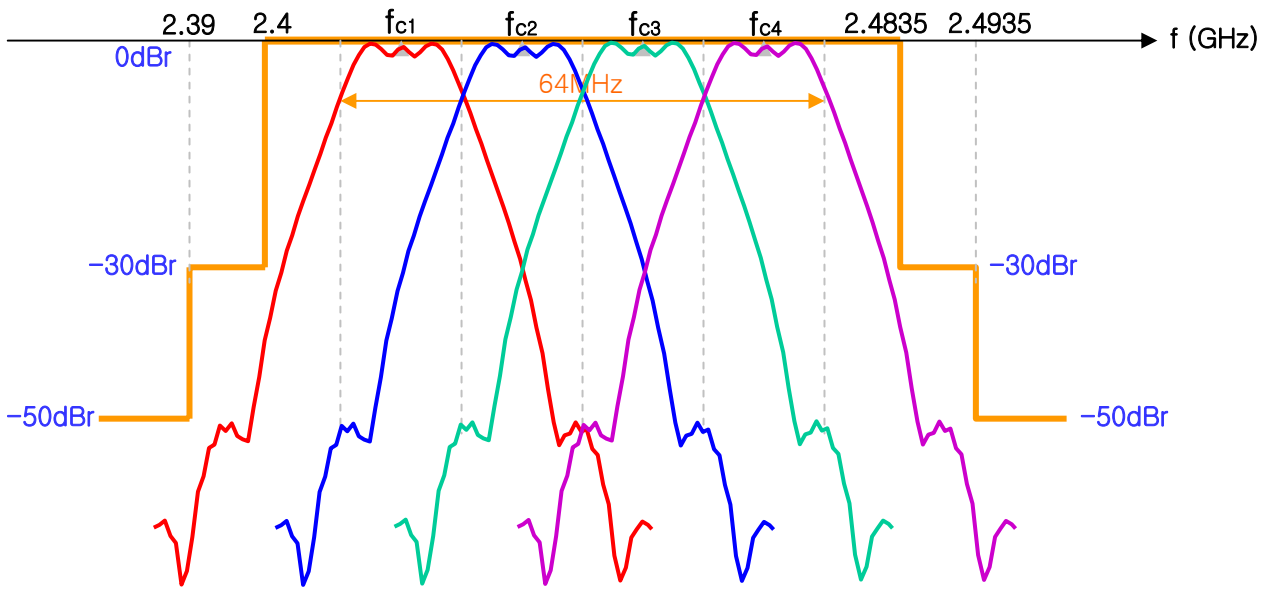
2. M-ary DBO-CSK TECHNOLOGY

Waveform of Chirp-Shift-Keying (CSK) Signals



2. M-ary DBO-CSK TECHNOLOGY

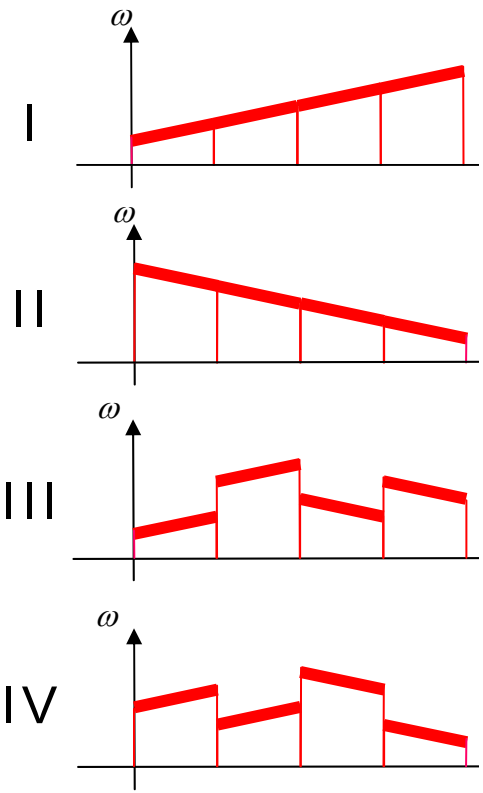
Spectrum of Sub-Chirp Signals

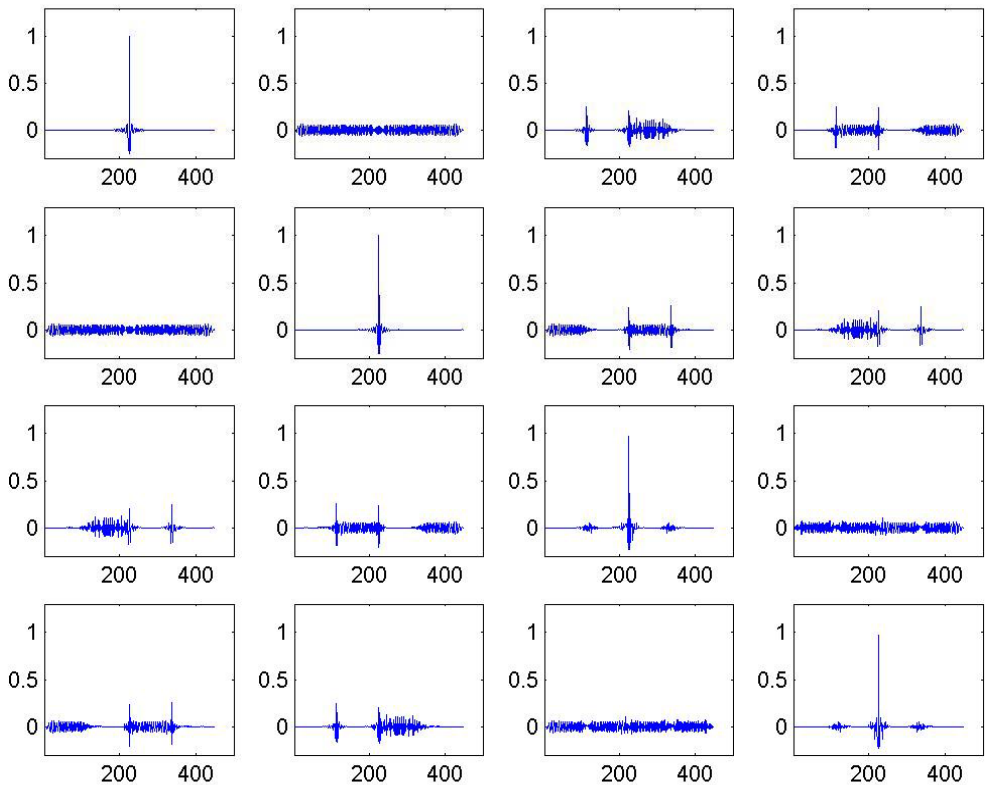


f_{C1} = 2.41775GHz
f_{C2} = 2.43375GHz
f_{C3} = 2.44975GHz
f_{C4} = 2.46575GHz

2. M-ary DBO-CSK TECHNOLOGY

Chirp-Shift-Keying (CSK) Signal sets for SOP





Each of CSK Signal consists of 4 sub-chirp signals.

Correlation Property between different Chirp-signals

2. M-ary DBO-CSK TECHNOLOGY

Bi-Orthogonal Modulation

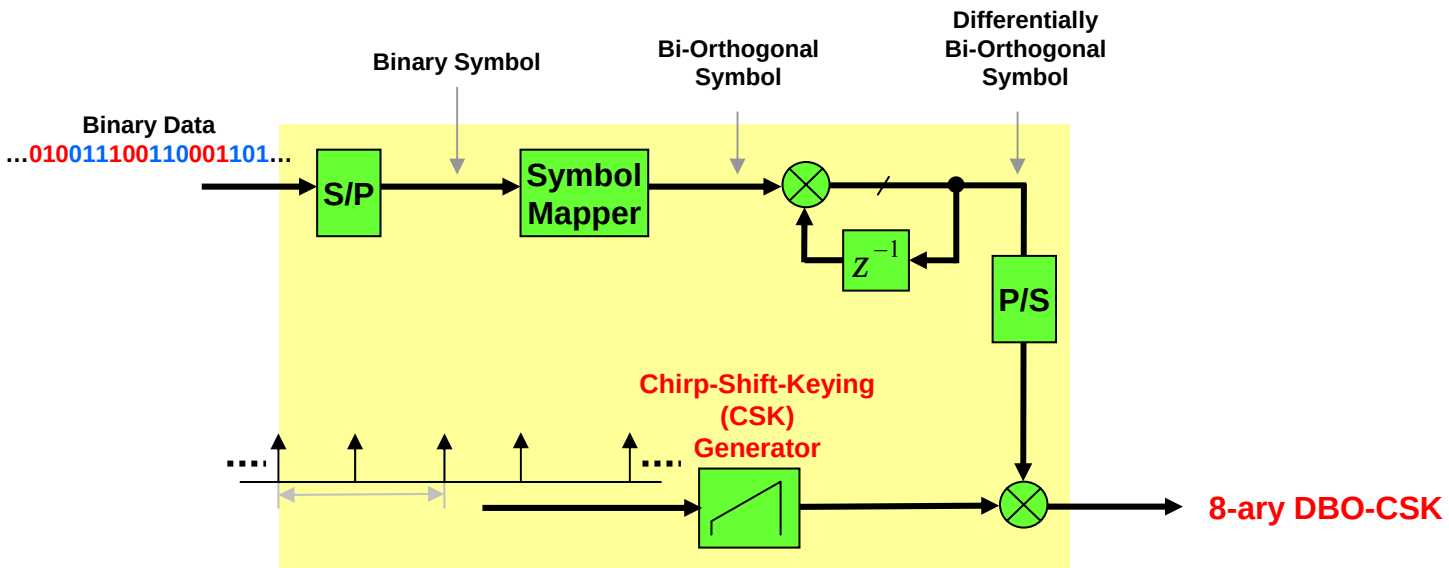
Bi-Orthogonal Symbol Mapping Table (M = 8)

Decimal (m)	Binary (b0,b1,b2)	Bi-Orthogonal Code (01,02,03,04)
0	000	1 1 1 1
1	001	1 -1 1 -1
2	010	1 1 -1 -1
3	011	1 -1 -1 1
4	100	-1 -1 -1 -1
5	101	-1 1 -1 1
6	110	-1 -1 1 1
7	111	-1 1 1 -1

3 bits/symbol

2. M-ary DBO-CSK TECHNOLOGY

8-ary Differentially Bi-Orthogonal Chirp-Shift-Keying(DBO-CSK) Modulator



3. GENERAL SOLUTION CRITERIA

3.1. Unit Manufacturing Cost/Complexity (UMC)

- **Transmitter Baseband ≤ 3k gates**
  - Scrambler : 15bit register and 1bit XOR => 154 gates
  - Block Encoder : 300 gates
  - 1X3 S/P and 4X1 P/S : 2bit register and 3bit register => 50 gates
  - Symbol Mapper : 3X8 address decoder with hard-wire table => 13 gates
  - Differential Encoder : 4bit XOR and 4bit register => 56 gates
  - Chirp-pulse Modulator : eight 6X56 address decoder with hard-wire table and four 4bit adder => 1680 gates
  - Other blocks : 700 gates

- **Receiver Baseband ≤ 51k gates**
  - Differential Detector : 3240 registers, complex multiplier and four adders => 38960 gates
  - Symbol Demapper : (ten 1bit XORs + four 3bit adders) X 2 => 200 gates
  - Max Selector : 3bit two-step comparator X 2 => 54 gates
  - Two 1X4 S/P and one 3X1 P/S: 3bit register X 2 and 2bit register => 80 gates
  - Block Decoder : 3k gates
  - Descrambler : 15bit register (≈ 10 gates/register) and 1bit XOR => 154 gates
  - Other blocks : 7k gates

- **Analogue ≤ 5.6 mm^2 Die** (for 0.18 um library)

3. GENERAL SOLUTION CRITERIA

3.2. General Definitions

- **Payload bit rate and throughput**
  - 1Mbps throughput: 618Kbps
  - 250Kbps throughput: 216Kbps
- **Error rate:** see sub-section 5.6
- **Receiver sensitivity:** see sub-section 5.11
- **Antenna gain:** 0dBi
- **Band in use:**
  - 2.4GHz ISM Band
  - 64MHz Bandwidth: Consists of 4 sub-chirp signals

3. GENERAL SOLUTION CRITERIA

3.3. Signal Robustness

- **Co-existence / Interference Mitigation Technique**
  - Orthogonal / Quasi-Orthogonal Signal Set
  - High Spectral Processing Gain: Chirp
- **Interference Susceptibility**
  - Low Cross-Correlation property with Existing Signal
- **Robustness:**
  - Heavy Multi-path Environment
  - SOP
- **Low Sensitivity for Component Tolerance**
  - Crystal : ± 40ppm
- **Mobility**
  - Wide-band Chirp: Insensitive for Fading & Doppler Shift

3. GENERAL SOLUTION CRITERIA

3.4. Technical Feasibility

- **Manufacturability**
  - Baseband Digital Chip area: 0.7 mm^2 (0.18um Technology)

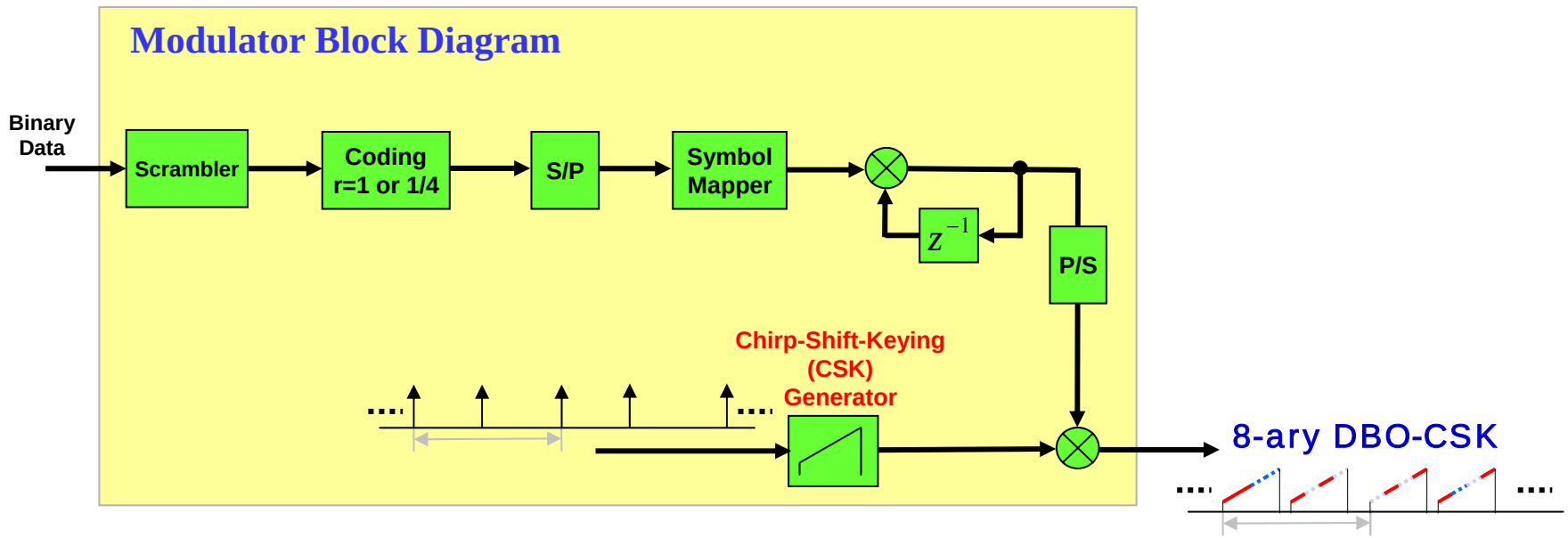
- **Time-to-Market**
  - 2005. 5. Proto-type DEMO (FPGA)
  - 2006. 1. Digital ASIC

- **Regulatory Impact**
  - 2.4GHz ISM Band: Globally Allowed to use
  - Tx Power: 0.1mW / 1.0mW / 10mW optional class
  - Some Critical Frequency Band within 2.4GHz: Can avoid Tx Power by Skip

3. GENERAL SOLUTION CRITERIA

3.4. Technical Feasibility

8-ary Differentially Bi-Orthogonal Chirp-Shift-Keying(DBO-CSK) Modulator



3. GENERAL SOLUTION CRITERIA

3.5. Scalability

- **Data-Rate:**
  - 2 rates: **1Mbps** or **250Kbps**
- **RF Tx Power:**
  - 3 classes: 0.1mW / 1.0mW / 10mW
- **Mobility Value:**
  - Data: Link Margin >= 30dB
  - Ranging: Preamble Duration is only less than 800usec
  - Chirp is insensitive for Doppler Shift
  - Can Moving High Speed:

4. MAC PROTOCOL SUPPLEMENT

4.1. MAC Enhancements and Modifications

- **Supplement for Scalability**
  - The proposed PHY has scalability for channelization
  - Scalability which is included in PHY should be added to MAC for 15.4a PHY layer (Ex. Data-rate Assignment per Packet)

- **Wake-up Mode for Power Consumption Consideration**
  - Power consumption is of significant concern
  - The proposed PHY can support ***advanced wake-up*** mode with superior SOP performance
  - Needing supplement to 15.4 MAC to advanced wake-up mode for low-power consumption

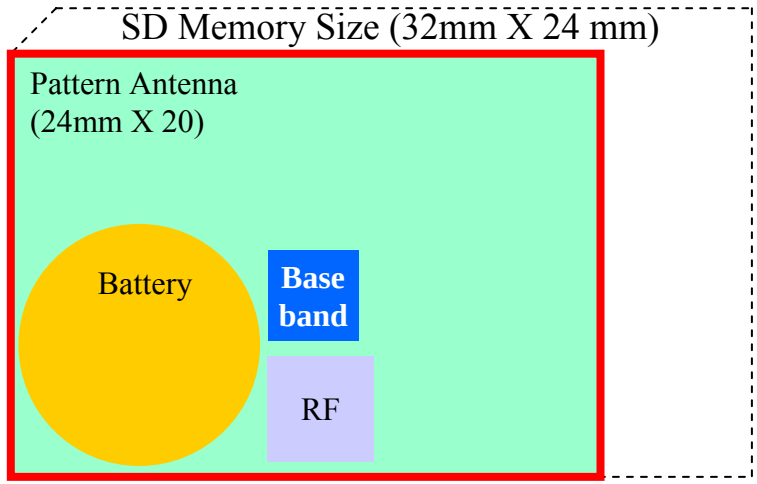
5. PHY LAYER CRITERIA

5.1. Channel models and payload data

- **Channel models and payload data**
  - CM1, CM2, & CM3
  - Payload Data: 32bytes per Packet
  - Data-rate: 1Mbps

5. PHY LAYER CRITERIA

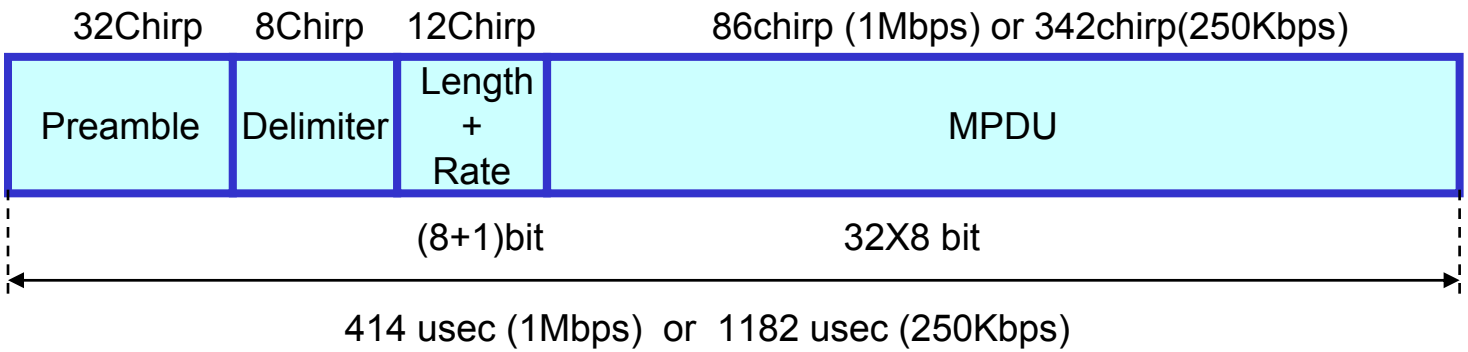
5.2. Size and Form Factor



5. PHY LAYER CRITERIA

5.3. PHY-SAP Payload Bit Rate and Data Throughput

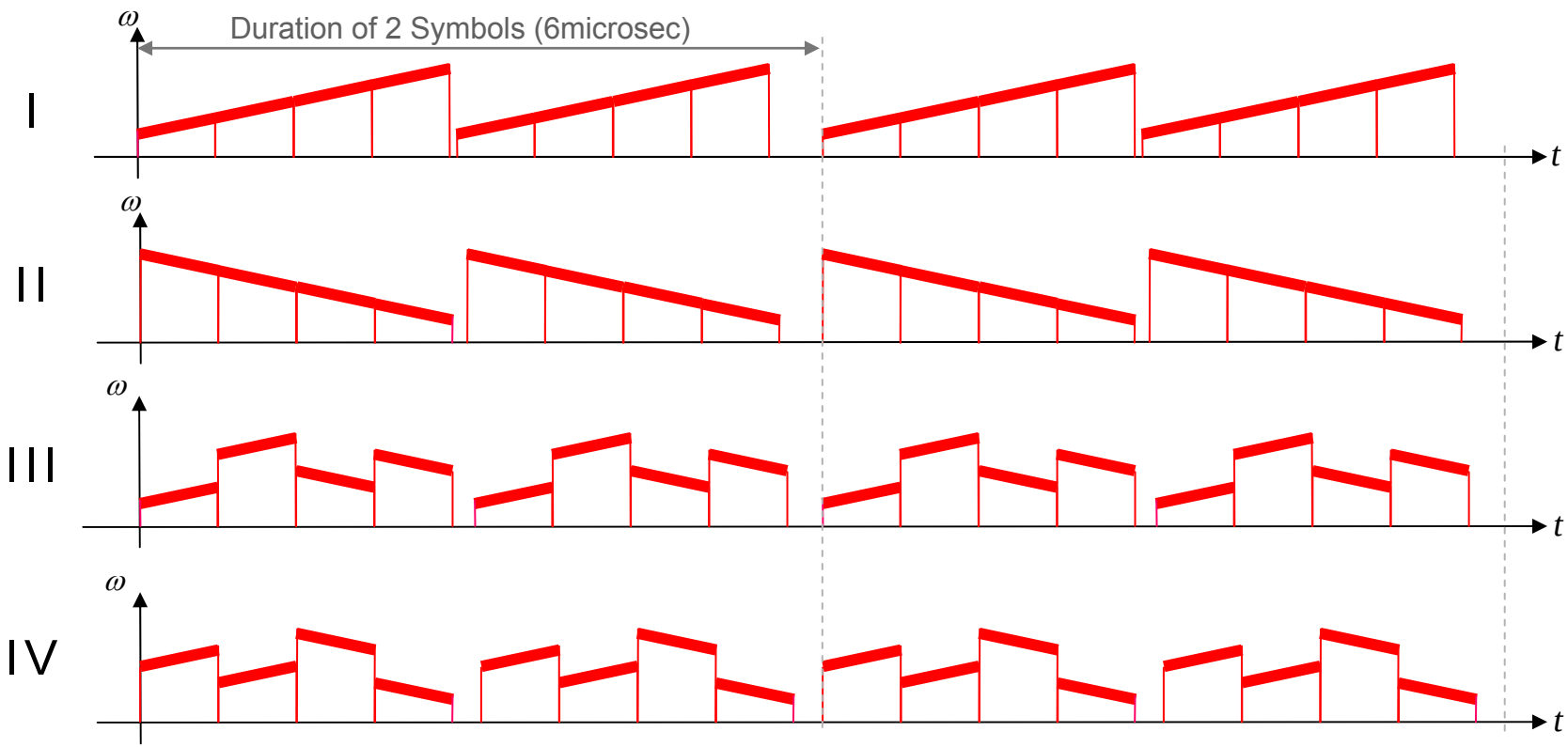
Payload bit-rate 1Mbps : Throughput 618 Kbps
Payload bit-rate 250Kbps: Throughput 216 Kbps



5. PHY LAYER CRITERIA

5.4. Simultaneously Operating Piconets

Multiple piconet

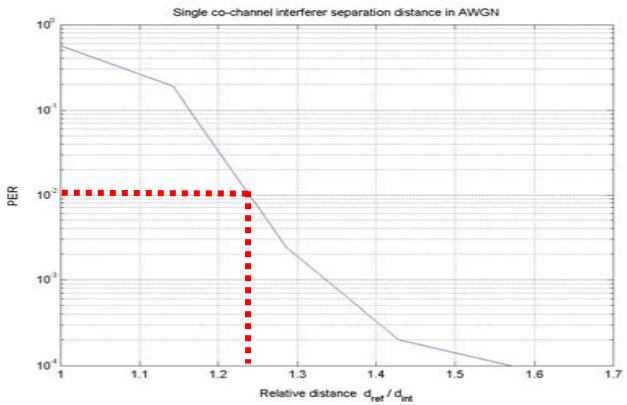


5. PHY LAYER CRITERIA

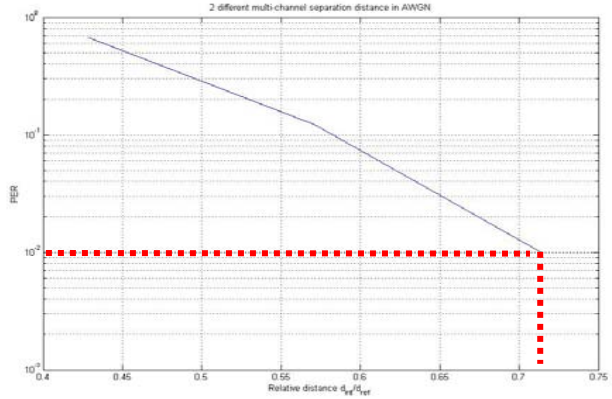
5.4. Simultaneously Operating Piconets

AWGN Channel

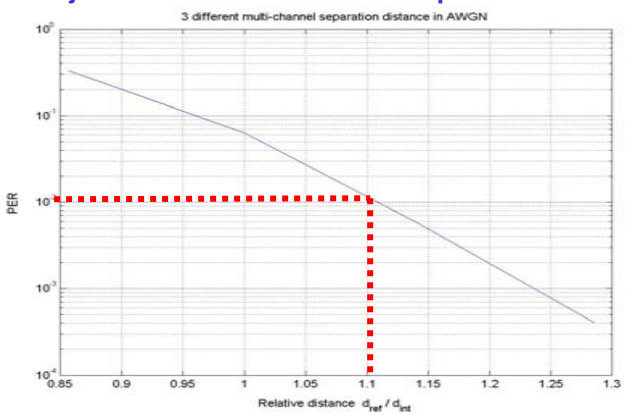
Single Co-Channel Interferer Separation Distance



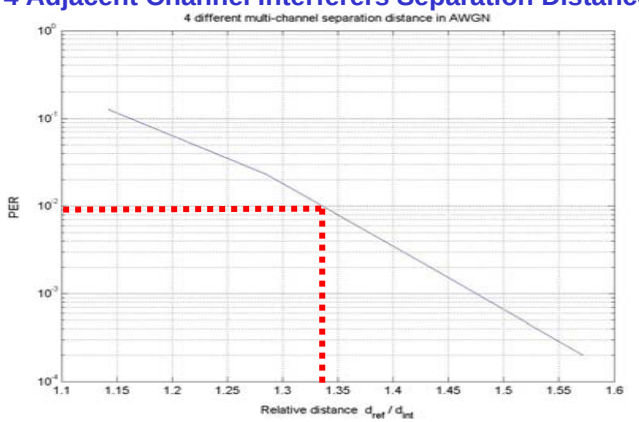
2 Adjacent Channel Interferers Separation Distance



3 Adjacent Channel Interferers Separation Distance



4 Adjacent Channel Interferers Separation Distance

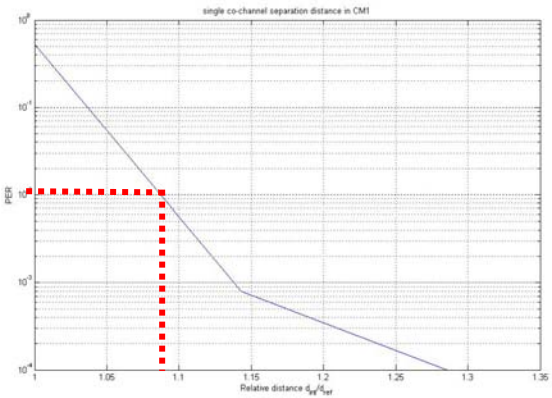


5. PHY LAYER CRITERIA

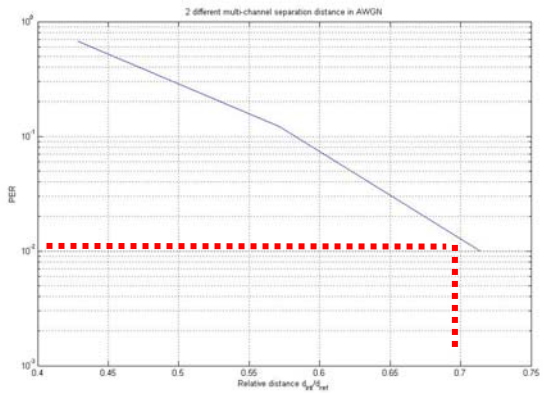
5.4. Simultaneously Operating Piconets

CM1

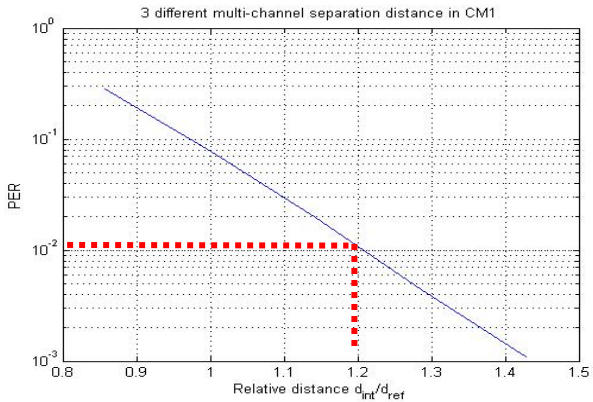
Single Co-Channel Interferer Separation Distance



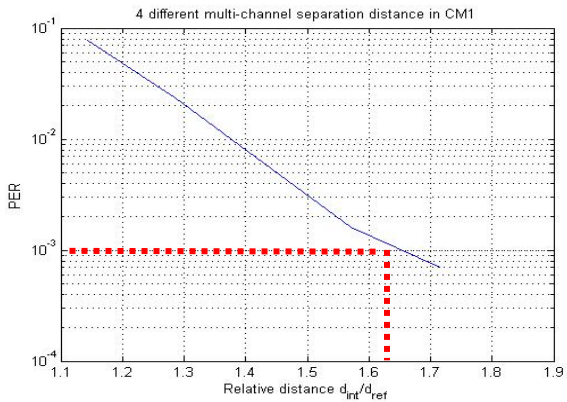
2 Adjacent Channel Interferers Separation Distance



3 Adjacent Channel Interferers Separation Distance



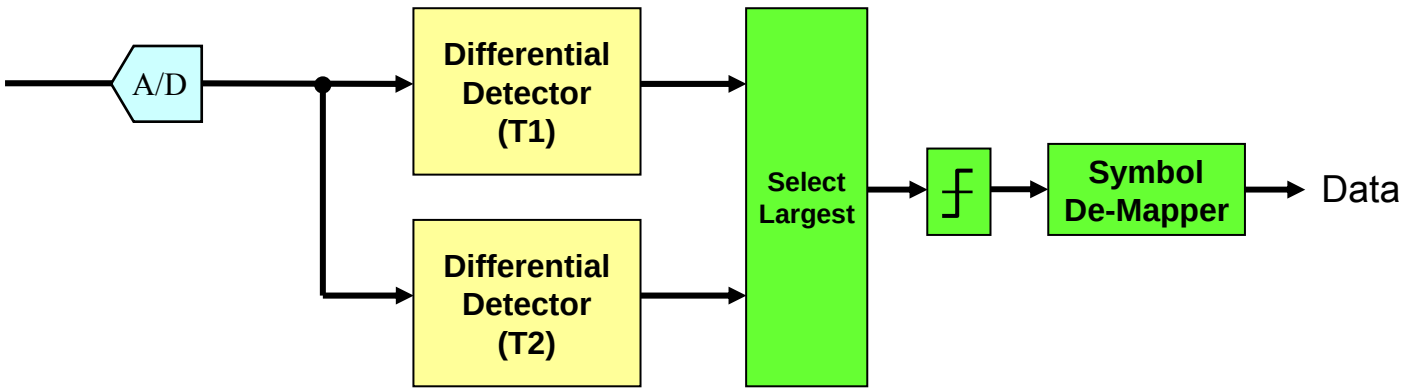
4 Adjacent Channel Interferers Separation Distance



5. PHY LAYER CRITERIA

5.5. Signal Acquisition

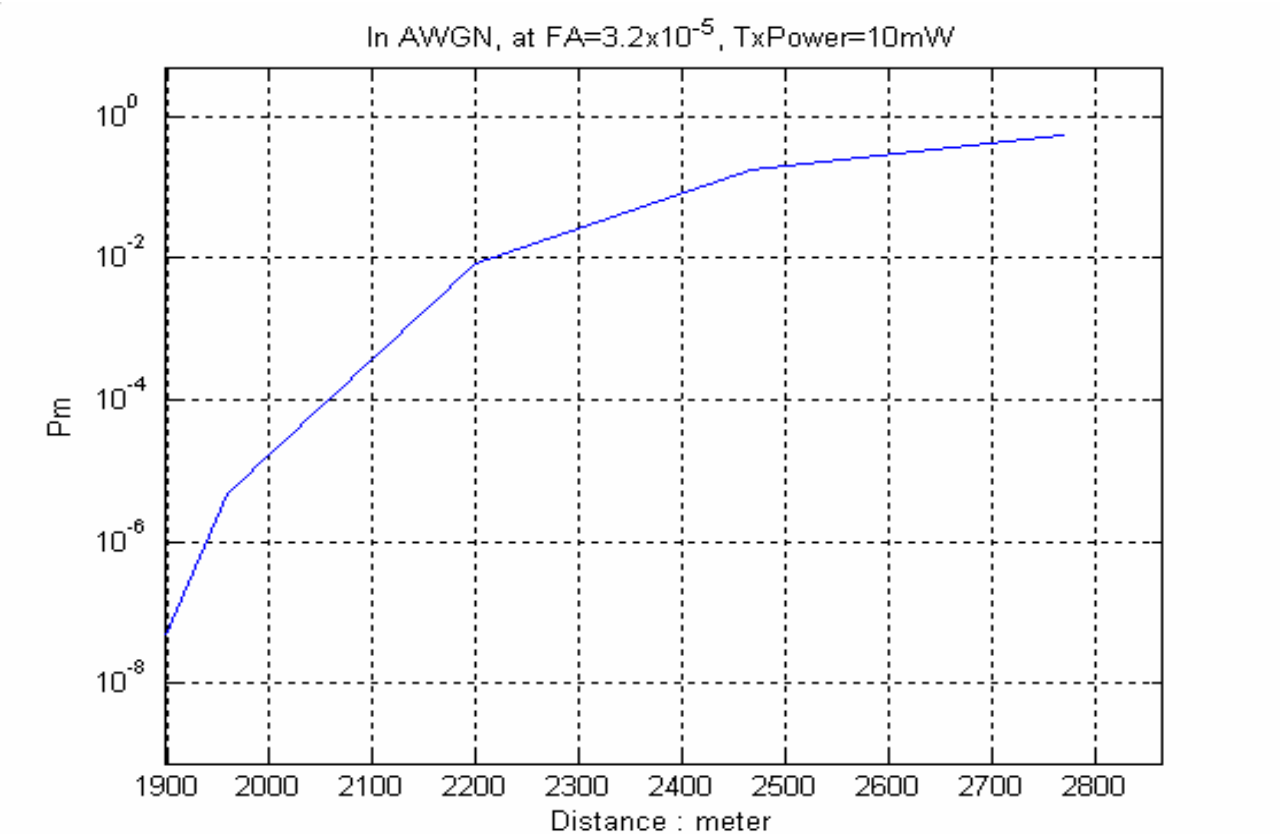
Signal Acquisition



5. PHY LAYER CRITERIA

5.5. Signal Acquisition

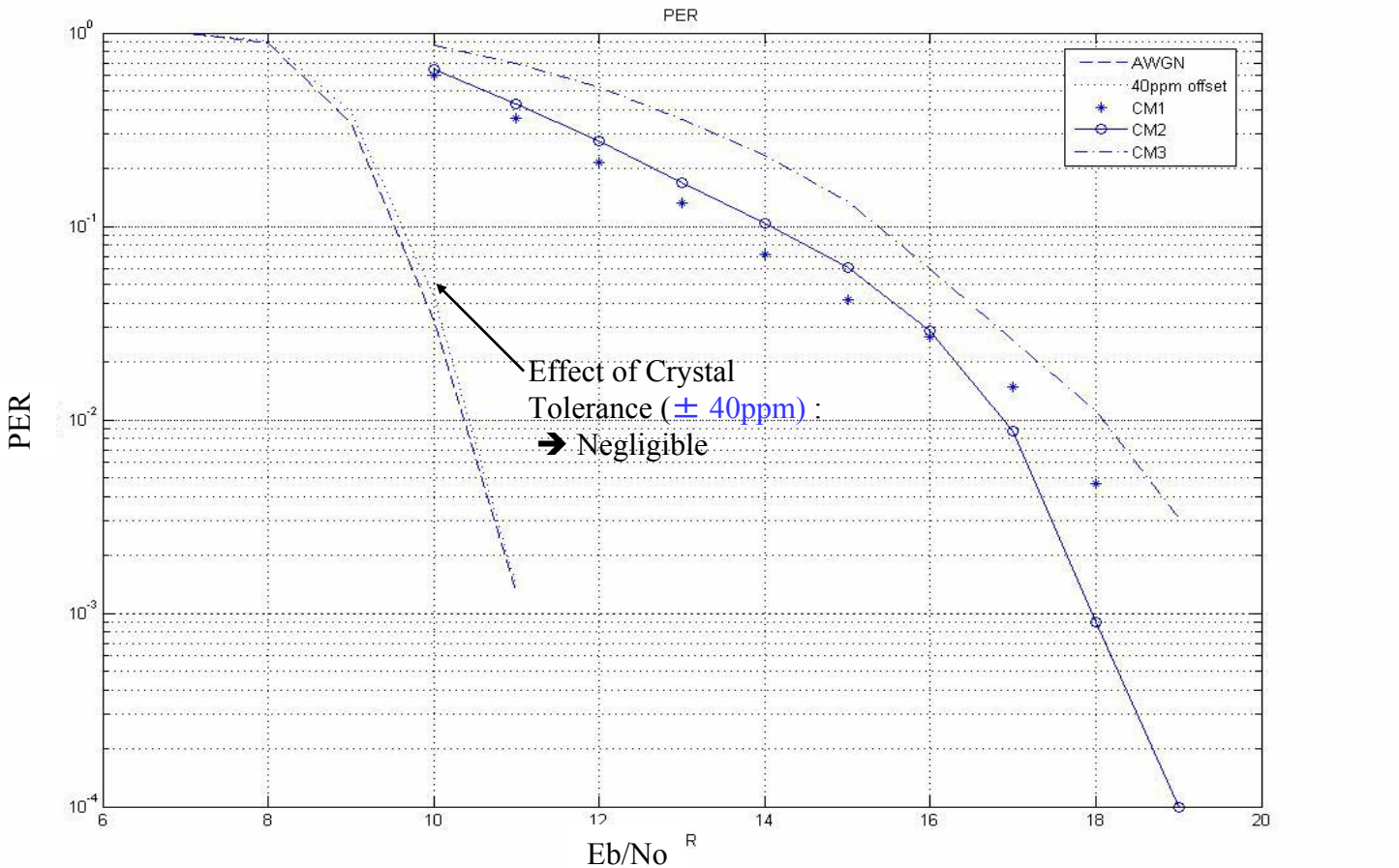
Miss Detection Probability



5. PHY LAYER CRITERIA

5.6. System Performance

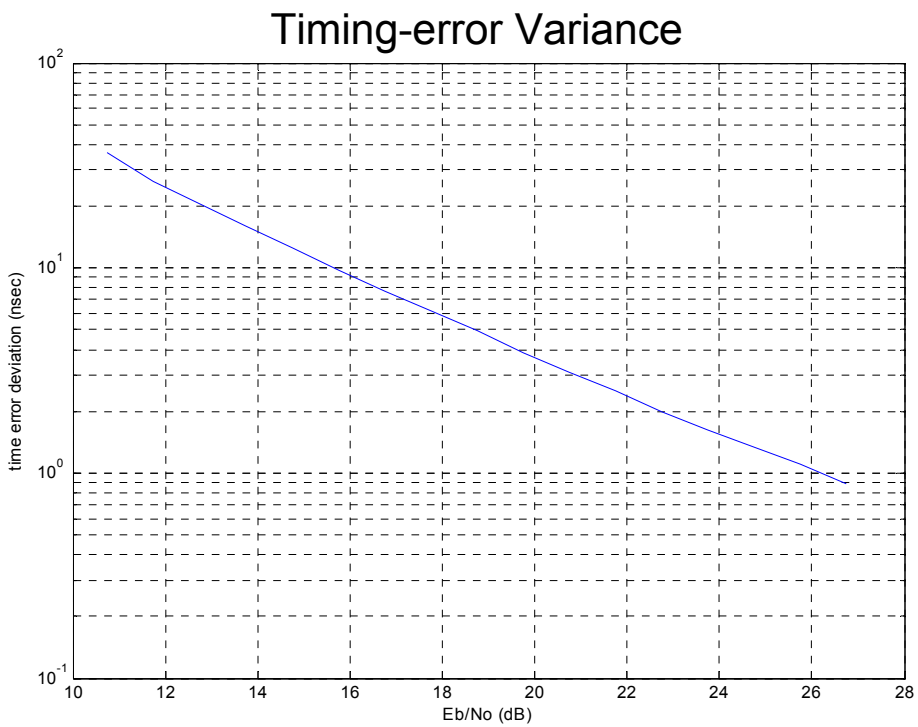
Data Rate : 1Mbps



5. PHY LAYER CRITERIA

5.7. Ranging

- **TDOA Based Ranging with Chirp Signal**
- **Estimation Precision: < 1m @ Eb/No greater than 22dB**



5. PHY LAYER CRITERIA

5.8. Link Budget

Parameter	Mandatory value		optional value	
peak payload bit rate(Rb)	250	kbps	1000	kbps
Average Tx Power(Pt)	10	dBm	10	dBm
Tx antenna gain(Gt)	0	dBi	0	dBi
fc' = sqrt(fminfmax) −10dB	2.44	GHz	2.44	GHz
Path loss at 1meter(L1=20log10(4pifc'/c))	40.2	dB	40.2	dB
distance	30	m	30	m
path loss at d m(L2=20log10(d))	29.5		29.5	
Rx antenna gain(Gr)	0	dBi	0	dBi
Rx power(Pr = Pt+Gt+Gr−L1−L2(dB))	−59.7	dBm	−59.7	dBm
Average noise power per bit	−120.0	dBm	−114.0	dBm
Rx Noise Figure(Nf)	7	dB	7	dB
Average noise power per bit(Pn=N+Nf)	−113.0	dBm	−107.0	dBm
Minimum Eb/No(S)	11	dB	11	dB
Implementation Loss(I)	3	dB	3	dB
Link Margin(M=Pr−Pn−S−I)	39.3	dB	33.3	dB
Proposed Min. Rx Sensitivity Level	−99.0	dBm	−93.0	dBm

5. PHY LAYER CRITERIA

5.9. Sensitivity

	Rx Sensitivity level (250kbps)	Rx Sensitivity level (1000kbps)
AWGN	-99dBm	-93dBm
CM1	-93dBm	-87dBm
CM2	-93.5dBm	-87.5dBm
CM3	-92.5dBm	-86.5dBm

5. PHY LAYER CRITERIA

5.10. Power Management Modes

- **Low-power Mode with Advanced Wake-up**
  - The proposed PHY has differentially bi-orthogonal detection and correlatively independent chirp-pulse waveform for multiple piconet

    => Superior SOP (Simultaneously Operating Piconets) performance

    => Low-power is achieved by *advanced wake-up* that the only desired piconets or group of nodes are called and the other piconets or nodes can estimate wake-up time from sleep state

    => Reducing Duty-Cycle and Extending Battery-life
  - This is compliant to “power consumption considerations” of 802.15.4 standard, and the mode operation for advanced wake-up may be added to this standard

5. PHY LAYER CRITERIA

5.11. Power Consumption

	Gate Equiv.	Die Area (mm^2)	Power Consumption
RF Section	-	5.6	60 mW @ Tx 10mW
Baseband @ Tx	3k	0.04	0.65 mW
Baseband @ Rx	51k	0.63	61.6 mW
Deep Sleep			12 uW

Base-band Target Library : 0.18 um Technology

5. PHY LAYER CRITERIA

5.12. Antenna Practicality

- **Antenna Size**
  - less than SD-Memory size: 24mm X 20mm
- **Frequency / Impulse Response**
- **Radiation Characteristics**
  - Isotropic: 0dBi