IEEE P802.15
Wireless Personal Area Networks

Project	IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)	
Title	**Technical Specification Draft for PSSS scheme**	
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Re:		
Abstract	This document describes the Parallel Sequence Spread Spectrum (PSSS) scheme for IEEE 802.15.4b technical specification	
Purpose	Discussion	
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IEEE 802.15.4b Draft
Section 6.9

6.6. Enhanced PSSS PHY specifications

The requirements for the enhanced PSSS PHY are specified in 6.9.1 through 6.9.4

6.6.1 Data rate

The data rate of the IEEE 802.15.4b enhanced PSSS PHY shall be 225 kbit/s.

6.6.2 Modulation and spreading

The enhanced PSSS PHY employs a (31+1)-ary quasi-orthogonal, parallel modulation technique. During each data symbol period, fifteen information bits are used to each select one of 15 nearly orthogonal pseudo-random (PN) sequences or their inverses. Such resulting 15 PN sequences are being super-positioned, a simple precoding is then executed per symbol, and the aggregate (31+1)-chip sequence is modulated onto the carrier using amplitude shift keying (ASK).

6.6.2.1 Reference modulator diagram

The functional block diagram in Table 1 is provided as a reference for specifying the enhanced PSSS PHY modulation and spreading functions. The number in each block refers to the subclause that describes that function.

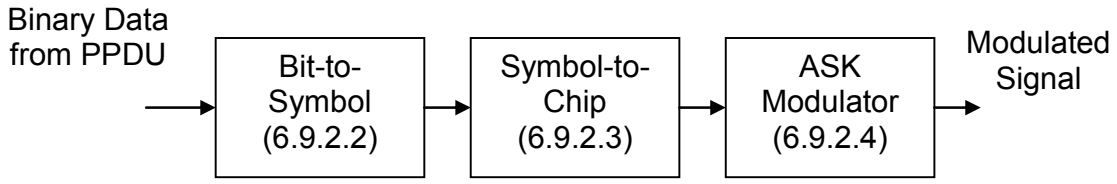

Table 1– Modulation and Spreading Functions

Each octet of the PPDU is sequentially processed through the spreading and modulation functions (see Table 1). All binary data contained in the PPDU shall be encoded using the modulation and spreading functions shown in Figure xxx1.

Before the transmission of the first data octet of the PDU, a synchronization header with a preamble and a start of frame delimiter shall be transmitted as described in subclause 6.6.4.

6.6.2.2 Bit-to-symbol mapping

This subclause describes how binary information is mapped into data symbols.

The 15 first bits of the PPDU – starting with the least significant bit (b0) of the first octet of the PPDU and continuing with the subsequent octet of the PPDU – shall be mapped into the first data symbol. Further 15 bits from the PPDU are mapped sequentially to each subsequent data symbol until all octets of the PPDU are mapped into symbols, always mapping the least significant bits of any octet first. For each symbol, the least significant bit from the first octet mapped will form the least significant bit of that data symbol. The last symbol is filled with "0" bits in its high order bits.

6.6.2.3 Symbol-to-chip mapping

Each data symbol shall be mapped into a 32-chip sequence as described in this subclause.

Table 2 provides an overview of the symbol-to-chip mapping.

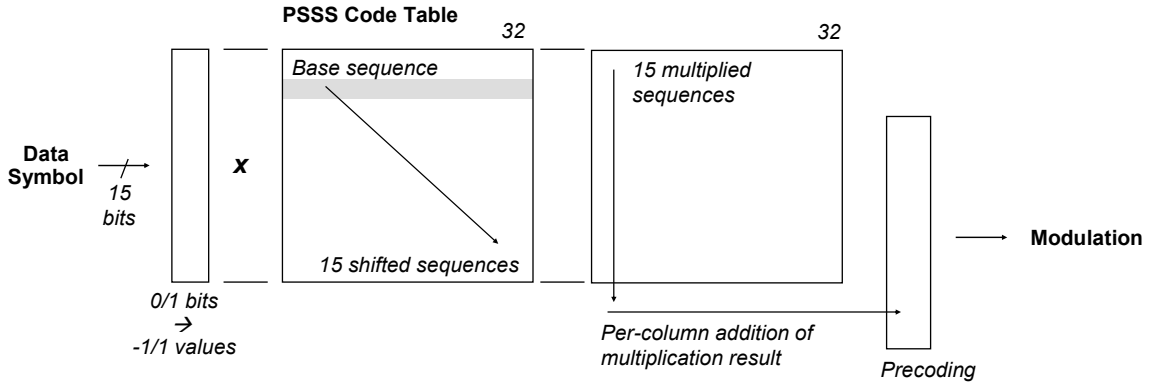

Table 2– Symbol-to-Chip mapping

Each bit of the data symbol is multiplied with its corresponding sequence of the code table defined in Table 3. The PSSS code table was generated by selecting 15 cyclically shifted sequences of a 31-chip base sequence and then adding a one bit cyclic extension to each sequence.

Table 3– PSSS Code table used in Symbol-to-Chip mapping

Sequence number	Chip number																															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1
1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1
2	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1
3	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1
4	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1
5	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1
6	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1
7	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1
8	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1
9	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1	-1	1
10	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1	1	-1
11	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1	1	-1	-1	1	-1	1
12	1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	-1	1	1	-1	1	-1	1	-1	-1	-1	-1	-1	1	-1	-1	1
13	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	1	-1	-1
14	-1	1	-1	-1	1	-1	1	1	-1	-1	1	1	1	1	1	-1	-1	-1	1	1	-1	1	1	1	-1	1	-1	1	-1	-1	-1	-1

The vector of bits in the data symbol is multiplied with the PSSS code table. I.e. bit b0 of the data symbol is multiplied with sequence number "0", bit b1 of the data symbol with sequence number "1", etc. For the value "0" of the bits of the data symbol the corresponding sequence is multiplied with "-1", for the value "1" with "1". The result is a table formed – depending on the bit values of the data symbol – row-by-row with the actual or inverse of the corresponding PSSS code sequence.

Subsequently, the chips of each multiplied sequence are added per column, e.g. the chips number "3" of each multiplied sequence are added to form the chip c3. The per-column results are 32 chips c0…c31.

After the per-column addition, precoding is executed for the 32 chips of each symbol. Precoding is performed in two steps: In the first step the values of the sequence of the 32 multi-valued chips are aligned symmetrical to zero without changing the relative difference between the chips. In the second step, the values of all 32 multi-valued chips in the symbol are scaled linearly so that the value of the chip(s) with the highest absolute value will be converted to the amplitude limit. The precoding of one symbol is executed independent of the precoding of any other symbol.

The precoded sequence of 32 multi-value chips is modulated as described in section 6.9.2.4

6.6.2.4 ASK modulation

The chip sequences representing each data symbol are modulated onto the carrier using ASK with raised cosine pulse shaping. The chip rate is 480 kchips/s.

6.9.2.4.1 Pulse shape

The pulse shape used to represent each baseband chip is described by

$$h(t) = 4\beta \frac{\cos\left((1+\beta)\pi t / T_C\right) + \sin\left((1-\beta)\pi t / T\right) / \left(4\beta t / T_C\right)}{\pi\sqrt{T_C}\left(\left(4\beta t / T_C\right)^2 - 1\right)}$$

with rolloff factor $\beta = 0.1$.

6.9.2.4.2 Chip transmission order

During each symbol period the least significant chip, c0, is transmitted first and the most significant chip, c31, is transmitted last.

6.6.3 Sub-1-GHz radio specification for the enhanced PSSS PHY

In addition to meeting regional regulatory requirements, devices operating in the sub-1-GHz band shall also meet the radio requirements in 6.6.3.1 through 6.6.3.5.

6.6.3.1 Operating frequency range

The enhanced PSSS PHY operates in the 868.0…868.6 MHz frequency band and in other bands as specified in one of the channel tables defined in subclause 6.6.5 of this specification.

Editor's Note:

In the joint proposal we agreed to define channel tables that define per regulatory domain which channel at which frequency will use what spreading and modulation mode. This was seen as a move to improve flexibility to add further channels for additional or existing regulatory domains if and when new regulatory rules become effective that enable the use of one or multiple IEEE802.15.4 PHYs.

We need to add that subclause and with it the PHY PIB parameter that indicates which channel table is to be used by an implementation.

Based on today's regulatory environment, one PSSS channel at 868.3 MHz for Europe and COBI channels in the 902..928 MHz band for the US will be defined by TG4b.

6.6.3.2 Transmit power spectral density (PSD) mask

The transmitted spectral density shall meet the regulatory requirements.

The following definitions of this subclause apply only when multiple enhanced PSSS PHY channels are defined in a channel table. It does not apply when only one single enhanced PSSS PHY channel is defined in the 868.0…868.6 MHz frequency band.

The transmitted spectral products shall be less than the limits specified in Table 4. For both relative and absolute limits, average spectral power shall be measured using a 100 kHz resolution bandwidth. For the relative limit, the reference level shall be the highest average spectral power measured within ± 300 kHz of the carrier frequency.

Table 4– Enhanced PSSS PHY transmit PSD limits

Frequency	Mode	Relative limit < 1GHz	Absolute limit < 1 GHz	Relative limit < 1GHz	Absolute limit > 1 GHz
| f – fc | > 300 kHz	Operating	-50 dB	-36 dBm (250nW)	-44 dB	-30dBm (1µW)
| f – fc | > 300 kHz	Standby	- 61 dB	-57 dBm (2nW)	- 51 dB	-47 dBm (20nW)

Editors Note:
I'm uncertain if we should add a reference to the ETSI Recommendation

6.6.3.3 Symbol rate
The enhanced PSSS PHY symbol rate shall be 15 ksymbols/s ± 20 ppm.

6.6.3.4 Receiver sensitivity
Under the conditions specified in 6.1.6, a compliant device shall be capable of achieving a sensitivity of –85 dBm or better.

Editor's Note:
In line with the objectives of the TG4b PHY work and the OEM requirements stated in the TG4b task group, we could consider to require a better receiver sensitivity here.

6.6.3.5 Receiver jamming resistance
This subclause only applies when multiple enhanced PSSS PHY channels are defined in a channel table. It does not apply when only one single enhanced PSSS PHY channel is defined in the 868.0…868.6 MHz frequency band.

The minimum jamming resistance levels are given in Table 5. The adjacent channel is one on either side of the desired channel that is closest in frequency to the desired channel, and the alternate channel is one more removed from the adjacent channel. For example, when channel 5 is the desired channel, channel 4 and channel 6 are the adjacent channels and channel 3 and channel 7 are the alternate channels.

Table 5 – Minimum receiver jamming resistance requirements for enhanced PSSS PHY

Adjacent channel rejection	Alternate channel rejection
0 dB	30 dB

The adjacent channel rejection shall be measured as follows: The desired signal shall be a compliant IEEE 802.15.4b enhanced PSSS PHY signal of pseudo-random data. The desired signal is input to the receiver at a level 3 dB above the maximum allowed receiver sensitivity given in 6.6.3.4.

In either the adjacent or the alternate channel, an IEEE 802.15.4 signal is input at the relative level specified in Table xxx4. The test shall be performed for only one interfering signal at a time. The receiver shall meet the error rate criteria defined in 6.1.6 under these conditions.

6.6.4 Synchronization header

Before the transmission of the first data octet of the PDU, a synchronization header with a preamble and a start of frame delimiter shall be transmitted.

The entire synchronization header and frame delimiter are transmitted with BPSK modulation with raised cosine pulse shaping as defined in subsection 6.9.2.4.1 at the same chip rate as the chips transmitted for the PPDU data. Figure 16 illustrates the synchronization header.

6.6.4.1 Preamble

The preamble is a 32-chip sequence that is formed out of 2 Barker codes as shown in Table 6. The left-most chip number “0” in the diagram is transmitted first.

Table 6– Preamble for enhanced PSSS PHY

Chip number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Value	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0
	Fill bits				Barker Sequence 1													Barker Sequence 2													Fill bits		

6.6.4.2 Start-of-frame delimiter

The SFD is an 8 bit field indicating the end of the synchronization (preamble) field and the start of the packet data. The SFD shall be formatted as illustrated in Figure 17.

Editor's note:

The SoF is unchanged. Instead of showing it in a table again, we better reference only where it is defined in the specification.

Common sections

6.6.5 Channel table

Editor's note:
This section need to be defined for all PHY modes together.