Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: [DS-UWB Responses to MB-OFDM-Voter NO Comments]
Date Submitted: [March 2004]
Source: [Matt Welborn] Company [Motorola]
Address [8133 Leesburg Pike]
Voice:[703-269-3000], E-Mail:[mwelborn@xtremespectrum.com]

Re: []

Abstract: [Response to NO voter comments and feedback regarding the DS-UWB (Merger #2) Proposal]

Purpose: [Provide technical information to the TG3a voters regarding DS-UWB (Merger #2) Proposal]

Motivation

- The OFDM approach has gone through repeated confirmation votes and has made changes as a response to NO votes received in that process. The DS approach has not had the benefit of this process and so is far away from consideration as a polished solution.

- The MERGED PROPOSAL #2 (DS-UWB) proposal is a "polished" solution under consideration by TG3a.
- The facts are:
  - It is backed not only by operating chips, but fully integrated operating systems
  - It has the benefit of years of practice. True learn-by-doing engineering
  - It is not an unproven concept that is still on the drawing board
    - Where history shows there is always a series of issues that are only revealed sequentially

- The DS-UWB proposal HAS benefited from the IEEE process
  - The DS-UWB proposal team, in response to TG3a feedback and customer requirements, has made numerous incremental changes
  - These changes make the DS-UWB proposal a significantly better match to the applications that TG3a seeks to serve.
- We look forward to showing TG3a the improvements and how they map to applications in such a way that makes DS-UWB all the more compelling.

Question 1: World-wide Compliance

- The MBOK proposal relies on implementing a Soft [Spectrum] Adaptation (SSA) scheme to ensure compliance with potentially different world-wide regulations….

- If it is not feasible to implement the SSA scheme in Silicon, *are there any other mechanisms* that can be used to ensure world-wide compliance? If yes, can you provide details?

Response 1: World-wide Compliance

1. The question inappropriately states that DS-UWB "relies" on SSA, suggesting that SSA is the only way DS-UWB has of adjusting its spectrum.

- DS-UWB has multiple powerful techniques to control its spectrum
  - Small, low-cost filters are already used for front-end protection and spectral shaping
  - Any mechanism, static or dynamic, that modifies the pulse shape or code, can be used
    - E.g. the low-pass RRC filter illustrated in the pulse generator in doc 153
      - This filter could easily be dynamically tuned or switched
    - Analog linear pulse combination - For example, in document 03/111r0
- ***These can be used without Tx-Rx negotiation protocols***
- The DS-UWB receiver is insensitive to the transmitted pulse shape
  - Only the chipping rates and center frequencies need to match,
  - The exact frequency of a narrow notch has little effect
  - The exact frequency for the edge of the pass-band has little effect

Question 1: World-wide Compliance

2. The question inappropriately assumes that real-time adaptation is required to "ensure world-wide compliance"

- The facts are:
  - There are no other regulations today besides those of the FCC
  - The other nations are working hard to have a global standard
  - None are considering dynamic notching as a requirement for UWB operation
    - For example, Software Defined Radio (SDR) schemes that have been suggested in other bands rely on built in GPS and access to large data-bases with maps of receiver locations so that the SDR knows how to protect receivers that do identify themselves by transmitting

- The desired regulatory outcome is a global standard that would preclude the need for special modes for different regions

Response 1: World-wide Compliance

3. The main requirement to obtain world-wide regulations is to minimize the potential for interference.

*   The fact is:

    –   ***All*** presentations to TG3a have shown that ***DS-UWB has optimal*** interference.

        *   MBOA presented measurements & analysis that showed DS-UWB ha the minimum interference (same as white noise)

        *   Other parties showed that DS-UWB had minimum interference by a more significant amount

    –   As a result, DS-UWB makes it easy to get world-wide regulations passed

Question 2 – How does SSA work?

- However, the CRL presentation in January 2003 shows that the SSA scheme would require the implementation of at least a 4-bit, 71.1 GHz DAC, or even a 284.4 GHz DAC. We were unable to obtain information regarding the power consumption, complexity or implementation feasibility of such a high-speed DAC. To better understand the global compliance capability of the MBOK proposal we would like answers to the following questions.

- As stated on slide 4, SSA is not required, is not a "preferred architecture," and is an entirely optional method.

Response 2: How does SSA work?

Specific questions on digital pulse generation using DACs

a. Is such a high-speed DAC feasible in Silicon?

The feasibility of directly generating SSA pulse using 3-bit, 8.8 GHz DAC are under investigation in CRL & CRL-UWB Consortium. It has been tested that this kind of DAC implementation is feasible utilizing present digital signal processing (DSP) technologies.

b. What is the expected power consumption and die-area of such a high-speed DAC?

The expected power consumption and die-area for the current RF unit including SSA pulse generator (DAC) is totally 3.2 mm*mm and 63 mW, respectively.

Response 2: How does SSA work

c. What is the trade-off between the DAC sampling rate and the depth and width of the notch that can be generated using SSA?

- It has been observed that decreasing the DAC sampling rate had almost no affected on the depth and width of the notch in a designed SSA pulse.

- It has been found that decreasing the DAC bit-width raises the spectral side-lobes.
  - 3 or more bits are required to get acceptable side-lobes, according to CRL Test-bed results.

Question 3: System Performance

The MBOK proposal has provided performance results for only some of the modes. In addition, multiple receiver architectures have been assumed to address issues related to performance, complexity and the different modes. In reality, only one of the architectures can be chosen for an implementation. To better understand the proposal and the trade-offs associated with an implementation, we would like all results to be presented for a preferred architecture. To better understand the capabilities and limitation of the MBOK proposal, we would like answers to the following questions.

(a) Can your present all the requirements stated in the selection criterion document, namely the performance, complexity, power consumption, SOP and coexistence for a preferred receiver architecture?

Response 3: System Performance

- "In reality, only one of the architectures can be chosen for an implementation"

- The latest DS-UWB proposal includes a "preferred architecture" that scales the data-rate primarily by using variable code-length rather than MBOK

- The changes specifically addresses handheld device requirements:
  - Higher speeds at shorter ranges and longer battery life
  - Applications like high-speed filesync to camcorder, PDA, tablet-PC, MP3/MPEG recorder/player, cell-phone/camera
  - Significantly reduced digital complexity of DS-UWB solution
    - Reduced power consumption and die size

Overview of DS-UWB Improvements

- Support for much higher data rates
  - BPSK modulation using variable length spreading codes
  - 4-BOK mode retained as optional

- At same time, much lower complexity and power
  - Essential for mobile & handheld applications
  - As low as 200k gates or less (1/3 of previous estimates) for great performance at long range and high rates at short range
  - Support for ultra-low power operation for short range (1-2 m) very high rates using un-coded modes (w/o Viterbi decoder)

- Harmonization & interoperability with MB-OFDM through Common Signaling Mode (CSM)
  - A single multi-mode PHY with both DS-UWB and MB-OFDM
  - Best characteristics of both approaches with most flexibility

DS-UWB Operating Bands & SOP
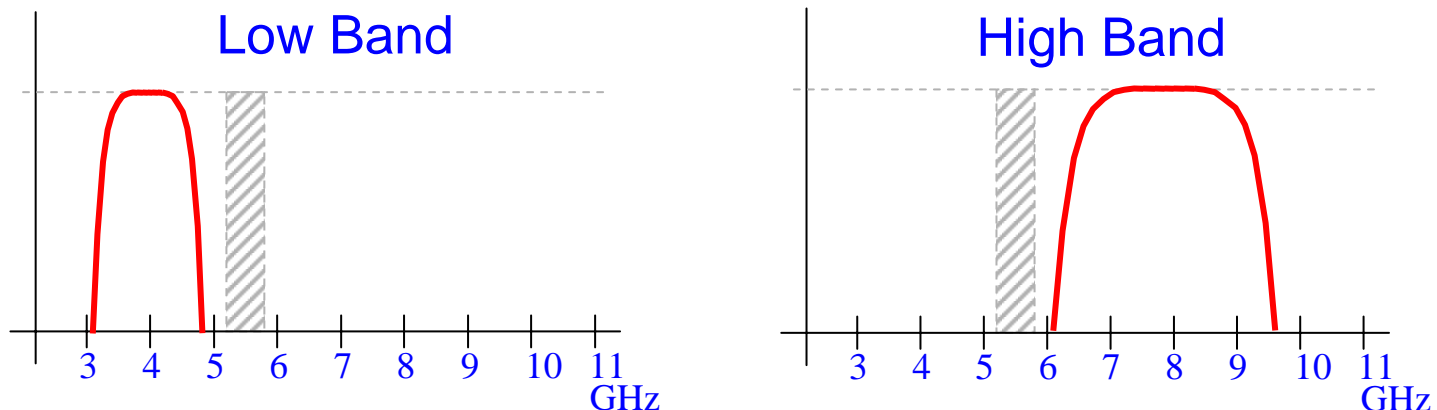
Low Band

High Band

- Each piconet operates in one of two bands
  - Low band (below U-NII, 3.1 to 4.9 GHz)
  - High band (optional, above U-NII, 6.2 to 9.7 GHz)

- Support for multiple piconets
  - Classic spread spectrum approach
  - Acquisition uses unique length-24 spreading codes
  - Chipping rate offsets to minimize cross-correlation

Data Rates Supported by DS-UWB

Data Rate	FEC Rate	Code Length	Range (AWGN)
28 Mbps	½	24	29.3 m
55 Mbps	½	12	22.1 m
110 Mbps	½	6	18.3 m
220 Mbps	½	3	12.9 m
500 Mbps	¾	2	7.3 m
660 Mbps	1	2	3 m
1000 Mbps	¾	1	5 m
1320 Mbps	1	1	2 m

Similar Modes defined for high band

Response 3: System Performance (cont.)

- Specific proposal improvements address handheld requirements
  - Implementing flexible code-lengths is simple & provides processing flexibility
  - FEC flexibility provides lower complexity modes with good performance
- Reduced k=7 FEC code to a k=6 FEC code resulting in a 50% reduction in power consumption & gate count for a small performance loss
- At short range FEC can be reduced to k=4 (optional) or turned off
  - The low fading across the wide coherent bandwidth allows FEC to be turned off at the highest speeds / shortest ranges (1-2m)
  - This give considerable power (and potential complexity) savings
- The gates applied to rake or CMF can be "swapped" as a function of code-length/data-rate
  - Used in parallel (fewer taps) at the higher speeds & short range
  - Used in series (more taps) at the lower speeds & longer range
- Takes advantage of short-range to reduce rake power
  - Rake can be turned off to save power at the shorter-range modes
  - Processing gain is not required at short range
- Thus the "preferred architecture" serves both handheld and powered devices that may require more range

Complexity For a Rake Receiver

Pre-Select Filter

$\cos (2\pi f_c t)$

I

$\sin (2\pi f_c t)$

Q

LNA

LPF

GA/VGA

ADC 1326 MHz, 3-bit ADC

LPF

GA/VGA

ADC 1326 MHz, 3-bit ADC

Synch. & Rake

DFE, De-Interleave & FEC Decode
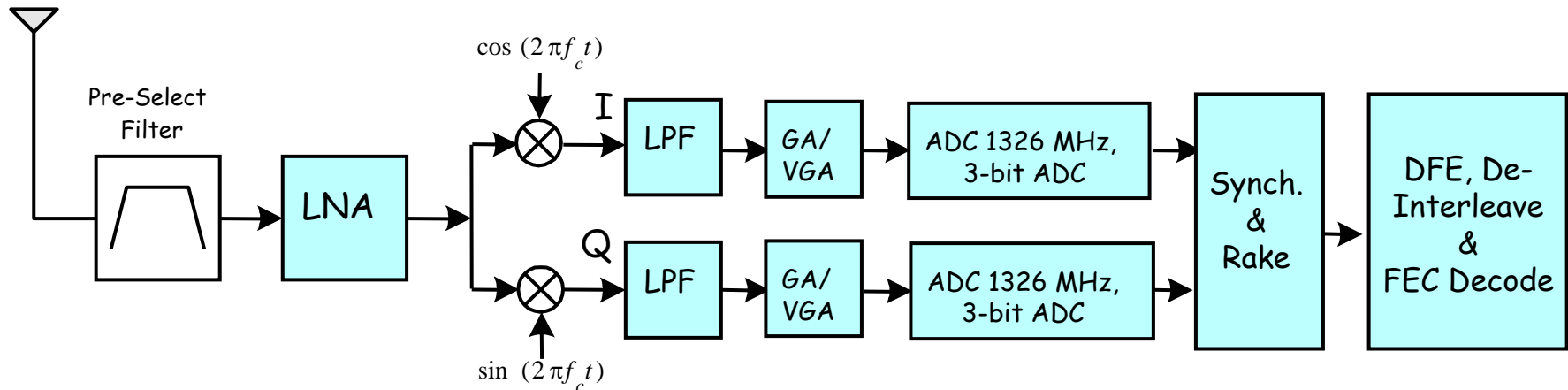
- Architecture assumptions
  - Front-end filter + LNA
  - I&Q sampling using 3-bit ADCs
  - 16-finger rake (at 110 Mbps) with 3-bit complex rake taps
  - Decision feedback equalizer at symbol rate
  - Viterbi decoder for k=6 convolutional code

Complexity Estimate Assumptions

- **Methodology for complexity estimate**
  - Use same approach as Merger #1 team in 03/449r0
  - Compute gate counts for 85.5 MHz clock speed
    - Estimates for functions at other speeds are adjusted using clock speed ratio

- **Modifications**
  - Removed functions no longer necessary (RS, MBOK)
  - Reduced complexity due to k=6 FEC code
  - Rake complexity reduction for DS-UWB improvements
    - Allows code correlator to be placed before the rake
  - Synchronization complexity
    - Previous estimate for 3-bit architecture was based on 1-bit correlator with length 553 – not appropriate here
  - Added complexity estimate for equalizer
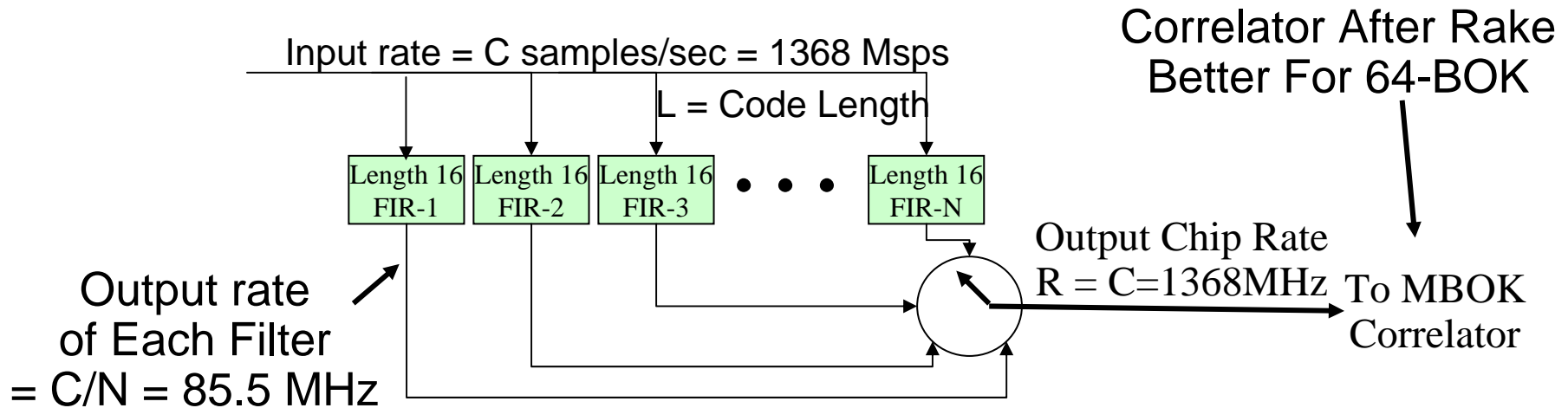
Complexity Estimates

Component	16-Finger Architecture (03/449r0 Estimate) **PREVIOUS PROPOSAL**	DS-UWB 16-Finger Rake Architecture **IMPROVED PROPOSAL**	DS-UWB 32-Finger Rake Architecture **IMPROVED PROPOSAL**
Matched filter [rake]	205K	26K	45K
Viterbi decoder	108K	54K	54K
Reed-Solomon decoder	20K	Not needed	Not needed
MBOK demodulator	61K	Not needed	Not needed
Synchronization	177K	30K	30K
Channel estimation	24K	24K	24K
Other Miscellaneous including RAM	30K	30K	30K
Equalizer	Not used	20K	20K
Total gates @ 85.5 MHz	604K	**184K**	**203K**

How Can The Rake Be So Small?

- ## Gate count reduction is due to
  - ### Moving of code correlator prior to rake
    - Code correlator (only requires adders) reduces processing rate to symbol rate prior to CMF or rake processing
  - ### Output rate is L times lower (L= code length)
    - Reduces output rate by the code length
  - ### Replace 64-BOK with 2-BOK (BPSK)
- ## A/D Is 3 bits, not 4 bits

MBOA Estimates Based On 16 Parallel Branches, 4-bit A/D, Chip-Rate Output

Parallel N=16 filters so each can run slower by a factor of 16
1368/16 = 85.5 MHz

Input rate = C samples/sec = 1368 Msps

Correlator After Rake
Better For 64-BOK

L = Code Length

| Length 16 FIR-1 | Length 16 FIR-2 | Length 16 FIR-3 | • • • | Length 16 FIR-N |

Output Chip Rate
R = C=1368MHz   To MBOK
Correlator

Output rate
of Each Filter
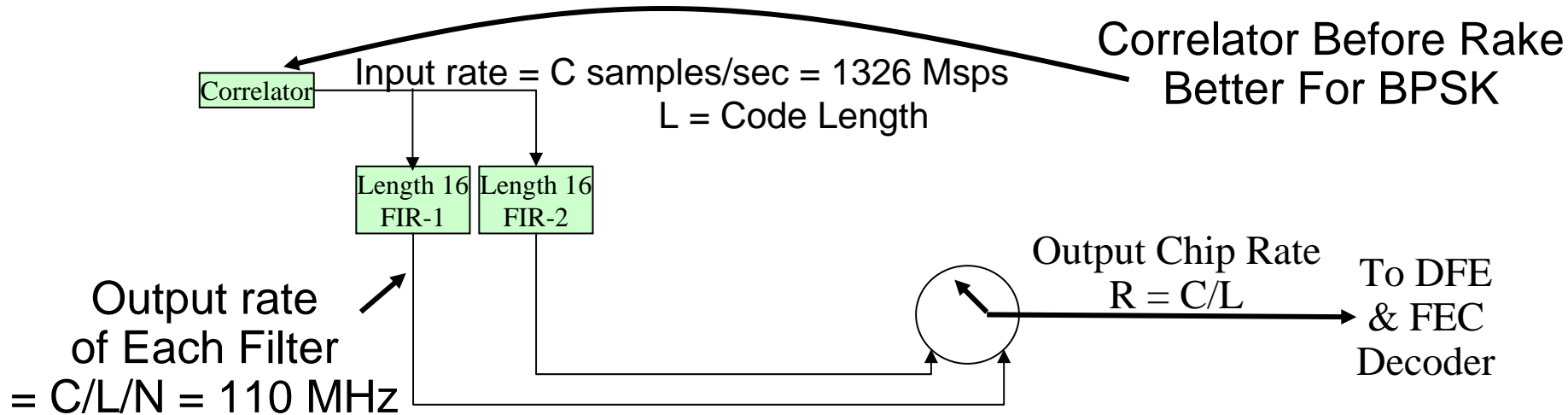= C/N = 85.5 MHz

OLD PROPOSAL CALCULATED BY MBOA
Complexity = (16 multipliers) * (N=16 branches) * (800 gates per 4-bit mult)

= 205k Gates   @ 85.5 MHz for rake filter

Improved Proposal Is Based On 2 Parallel Branches, 3-bit A/D, Symbol Rate Output

Parallel N=2 filters so each can run slower by a factor of 2

$$1326/L/2 = 1326/6/2 = 110 \text{ MHz}$$

Correlator Before Rake Better For BPSK

Correlator

Input rate = C samples/sec = 1326 Msps

L = Code Length

Length 16 FIR-1   Length 16 FIR-2

Output rate
of Each Filter
= C/L/N = 110 MHz

Output Chip Rate
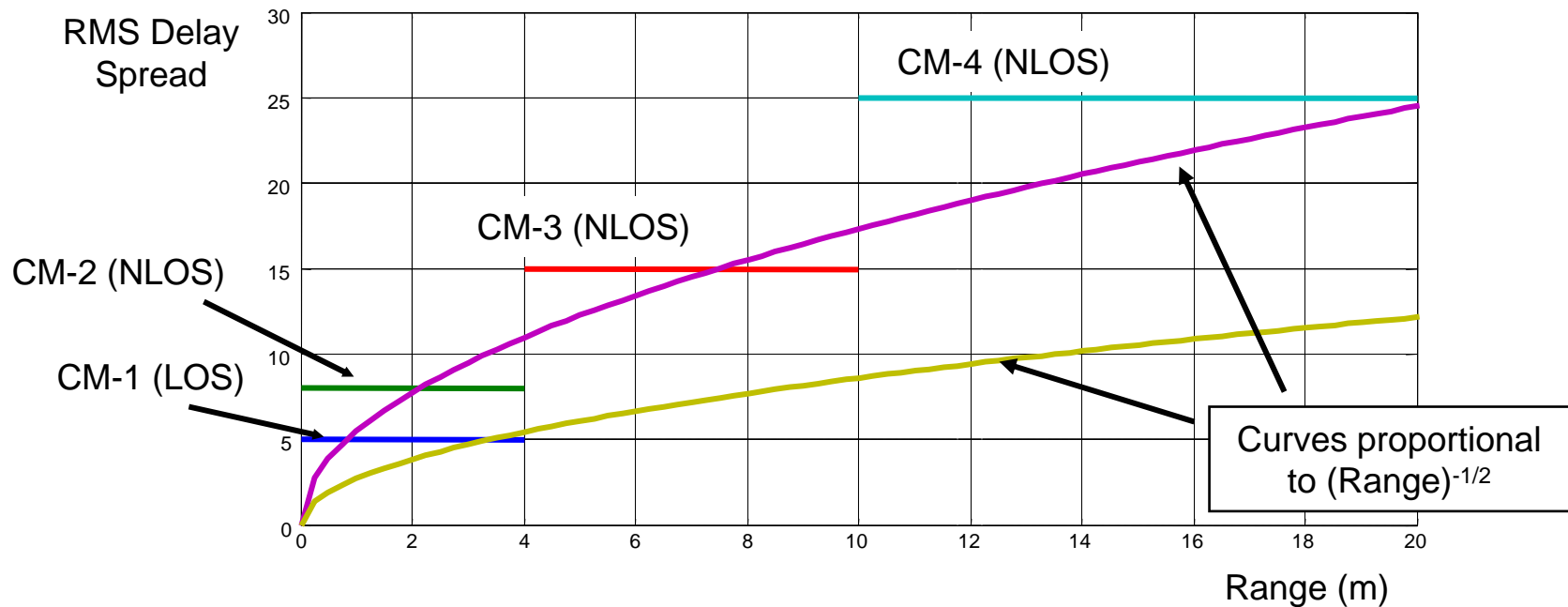$R = C/L$

To DFE
& FEC
Decoder

NEW PROPOSAL CHANGES TO

Complexity = (16 multipliers) * (N=2 branches) * (400 gates per 3-bit mult) * (110 MHz)

= 26k Gates (including adders and overhead)

85.5MHz

Improved Proposal has Variable Rake Terms to Match Multipath & Save Power

RMS Delay Spread

CM-4 (NLOS)

CM-3 (NLOS)

CM-2 (NLOS)

CM-1 (LOS)

Curves proportional to $(Range)^{-1/2}$

Range (m)

- **Multipath delay spread increases with range**
  - High rate modes operate at shorter ranges – few taps
  - Lower rate modes operate at longer ranges – more taps
  - In AWGN, only one tap is needed

How can the Rake Adapt to Speed?

FIR1
8 taps

FIR2
8 taps

FIR3
8 taps

FIR4
8 taps

For 220 Mbps mode, L= 3, so the number of branches is n/3 = 4

Each branch is half as long as for 110 Mbps

At a rate 2x higher, we can use the same transistors (multipliers and adders) to implement a rake with twice the number of branches, each half as long – for the same total complexity

Output rate 440 MHz (220 Mbps)
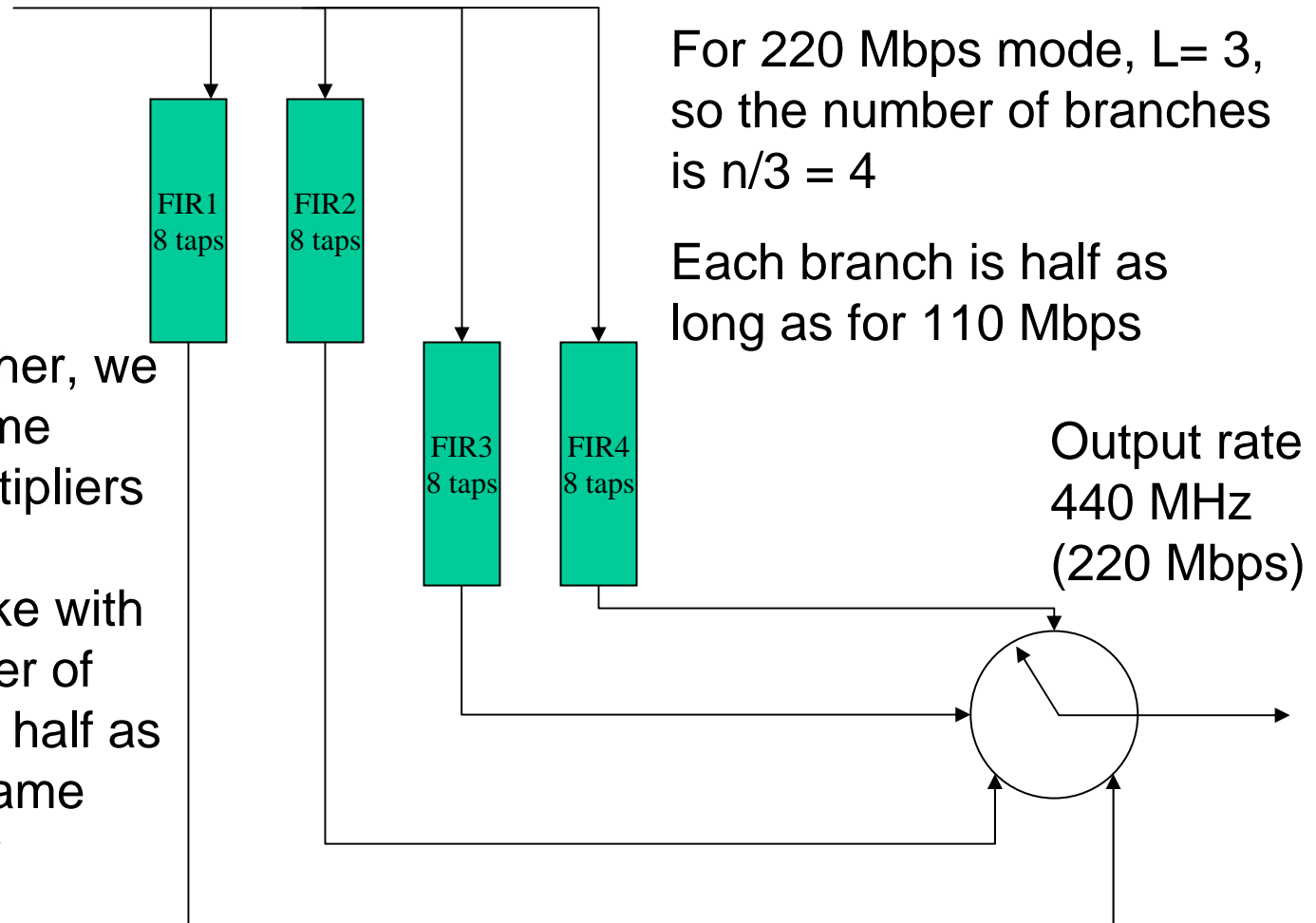
Low Rake Complexity for 16 Fingers

- Adaptive rake complexity
  - 16 taps at 110 Mbps (220 MHz before FEC)
  - 8 taps at 220 Mbps (6-10 meters)
  - 5 taps at 500 Mbps (3-4 meters)
  - 2 taps at 1000 Mbps (1-2 meters)
- Gate counts for a 16-finger rake implementation
  - Assume 400 gates/3-bit complex multiply
  - Needs 16 3-bit complex multiplies at 220 MHz output rate
  - Needs 2 parallel branches for 110 MHz clock (n=2)
  - Total is 32 multipliers for 12,800 gates
  - Also add 64 adders at average 34 gates/adder $\approx$ 2200 gates
  - Add 5000 gates (33%) for miscellaneous overhead
  - Total gate count is 20,000 at 110 MHz
  - Equivalent to 26K gates at 85.5 MHz (per 03/449r0 methodology)
- 12 taps = 21K gates, 24 taps = 35K gates, 32 taps = 45K gates

Synchronization & Equalizer

- Synchronization complexity
  - Receiver correlates against length-24 acquisition spreading codes
  - Output is at symbol rate (Fchip/24 = 55 MHz)
  - Correlation involves only multiplication by –1/0/+1 (i.e. only adders)
  - Multiple correlator branches in parallel improves acquisition
    - Faster search though range of possible timing offsets
    - Allows longer integration during each step
  - Synchronization uses the same correlators used for rake
  - Estimate allows 30K additional gates for synchronization and 24K additional gates for channel estimation
- Equalizer complexity
  - Linear equalizer: just another FIR filter (real-valued for BPSK)
  - Assume 400 gates per multiply/accumulate (very conservative)
  - 20-tap LEQ at 220 MHz = 40 multiply/accumulates @ 110 MHz
    - Same gates provide 10 taps at 440 MHz, 6 taps at 660 MHz
  - Total gates for LEQ < 21K @ 85.5 MHz
  - DFE uses no multipliers→feedback & add: 30 taps =<20 K gates @ 85.5 MHz

Question 3: System Performance (cont.)

(b) Performance results in the presence of multi-path, SOP performance and robustness to narrow-band interferers have not been presented for the MBOK modes corresponding to 114 Mbps and 200 Mbps. Can you provide all results for these two modes?

These two specific modes (114 and 200 Mbps) have been superceded in the current DS-UWB proposal.

Performance results for current are given in response to other questions.

Multipath Performance for **110 Mbps**

110 Mbps	90% Outage	Mean of Top 90%
CM1	13.5	16.9
CM2	11.7	14.6
CM3	11.4	13.4
CM4	10.8	13.0

Simulation Includes:

16 finger rake with coefficients quantized to 3-bits

3-bit A/D (I and Q channels)

RRC pulse shaping

DFE trained in < 5us in noisy channel (12 Taps)

Front-end filter for Tx/Rx + 6.6 dB Noise Figure

Packet loss due to acquisition failure

AWGN Range @110 Mbps = 22.2 m

Multipath Performance for **220 Mbps**

220 Mbps	90% Outage	Mean of Top 90%
CM1	8.4	10.2
CM2	5.8	8.2
CM3	4.9	6.2

Simulation Includes:

8 finger rake with coefficients quantized to 3-bits

3-bit A/D (I and Q channels)

RRC pulse shaping

DFE trained in < 5us in noisy channel (12 Taps)

Front-end filter for Tx/Rx + 6.6 dB Noise Figure

Packet loss due to acquisition failure

AWGN Range @220 Mbps = 16.2 m

8 vs. 16 Finger Rake @ 220 Mbps

220 Mbps	8 Finger 90% Outage	16 Finger 90% Outage	8 Finger Mean of Top 90%	16 Finger Mean of Top 90%
CM2	5.8	7.2	8.2	8.8
CM3	4.9	7.0	6.2	8.4

Increase in complexity due to
- 16 Finger Rake @ 220 Mbps
- DFE Extended to 24 Taps

AWGN SOP Distance Ratios

	Test Distance	1 Int. dist ratio	2 Int. dist ratio	3 Int. dist ratio
110 Mbps	15.7 m	0.65	0.92	1.16
220 Mbps	11.4 m	0.90	1.28	1.60

- AWGN distances for low band
- High band ratios expected to be lower
  - Operates with 2x bandwidth, so 3 dB more processing gain

Response 3: Data Throughput Performance

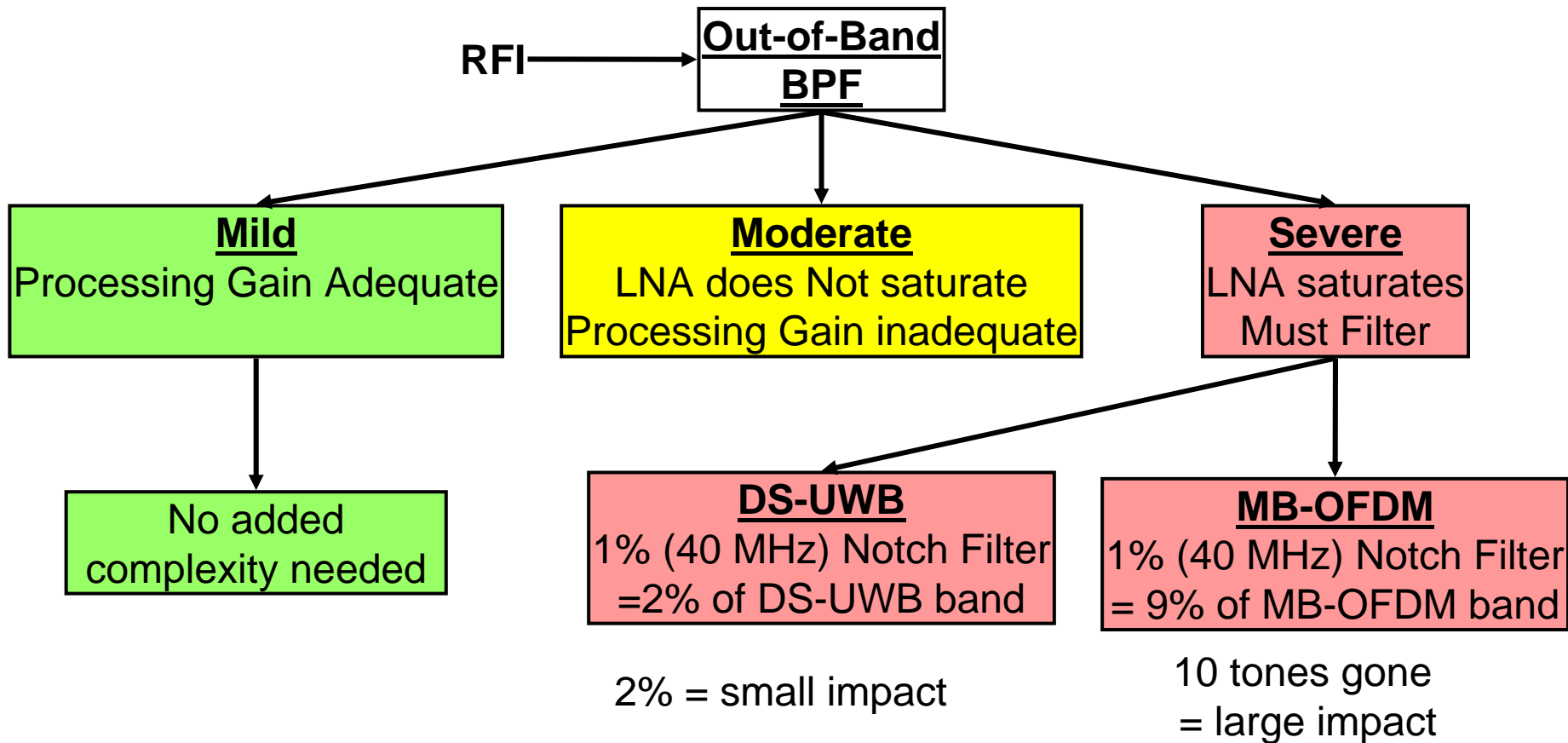|										
Bit Rate (Mbps)		27.5	55	82.5	110	220	495	660	990	1320
FEC symbol rate		55	110	110	220	440	660	660	1320	1320
Code Lenth		24	12	12	6	3	2	2	1	1
BPSK/QPSK		BPSK	BPSK	BPSK	BPSK	BPSK	BPSK	BPSK	BPSK	BPSK
Bits per symbol										
Payload FEC rate		0.5	0.5	0.75	0.5	0.5	0.75	1	0.75	1
T_PA_INITIAL	15									
T_PA_CONT	0									
T_PHYHDR_INITIAL	1.31									
T_MACHDR_INITIAL	4.36									
T_HCS_INITIAL	0.87									
T_PHYHDR_CONT		0.87	0.44	0.29	0.22	0.11	0.05	0.04	0.02	0.02
T_MACHDR_CONT		2.91	1.45	0.97	0.73	0.36	0.16	0.12	0.08	0.06
T_HCS_CONT		0.58	0.29	0.19	0.15	0.07	0.03	0.02	0.02	0.01
T_MPDU		297.89	148.95	99.30	74.47	37.24	16.55	12.41	8.27	6.21
T_FCS		1.16	0.58	0.39	0.29	0.15	0.06	0.05	0.03	0.02
T_SIFS	5	5	5	5	5	5	5	5	5	5
T_FEC_OH		13.27	6.64	6.64	3.32	1.66	1.11	1.11	0.55	0.55
T_MIFS	0	0	0	0	0	0	0	0	0	0
T_ONE_FRAME		338.87	182.71	132.87	104.63	65.59	44.27	40.11	35.41	33.33
Throughput_1 (Mbps)		24.17	44.84	61.66	78.30	124.90	185.06	204.23	231.38	245.79
T_FIVE_FRAMES		1552.55	789.55	537.42	408.05	217.30	111.69	90.68	69.12	58.61
Throughput_5 (Mbps)		26.38	51.88	76.22	100.38	188.50	366.72	451.69	592.60	698.81

- Throughput analysis based on 1024-octet packet length
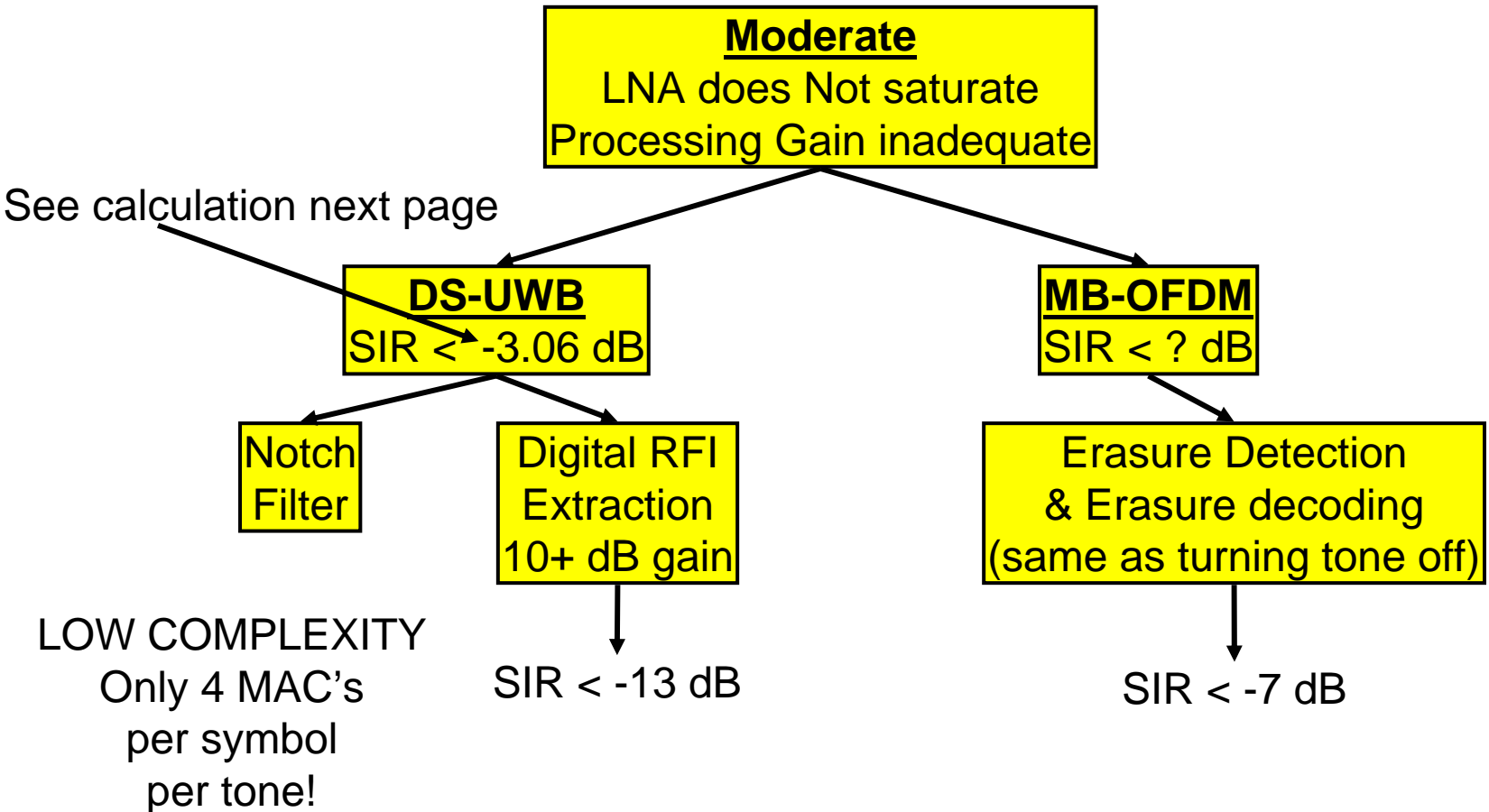
Question 4: Narrow-Band Interference

(c) **Robustness to Narrow-band Interferers**: Document 15-03-0449-03-003a also demonstrates that the MBOK system does not meet the requirements of the selection criteria document in its ability to handle narrow band interferers. It is shown to be about 10 dB worse than the MB-OFDM system. The MBOK proposal claims that narrow-band interference rejection is performed using an external tunable notch filter. Can you provide details on the mechanism to detect a narrow-band interferer, the effectiveness and complexity of the detection circuitry and the loss in performance due to inserting a tunable notch filter at the receiver? Is the insertion loss due to the tunable notch filter also considered for all the other performance results?

- Warning: A complete response to this question seems to require a direct comparison with NBI performance results for MB-OFDM systems
- We do not agree with the results referenced above and will show a calculation we believe is correct.

NarrowBand Interference (NBI)
# Radio Frequency Interference (RFI)
3-Cases

RFI → **Out-of-Band BPF**

Mild
Processing Gain Adequate

Moderate
LNA does Not saturate
Processing Gain inadequate

Severe
LNA saturates
Must Filter

No added
complexity needed

DS-UWB
1% (40 MHz) Notch Filter
=2% of DS-UWB band

MB-OFDM
1% (40 MHz) Notch Filter
= 9% of MB-OFDM band

2% = small impact

10 tones gone
= large impact

Moderate RFI

Moderate
LNA does Not saturate
Processing Gain inadequate

See calculation next page

DS-UWB
SIR < -3.06 dB

MB-OFDM
SIR < ? dB

Notch
Filter

Digital RFI
Extraction
10+ dB gain

Erasure Detection
& Erasure decoding
(same as turning tone off)

LOW COMPLEXITY
Only 4 MAC's
per symbol
per tone!

SIR < -13 dB

SIR < -7 dB

Response 4: Narrow-Band Interference

- **DS-UWB receivers with 3-bit ADC architectures**
  - Simulations with no active NBI compensation indicate about 3 dB I-to-S is to be expected
  - Simple analysis with NO ACTIVE COMPENSATION (worst case):
    - Required Eb/No is 5.0 dB for rate-½ FEC code
    - Assume 1.5 dB implementation loss (based on simulation results)
    - Total noise-per-bit is –87 dBm = -174dBm/Hz + 10log(110MHz) + (6.6 dB NF)
    - Sensitivity = -87+5+1.5= 80.5
    - Sensitivity + 6dB (per spec) = signal power (S) = -74.5 dBm
    - Allowable (I+N) = -74.5 - 5.0 - 1.5 = -81 dBm (assume I is noise-like at slicer)
    - Allowable I is therefore 10*log(10^(-81/10)-10^(-87/10)) = -82.24 dBm
    - At 110 Mbps, processing gain is 12:1 over (I+N) in signal bandwidth → 10.8 dB gain (worst case)
      - Processing gain is a function of tone frequency – depends on pulse shape. At band edges, gain is much higher
    - Allowable I-to-S is therefore -81.24 + 10.8 -(-74.5) = **3.06 dB I-to-S**
  - Result for high-band operation is 6.0 dB allowable I-to-S
    - 3 dB better than low band operation because 2x signal bandwidth provides 3 dB more processing gain
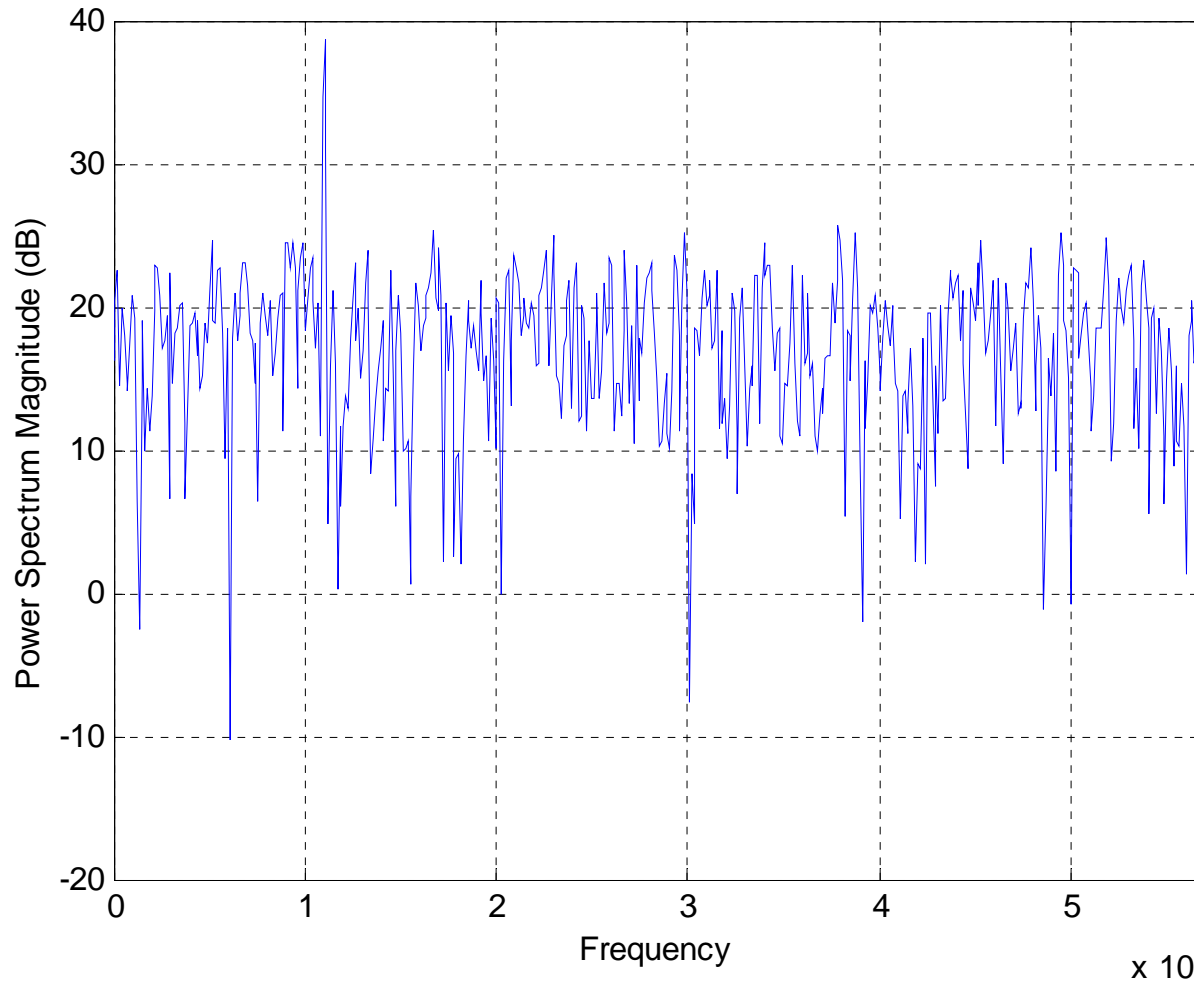
Digital RFI Removal

- Real signal and noise from hardware
- A/D samples fed into Matlab
- 6 bits used to represent basis functions
- Data processed in 128 sample blocks

Before (SIR = 5 dB)

After (SNR = 15 dB)
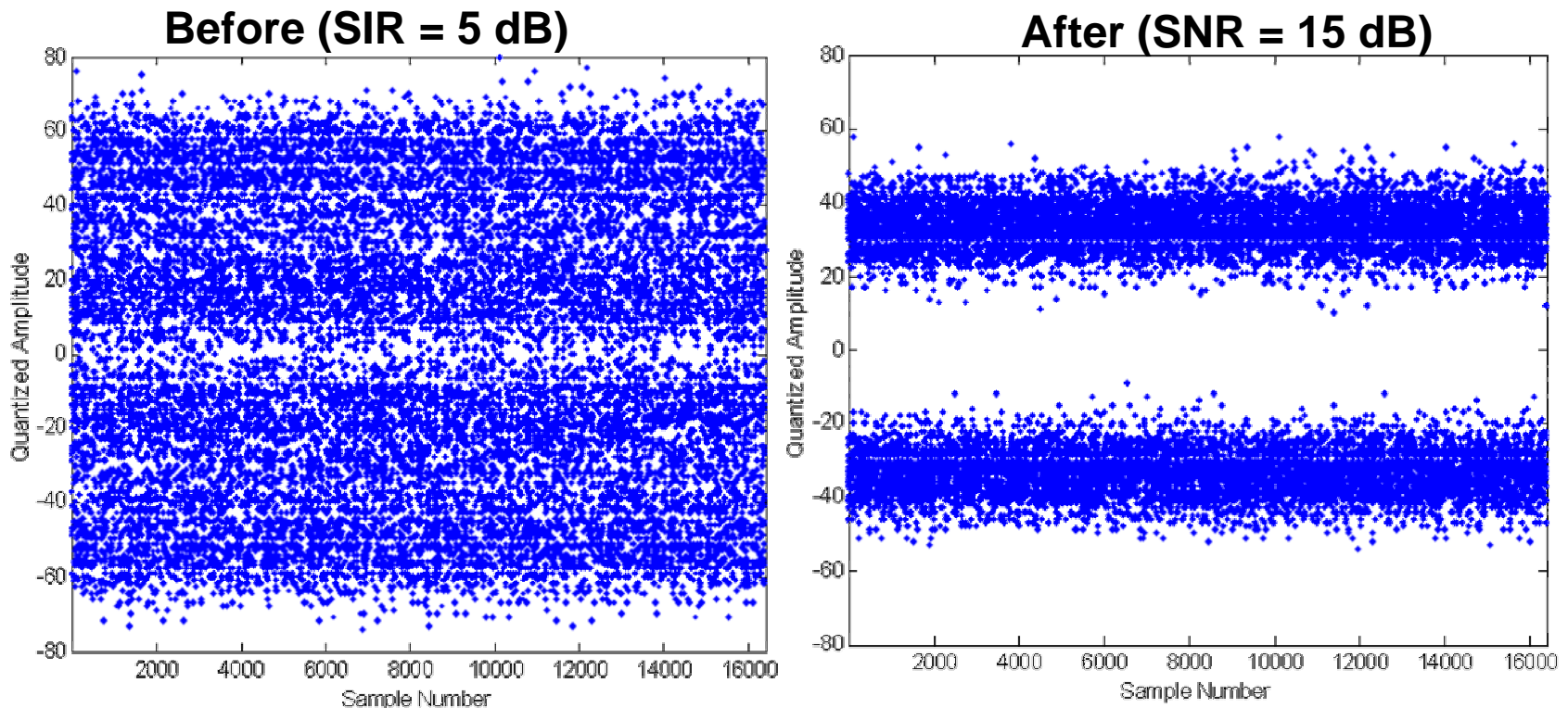
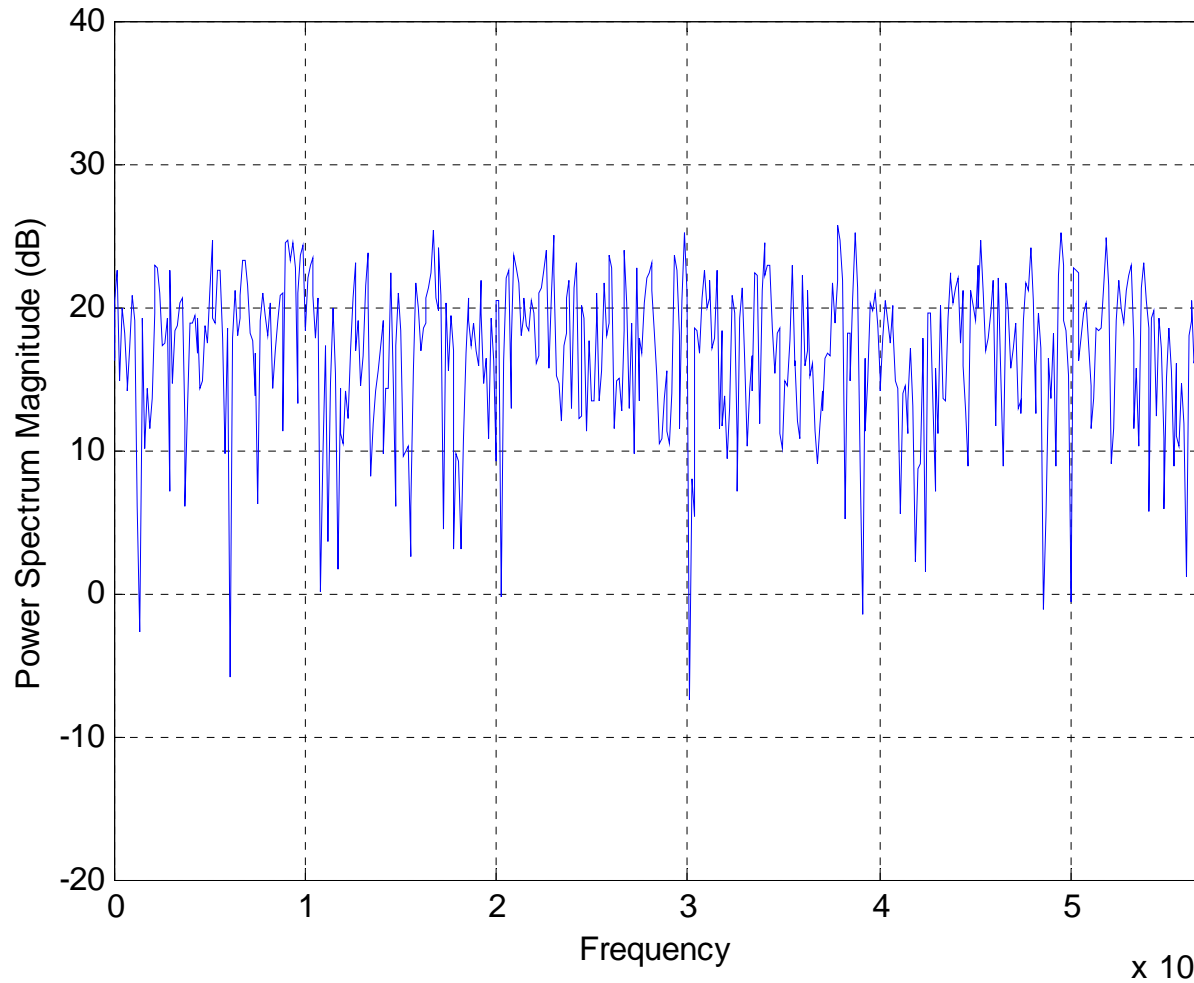# Quantized RFI Suppression Performance Vs. Frequency Error
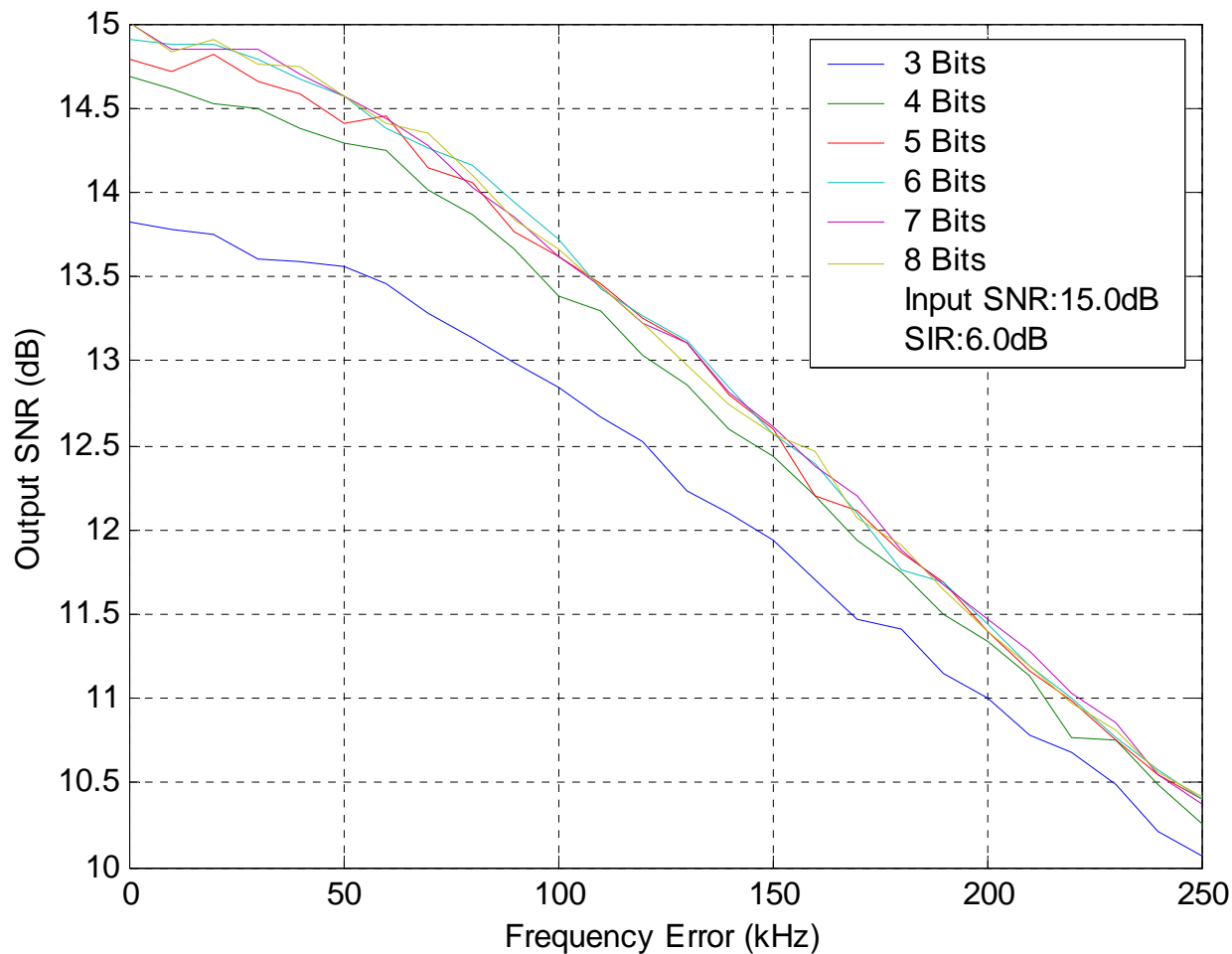
Spectrum Before Extraction

Fd = 114e6

Resolution:
Fd/1024 =
111 kHz

Spectrum After Extraction

Fd = 114e6

Resolution:
Fd/1024 =
111 kHz

Response 4: Narrow-Band Interference

- Assumptions for the DS-UWB 16-finger rake architecture analysis included no additional processing to combat NBI
  - The referenced document acknowledges that it "may be possible to use DSP techniques" to improve DS-UWB performance in NBI, but "the complexity of the [DS-UWB] receiver will then increase"
  - It seems that no attempt was made to improve the DS-UWB performance in NBI
- The equivalent results for the MB-OFDM approach assumed that the MB-OFDM receiver had implemented additional processing (erasure decoding) in order to actively combat NBI (per 03/268r1)
  - No details given on complexity of erasure decoding or algorithm training
  - It does not appear that this erasure decoding technique would otherwise be required for implementation of a compliant MB-OFDM device
  - Erasure decoding therefore represents an "increase" in "complexity" made in order to actively compensate for NBI
  - No details were given on the NBI performance of MB-OFDM *without* erasure decoding
- A more neutral comparison would be
  - Both system use active compensation for NBI, or
  - Neither system uses DSP compensation above what is required for compliance
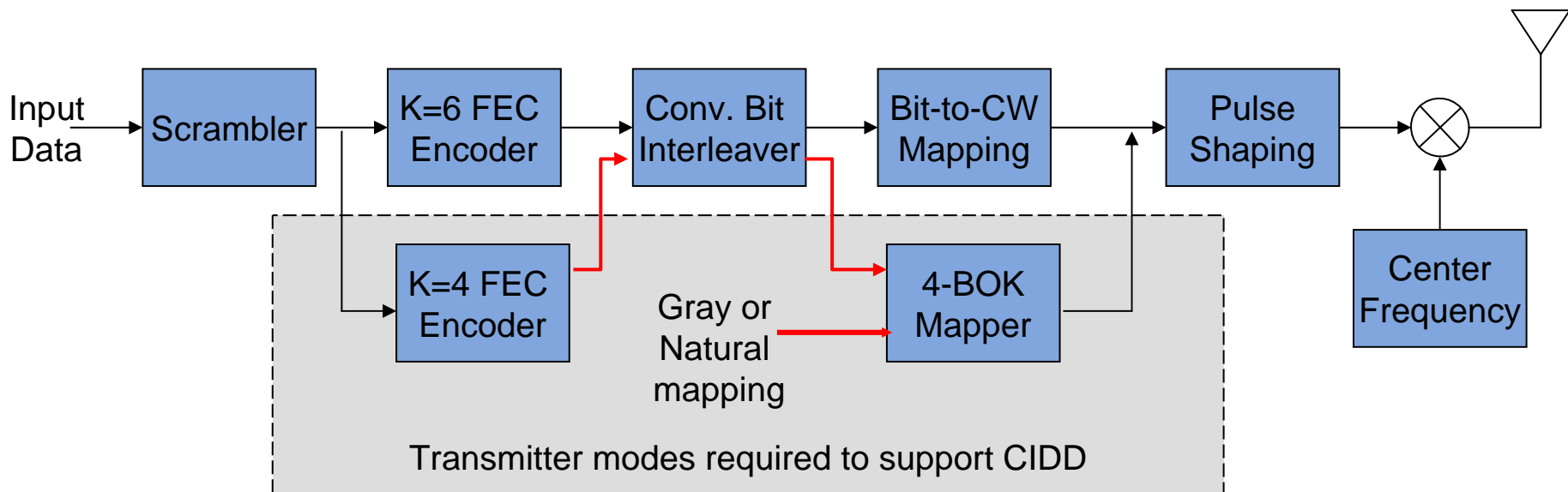
Question 5: Forward Error Correction

The 114 Mbps mode has two possible coding schemes, one with a K = 7 convolutional code and the other with a K = 4 convolutional code. The K = 4 convolutional code has been used to enable an iterative soft decoder and demodulator. It is confusing to an implementer if multiple coding schemes are specified for the same data rate. If the proponents feel that one coding scheme provides a better performance versus complexity trade-off, they should choose the better of the two coding schemes. Otherwise, an implementer has to build multiple decoders at the receiver. In addition, it is not clear how a DEV would decide on which of the two coding schemes to use for this data rate.

Response 5: Forward Error Correction

- The new DS-UWB proposal addressed this issue while addressing the speed/power demands of handheld devices.

- A huge power advantage in trade for a very small decrease in range (<.5 dB) can be obtained by changing to a K=6 FEC
  - Smaller width lattice, and much shorter trace-back

- In order to further reduce power, our new proposal can use a K=4 code in some of the highest speed modes.
  - One or the other or both can be "not used" and turned off to conserve power.
  - A k=4 FEC is a very small investment in die-size and is ¼ the power of a k=6 and much more amenable to run at 660-1400 Mbps input rates

- To allow the benefits of CIDD, the k=4 encoder can be used instead of the k=6 encoder in the lower speed modes.

- This information can be passed in the PHY header.

Response 5: Forward Error Correction

- Transmitter supports both k=4 and k=6 FEC encoders
  - k=4 encoder can be used at higher rates (for lower complexity implementation)
  - k=4 encoder also used to support iterative decoding (CIDD)

Response 5: Forward Error Correction

A RS code is used as a concatenated code for data rates of 112 Mbps, 200 Mbps, 224 Mbps and 448 Mbps. The use of a concatenated code results in latency due to the need to receive the entire code word before decoding/de-interleaving and the latency of the decoder operation. For instance, a latency of two code words at a data rate of 112 Mbps corresponds to ~8 microseconds. However, the SIFS time specified in the MBOK proposal is 5 microseconds. How is it possible to meet the SIFS time, if a concatenated code is used?

Reed-Solomon codes are no longer a part of the DS-UWB proposal.

Question 6: Acquisition Limits

The acquisition curves presented in document 802-15-03/334r5 (slide 58) shows that the system is acquisition limited. For instance, when transmitting at a data rate of 114 Mbps and operating at an Eb/N0 of 4 dB (corresponds to sensitivity) approximately 15% of the packets are missed even when the false alarm probability is set at a high value of 1%. This is a serious deficiency in the system and would have a greater impact at lower data rates and hence needs to be addressed. In addition, could you also provide the acquisition time necessary to obtain this performance?

- The results mentioned above assumed the equivalent of 3-finger rake complexity
  - For architecture analyzed here, it is reasonable to usemore parallel acquisition correlators
  - Also, minimum operating Eb/No is higher (5 dB) than previously
- Acquisition is based on sliding correlator design using hierarchical sequence
  - With more correlators, acquisition is faster <u>and</u> provides more integration at each point
  - Acquisition correlators reuse the same transistors as CMF or rake stages

Question 6: Acquisition Limits
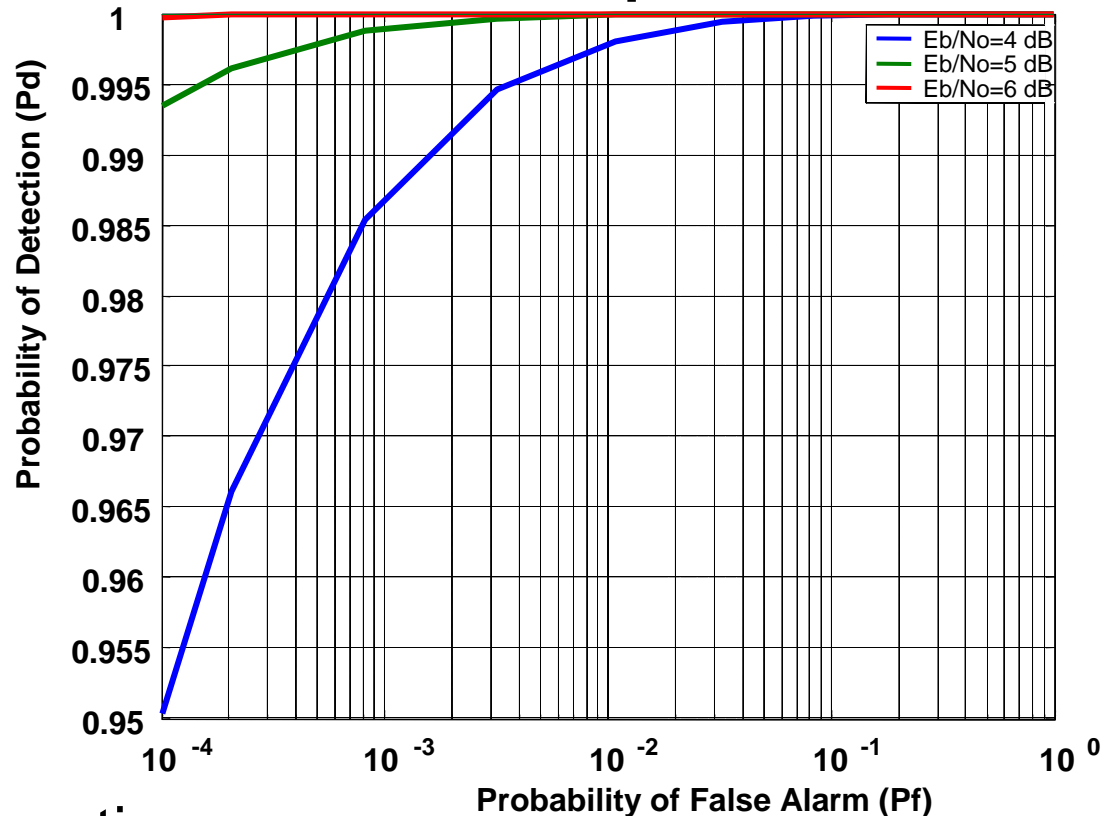
- Assumptions:
  - Nine parallel acquisition correlators
  - Provides longer integration at each point white still providing 5 usec. acquisition

Question 7: Multi-path Robustness

- The performance in a multi-path environment is one of the critical features for a high-rate UWB PHY. The MBOK proposal has not clearly stated the receiver requirements in handling the multi-path channels and the system impairments that have been included in these simulations. Clarifications on the following points would help us understand the MBOK proposal better.

- (a) Simulation results presented in document 15-03-0449-03-003a shows that the 200 Mbps and 480 Mbps modes reach an error floor in a multi-path channel environment in the presence of realistic system impairments. If you do not agree with this conclusion, can you present detailed simulation results to the contrary and the assumptions on system impairments that are made?

Response 7: Multi-path Robustness

- The simulation shown in 15-03-0449-03-003a failed to take into account that a well-designed DS-UWB receiver will use an equalizer
- The equalizer for DS-UWB has been proven as it is operational in a working chip set
- It is NOT a major block, but accounts for only 3% of the die size and 3% of the power
  - See complexity analysis in Question 3 Response
- The two specific modes (200 and 480 Mbps) to which the question above refers have been superceded in the current DS-UWB proposal
- Performance results are provided in Question 3 response

Question 7: Multi-path Robustness (Cont)

(b) All the multi-path performance results presented in the MBOK proposal assumes a 150 finger RAKE. Does an implementer have to implement this many RAKE fingers to obtain a performance capable of meeting the selection criterion document? If not, can you provide detailed simulation results to justify how many RAKE fingers are needed?

- The response to Question 3 showed simulation results for a 16-finger rake implementation that exceed the requirements of the selection criteria.

- Given the above, DS-UWB implementations do not require 150 rake fingers to meet the selection criteria requirements. The 150-finger performance referred to above was for an ultra-simple 1-bit ADC implementation that actually required ZERO multipliers for the rake.

Question 7: Multi-path Robustness (Cont)

(c) In a presentation by the MBOK proponents in January 2004, it was stated that an equalizer, especially a DFE, is required at the receiver to ensure that there is no error floor. However no simulation results were presented to show the system performance when an equalizer is used, the complexity requirements of the equalizer or whether a DFE is feasible (from a complexity perspective) for the 64-BOK mode. Can you present detailed simulation results when an equalizer is used and provide additional information on the expected complexity (gate count) of the equalizer and also address issues related to equalizer training?

The response to Question 3 shows simulation results for a 16-finger rake implementation that demonstrates the effectiveness of a DFE

Complexity estimates for a DFE and linear equalizer are also presented

Note: 64-BOK is no longer a supported mode for the DS-UWB proposal. The discussion of a 64-BOK DFE is unnecessary at this time.

Question 7: Multi-path Robustness (Cont)

(d) The MBOK proposal from May 2003 states that DFE error propagation is not an issue for UWB multi-path channels. This is justified by simulations performed at a very high SNR of 9.6 dB and 12.6 dB. This ignores the fact that the MBOK proposal has an FEC and operates at an E_b/N_0 of ~4 dB for a BER of 10^{-5}. In addition, the DFE uses the tentative decisions generated at the channel SNR, which corresponds to ~1 dB for a Rate ½ code. Can you provide results characterizing the impact of DFE error propagation at the realistic operating point?

The response to Question 3 shows simulation results for a 16-finger rake implementation that demonstrates the effectiveness of a DFE.

The results demonstrate that error propagation is not a significant issue for the channels and data rates analyzed.

Note: For the current DS-UWB proposal, the FEC would operate at a minimum of 5.0 dB E_b/N_o for a BER of 10^{-5}. The DFE decisions are made at the output of the slicer after the benefit of the code sequence processing gain (I.e. de-spreading), not at the channel SNR.

Question 7: Multi-path Robustness (Cont)

- (e) It has been stated by many, including the MBOK proponents that the transmitter back-off needs to be included in the link budget analysis and performance results. The MBOK proposal needs a theoretical transmitter back-off of ~2 dB for some of the modes (2-BOK, 4-BOK, etc). However, neither the link budget table nor the performance results seem to include this back-off. Can you provide results after including this theoretical back-off value?

- A link budget analysis is provided on the next slide
- It indicates the AWGN link margin for each proposed data rate
- The calculation included the worst case transmitter back-off values.
- Many of the data rates have a 0 dB back-off
  - The new DS-UWB proposal includes several modes where the ternary code has all bits=0 except for one
  - Such a code is perfectly white
- The back-off values are 1.9 dB for the worst-case ternary L=24 code and 1.1 dB for the worst-case ternary L=12 code

Response 7: Multi-path Robustness (Cont)

	DS-UWB 28 Mbps	DS-UWB 55 Mbps	DS-UWB 110 Mbps	DS-UWB 220 Mbps	DS-UWB 500 Mbps	DS-UWB 1000 Mbps
FEC Rate	0.50	0.50	0.50	0.50	0.75	0.75
Spreading code length	24.0	12.0	6.0	3.0	2.0	1.0
Data Rate (Mbps)	27.6	55.3	110.5	221.0	497.3	994.5
Baseline Tx Power (dBm)	-10.0	-10.0	-10.0	-10.0	-10.0	-10.0
Tx power w/ back-off (dBm)	-11.9	-11.1	-10.0	-10.0	-10.0	-10.0
Total Path Loss (dB)	64.2	64.2	64.2	56.2	50.2	50.2
Received Power (dBm)	-76.1	-75.3	-74.2	-66.3	-60.2	-60.2
Noise Power per Bit	-99.6	-96.6	-93.6	-90.6	-87.0	-84.0
Noise Figure (dB)	6.6	6.6	6.6	6.6	6.6	6.6
Total Noise Power (dBm)	-93.0	-90.0	-87.0	-84.0	-80.4	-77.4
Code Gain (dB)	4.6	4.6	4.6	4.6	3.6	3.6
Required Eb/No (dB)	5.0	5.0	5.0	5.0	6.0	6.0
Implementation Loss (dB)*	2.5	2.5	2.5	2.5	3.0	3.0
Link Margin (dB)	9.4	7.2	5.2	10.2	11.2	8.2
Sensitivity (dBm)	-85.5	-82.5	-79.5	-76.5	-71.4	-68.4
Margin Reference Range (m)	10	10	10	4	2	2
AWGN Range (m)	29.4	22.8	18.3	12.9	7.3	5.1

*Values for implementation loss used here are for comparison purposes, actual values are lower

Question 7: Multi-path Robustness (Cont)

(f) Our simulation results clearly show that the 112 Mbps mode out performs the 114 Mbps mode and the 224 Mbps mode out performs the 200 Mbps mode. In addition, the rate difference between 112 Mbps and 114 Mbps and 200 Mbps and 224 Mbps is negligible and therefore does not seem to add any value to the system. Have the authors considering dropping the 114 and 200 Mbps mode from the proposal? Before any comprise can occur, this proposal needs to be optimized.

The new proposal is a much better match to the majority of applications, particularly streaming multi-media for handheld devices.

The two specific modes (114 and 200 Mbps) you have suggested dropping have, in fact, been superceded.

Question 8: Complexity

(a) Please provide a complete complexity analysis for the reference receiver used to generate the system performance results. When providing digital gate count, also specify the clock frequency that is assumed.

Component	16-Finger Architecture (03/449r0 Estimate) **PREVIOUS PROPOSAL**	DS-UWB 16-Finger Rake Architecture **IMPROVED PROPOSAL**	DS-UWB 32-Finger Rake Architecture **IMPROVED PROPOSAL**
Matched filter [rake]	205K	26K	45K
Viterbi decoder	108K	54K	54K
Reed-Solomon decoder	20K	Not needed	Not needed
MBOK demodulator	61K	Not needed	Not needed
Synchronization	177K	30K	30K
Channel estimation	24K	24K	24K
Other Miscellaneous including RAM	30K	30K	30K
Equalizer	Not used	20K	20K
Total gates @ 85.5 MHz	604K	**184K**	**203K**

Question 8: Complexity (cont)

(b) Document 802-15-03/334r5 presents the complexity of a CIDD for a K = 3 convolutional code as 175 K gates. However, the proposal assumes the use of a K = 4 convolutional code. Can you present complexity results that are consistent with the modes that are described in the proposal?

CIDD is one possible decoder implementation for an optional receiver mode.

The k=4 and k=6 FEC encoders that are mandatory require only a few gates.

The complexity of a k=4 decoder is about 13k gates.

Decode that provides soft outputs (required for CIDD) has 1.5x higher complexity

Complexity estimates for K=6 and K=4 will be provided.

For iterated decoding, multiple iterations of the decode can be performed using multiple decoders. For N stages (@ 85.5 MHz):

N x (1.5 x 13k gates + 500 gates for 4-BOK likelihoods) = N x 20k gates

Question 9: Coexistence

(a) The selection criteria document requires either simulations or analysis based results for the distance at which the UWB receiver can tolerate other in-band/out-of band devices like IEEE 802.11a, IEEE 802.11b, Bluetooth, etc. The M-BOK proposal states that these are out-of-band devices and hence would not impact the UWB system. However, this assumes infinite out-of-band rejection at the UWB receiver which is not practical. Can you provide results on the minimum distance at which these devices can be tolerated and the corresponding assumptions on the front-end filter at the UWB receiver?

- The measured separation distances are 3 inches or less
  - For all of the devices listed
  - For other devices like 5.8 GHz and 2.4 GHz cordless phones.
- The actual separation distances are so small that they are in the near-field of the antennas where simulation and analysis breaks down.
- The front-end filter is a very straight forward 7-pole bandpass filter

Co-existence

	Microwave Oven	Bluetooth & IEEE 802.15.1 Interferer	IEEE 802.11b & IEEE 802.15.3 Interferer	IEEE 802.11a Interferer	IEEE 802.15.4 Interferer (2.45 GHz)
Max. tolerable interferer power at the slicer input	-82.3	-82.3	-82.3	-82.3	-82.3
Processing gain (code rate of 1/2 + L=6 code)	10.8	10.8	10.8	10.8	10.8
Minimum base-band filter attenuation	30.0	30.0	30.0	30.0	30.0
Front-end pre-select filter attenuation	40.0	40.0	40.0	30.0	40.0
Max. tolerable interferer power at the antenna	-1.5	-1.5	-1.5	-11.5	-1.5
Interferer power at 1m separation	-23.2	-40.0	-20.0	-31.9	-40.2
Minimum margin	21.7	38.5	18.5	20.4	38.7
Tolerable separation required (meters)	0.08	0.01	0.12	0.10	0.01

Question 10: Clear Channel Assessment

(a) Document 802.15-03/343r1, which was presented in September 2003, demonstrates that the MBOK proposal has great difficulty with clear channel assessment in a multi-path environment. In addition, CCA seems to work for only CM1 channel environment for ranges up to 4 meters. In addition, this does not take into account any crystal mismatches between the various DEVs. Could you state the assumptions that were made in generating the CCA performance results? Do you have any mechanism to ensure improved CCA performance? If so, can you provide details?

- Previous results using a squaring circuit were motivated by a desire for a CCA function that could simultaneously detect signal activity in multiple piconets using offset center frequencies
- The effectiveness of this technique is degraded in multipath
- Techniques are available to enhance the effectiveness of this approach
    - Essentially the same as the widely-studied problem of detecting a sinusoid in noise
- DS-UWB can, of course, provide CCA indication based on packet detection with high reliability.