IEEE P802.11
Wireless LANs

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| DMG PHY CID Resolution I |
| Date: 2018-07-03 |
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|  |  |  |  |  |

Abstract

This document proposes resolution to the following DMG PHY related CID: 1023, 1024, 1351, 1407. All references are to RevMD D1.0 except for CDMG proposed changes which are in reference to RevMD D1.5.

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| --- | --- | --- | --- | --- |
| 1023 | 2861.30 | 20.4.3.3.3 | In step 4) there is a division by (N\_CW-1). This I a problem when N\_CW=1. Need to deal with this case | a submission will be provided |

Proposed Resolution: **Reject**

Discussion:

Since the text specifically referes to second or subsequent LDPC codewords the formula does not apply when they do not exist, so that no change is required

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1024 | 2861.54 | 20.4.3.3.4 | The note "The scrambling and coding process does not affect the Differential Encoder initialization field of the DMG control mode header. However, a typical receiver implementation does not recover d(0) and hence does not recover the value of this field" is incorrect. Begin a part of the header, the bit must be decoded correctly to be received correctly. The LDPC decoder will create a value for this bit even if it the lower parts of the receiver do not. | Replace the text of the note with: "The scrambling process does not affect the Differential Encoder Initialization field of the DMG control mode header" |

Proposed Resolution: **Accept**

Discussion:

The issue is with the fact that the bit is part of the header, and therefore needs to be decoded correctly. In the 11ad, this bit was set to 0, which made sense, as it is difficult to decode it. However, 802.11-16 changed it to an arbitrary value. This means it must be decoded. The coding process does not directly affect the bit, because the LDCP code is a systematic code in which the parity bits are added to each codeword. It is also incorrect that the receiver does not recover d(0). It must recover it to get passing CRC in the header.

***Editor Modify the note in P2861L54-57 as follows:***

NOTE—The scrambling ~~and coding~~ process does not affect the Differential Encoder Initialization field of the DMG control mode header. ~~However, a typical receiver implementation does not recover d(0) and hence does not recover the value of this field.~~

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 1351 | 2845.01 | 1 | 20 | It's a bad idea for the scrambler state to be all-zeroes | In Table 20-11 append "May be set to anynonzero value." after "Bits X1-X4 of the initial scrambler state." In Table 20-13 append "May be set to anynonzero value." after "Bits X1-X7 of the initial scrambler state." |

Proposed Resolution: **Revised**

Discussion:

In 20.3.9 (which discusses the scrambling) we have the text: “For each PPDU, the transmitter shall select a nonzero seed value for the scrambler (bits x1 to(#240) x7). The seed value should be selected in a pseudorandom fashion.”. In control mode there is no need to set one of the 4 bits to 1, because 3 bits are always set to 1. In SC PHY, the mentioned text already covers the issue, and adding such text to the header table will create complications with related text below the table, as some scrambler bits are used in some cases for signaling.

***Editor: Modify the scrambler initialization line in table 20-11 (DMG control mode header fields)***

|  |  |  |  |
| --- | --- | --- | --- |
| Scrambler Initialization | 4 | 1 | Bits X1-X4 of the initial scrambler state (see 20.4.3.3.2 (Scrambler)) |

***Editor: Modify the scrambler initialization line in table 20-13 (*DMG SC mode header fields*)***

|  |  |  |  |
| --- | --- | --- | --- |
| Scrambler Initialization | 7 | 1 | Bits X1-X7 (see 20.3.9) |

***Editor: Modify the scrambler initialization line in table 24-6 (*CDMG control mode header fields)**

|  |  |  |  |
| --- | --- | --- | --- |
| Scrambler Initialization | 4 | 1 | Bits X1-X4 of the initial scrambler state (see 20.3.9 (Scrambler)) |

***Editor: Modify the scrambler initialization line in Table 24-8 (CDMG SC mode header fields)***

|  |  |  |  |
| --- | --- | --- | --- |
| Scrambler Initialization | 7 | 1 | Bits X1-X7 (see 20.3.9) |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 1407 | 2888.52 | 52 | 20.1 | The delta function is not defined | Add "where $delta(x) is 1 if x is 0 and 0 otherwise" at line 58 |

Proposed Resolution: **Revised**

***Editor: Insert the following text at P2888L58***

where $δ\left(n\right)=\left\{\begin{matrix}1&n=0\\0&otherwise\end{matrix}\right.$

**Issue without CID**

**Discussion:**

In Figure 10-80 Example of using BRP setup subphase to set up subsequent MIDC subphase in the DTI (D1.5) there is one instance of in which the field name TXSS-FBCK-REQ is misspelled as TX-FBCK-REQ.

We propose to fix it.

***Editor: in Figure 10-80 Example of using BRP setup subphase to set up subsequent MIDC subphase in the DTI), replace “TX-FBCK-REQ” with “TXSS-FBCK-REQ”.***



**References:**