IEEE P802.11
Wireless LANs

|  |
| --- |
| Proposed spec text for D0.1 |
| Date: 2018-03-01 |
| Author(s): |
| Name | Affiliation | Address | Phone | email |
| Alfred Asterjadhi | Qualcomm Inc. | 5775 Morehouse Dr, San Diego, CA 92109 | +1-858-658-5302 | aasterja@qti.qualcomm.com |
|  |  |  |  |  |
|  |  |  |  |  |

Abstract

This submission proposes draft for WUR frame format for the following portions of the SFD:

1. *[Assigned D0.1] The WUR frame has a Frame Check Sequence (FCS) that carries the CRC of the frame:*
* *Length and computation of FCS is TBD.*

*[Motion 6, Sep 2017, see [4] [41]]*

1. *[Assigned D0.2] The FCS additionally embeds BSSID information:*
	* *How to embed the BSSID information in the FCS is TBD*
	* *It is not applicable for pre-association WUR frames*

*[Motion 5, Nov 2017, see [6] [52]]*

1. *[Assigned D0.2] The method for embedding BSSID info. in the FCS is as follows:*
* *Compute the CRC assuming that Embedded BSSID field is present*
* *Embedded BSSID field is not present in the transmitted WUR frame*
* *The contents of the Embedded BSSID field is TBD*

*[Motion 2, Jan 2018, see [7] [53]]*

1. *[Assigned D0.2] The CRC of WUR frames shall use one of the following CRC engines from IEEE 802.11*
* *32-bit CRC, 16-bit CRC, 8-bit CRC*

*[Motion 1, Jan 2018, see [7] [53]]*

Revisions:

* Rev 0: Initial version of the document.
* Rev 1: incorporated suggestions received during the presentation (highlighted in green)
* Rev 2: Added motion text.

MOTION 1

Move to incorporate the changes proposed in 11-18/0414r2 to the IEEE802.11ba D0.1?

Interpretation of a Motion to Adopt

A motion to approve this submission means that the editing instructions and any changed or added material are actioned in the TGax Draft. This introduction is not part of the adopted material.

***Editing instructions formatted like this are intended to be copied into the TGba Draft (i.e. they are instructions to the 802.11 editor on how to merge the text with the baseline documents).***

***TGba Editor: Editing instructions preceded by “TGba Editor” are instructions to the TGba editor to modify existing material in the TGba draft. As a result of adopting the changes, the TGba editor will execute the instructions rather than copy them to the TGba Draft.***

**TGba Editor: *Change the paragraphs below of this subclause as follows (#NO CID):***

9.10.1 Basic components

Each Wake-Up Radio (WUR) frame consists of the following basic components:

—A *MAC header*, which comprises frame control, address, and type dependent (TD) control fields;

—A variable-length *frame body*, which, if present, contains information specific to the frame *type*;

—An *FCS*, which contains an IEEE TBD-bit CRC.

9.10.2 General WUR frame format

Figure 9-747a (WUR frame format) depicts the general MAC frame format for WUR frames.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | B0   B7 | B8  B19 | B20  B31 |  |  |
|  | Frame Control | Address | TD Control | Frame Body | FCS |
| Bits: | 8 | 12 | 12 | variable | *TBD*  |
|  | Figure 9-747a – WUR frame format |

**9.10.2.5 Frame Check Sequence (FCS) field**

The FCS field contains a *TBD*-bit CRC. The FCS is calculated over all the fields of the Frame Control, Address, TD Control, Frame Body field (if present), and Embedded BSSID field (if present). These fields are referred to as the *calculation fields*.

The Frame Body field is present in the *calculation fields* only when the WUR frame is a variable-length WUR frame (9.10.2.4 (Frame Body field)); otherwise, the Frame Body field is not present.

The Embedded BSSID field is present in the *calculation fields* only for WUR frames that are post-association WUR frames; otherwise the Embedded BSSID field is not present. The Embedded BSSID field, if present, is the last field of the *calculation fields*. The size and contents of the Embedded BSSID field is *TBD*.

The FCS is the 1s complement of the remainder generated by the modulo 2 division of the *calculation fields* by the polynomial *TBD*, where the shift-register state is preset to all 1s.

NOTE—The order of transmission of bits within the FCS field is defined in 9.2.2 (Conventions).

The *calculation fields* are processed in the order they would have been transmitted.

A schematic of the processing is shown in Figure X (CRC-*TBD* implementation), where the SERIAL DATA INPUT consists of the *calculation fields (BL, BL-1…, B1, B0),* with *BL* being the most significant bit of the *calculation fields*.

NOTE – THE CRC in the FCS is one of the CRC-8, CRC-16, or CRC-32. Which of these ones is still *TBD*.