IEEE P802.11
Wireless LANs

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| Clarification of the Scrambler Subclause |
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Abstract

This document proposes editorial changes to the subclause 30.5.9.3 Scrambler.

* + - 1. Scrambler
				1. Scrambler for Data field, L-Header, EDMG-Header-A, and EDMG-Header-B data bits and non-EDMG SC MCS1 coded bits

The Data field, L-Header, EDMG-Header-A, and EDMG-Header-B data bits and non-EDMG SC MCS1 coded bits (see 20.6.3.2.3) shall be scrambled applying scrambler defined in 20.3.9.

The scrambling of the Data field of an SU PPDU continues the scrambling of the L-Header and the EDMG-Header-A fields. The initial seed value is defined in the L-Header field.

The scrambling of the Data field of an MU PPDU is performed on a per user basis and continues the scrambling of the EDMG-Header-B field with reset of the seed value. The initial seed value is defined in the EDMG-Header-B field on a per user basis.

For an SU EDMG A-PPDU, the initial seed value is defined in the L-Header field and the scrambling of the *iPPDU*th PPDU continues the scrambling of (*iPPDU* – 1)th PPDU with no seed reset.

For a non-EDMG SC MCS1 scrambling and the codeword length equal to 672 bits, the 168 repeated systematic bits shall be scrambled in turn starting from bit 1 and ending with bit 168 (see 20.6.3.2.3). For each codeword, the transmitter shall reload the seed value to all ones (bits x1 through x7).

* + - * 1. Scrambler for EDMG-Header-A in SU EDMG A-PPDU, EDMG-Header-B, and EDMG SC MCS1 coded bits

The EDMG Header-A transmitted in SU EDMG A-PPDU (excluding the first PPDU) coded bits, EDMG-Header-B coded bits, and repeated systematic part of an LDPC codeword using EDMG SC MCS1 encoding shall be scrambled by XORing each bit in turn with a length 127 periodic sequence generated by polynomial .The generation of the sequence and the XOR operation are shown in Figure 144. Each data or header bit is XORed with the scrambler output  and the scrambler content is shifted once. The 127-bit sequence generated repeatedly by the scrambler shall be (leftmost used first), 01010100 11001110 11101001 01100011 01111011 01011011 00100100 01110000 10111110 01010111 00110100 01001111 00010100 00110000 01000000 1111111, when the all ones (bits x1 through x7).initial state is used.



Figure 144—EDMG-Header-A in SU EDMG A-PPDU, EDMG-Header-B, and EDMG SC MCS1 coded bits sequence scrambler

For an EDMG-Header-A of an SU EDMG A-PPDU (excluding the first PPDU) and EDMG SC mode, the scrambling of the coded bits starts at the 225th bit and ends at the (*NSTS* × 896 × *NCB*)th bit (see 30.5.7). The initial seed value is equal to all ones (bits x1 through x7).

For an EDMG-Header-A of an SU EDMG A-PPDU (excluding the first PPDU) and EDMG OFDM mode, the scrambling of the coded bits starts at the 225th bit and ends at the (*NSTS* × 4 × *NSD*)th bit (see 30.6.6). The initial seed value is equal to all ones (bits x1 through x7).

For an EDMG-Header-B scrambling and EDMG SC mode, the scrambling of the coded bits starts at the 225th bit and ends at the (*NSTS* × 448 × *NCB*)th bit (see 30.5.6). The initial seed value is equal to all ones (bits x1 through x7).

For an EDMG-Header-B scrambling and EDMG OFDM mode, the scrambling of the coded bits starts at the 225th bit and ends at the (*NSTS* × 2 × *NSD*)th bit (see 30.6.5). The initial seed value is equal to all ones (bits x1 through x7).

For an EDMG SC MCS1 scrambling and the codeword length equal to 672 bits, the 168 repeated systematic bits shall be scrambled in turn starting from bit 1 and ending with bit 168. For EDMG SC MCS1 scrambling and the codeword length equal to 1344 bits, the 336 repeated systematic bits shall be scrambled in turn starting from bit 1 and ending with bit 336. For each codeword, the transmitter shall reload the seed value to all ones (bits x1 through x7).

**References:**

1. Draft P802.11ay\_D1.0