IEEE P802.11
Wireless LANs

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| Clarification of the Scrambler Subclause |
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Abstract

This document proposes editorial changes to the subclause 30.5.9.3 Scrambler. The motivation for the proposed changes is to reflect all usages of the scrambler (MCS 1, EDMG-Header-A, and EDMG-Header-B).

* + - 1. Scrambler
				1. Data scrambler

The operation of the scrambler applied for the data bits is defined in 20.3.9. The scrambling of the PSDU of an SU PPDU continues the scrambling of the L-Header and the EDMG-Header-A fields. The initial seed value is defined in the L-Header field.

The scrambling of the PSDU of an MU PPDU is performed on a per user basis and continues the scrambling of the EDMG-Header-B field with reset of the seed value. The initial seed value is defined in the EDMG-Header-B field on a per user basis.

For an EDMG A-PPDU, the initial seed value is defined in the L-Header field and the scrambling of the iPPDUth PPDU continues the scrambling of (iPPDU – 1)th PPDU with no seed reset.

* + - * 1. Scrambler for EDMG SC MCS1, EDMG-Header-B, and EDMG-Header-A for EDMG A-PPDU

The repeated systematic part of a LDPC codeword using EDMG SC MCS1 encoding, EDMG-Header-B, and EDMG Header-A for EDMG A-PPDU shall be scrambled by XORing each bit in turn with a length 127 periodic sequence generated by polynomial .The generation of the sequence and the XOR operation are shown in Figure 144. Each data or header bit is XORed with the scrambler output  and the scrambler content is shifted once.



Figure 144—EDMG SC MCS1, EDMG-Header-B, and EDMG-Header-A for EDMG A-PPDU sequence scrambler

For EDMG SC MCS1 scrambling and the codeword length equal to 672 bits, the 168 repeated systematic bits shall be scrambled in turn starting from bit 1 and ending with bit 168. For EDMG SC MCS1 scrambling and the codeword length equal to 1344 bits, the 336 repeated systematic bits shall be scrambled in turn starting from bit 1 and ending with bit 336. For each codeword, the transmitter shall reload the seed value to all ones (bits x1 through x7).

For EDMG-Header-B scrambling and EDMG SC mode, the header bits scrambling starts at the 225th bit and ends at the (*NSTS* × 448 × *NCB*)th bit (see 30.5.6). The initial seed value is equal to all ones (bits x1 through x7).

For EDMG-Header-B scrambling and EDMG OFDM mode, the header bits scrambling starts at the 225th bit and ends at the (*NSTS* × 2 × *NSD*)th bit (see 30.6.5). The initial seed value is equal to all ones (bits x1 through x7).

For EDMG-Header-A of EDMG A-PPDU and EDMG SC mode, the scrambling starts at the 225th bit and ends at the (*NSTS* × 896 × *NCB*)th bit (see 30.5.7). The initial seed value is equal to all ones (bits x1 through x7).

For EDMG-Header-A of EDMG A-PPDU and EDMG OFDM mode, the scrambling starts at the 225th bit and ends at the (*NSTS* × 4 × *NSD*)th bit (see 30.6.6). The initial seed value is equal to all ones (bits x1 through x7).

**References:**

1. Draft P802.11ay\_D1.0