IEEE P802.11  
Wireless LANs

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [Draft text of ACK/BA transmission in mmWave Distribution Networks] | | | | |
| Date: 2018-01-8 | | | | |
| Author(s): | | | | |
| Name | Affiliation | Address | Phone | email |
| Lochan Verma | Qualcomm |  |  | lverma@qti.qualcomm.com |
| George Cherian | Qualcomm |  |  | gcherian@qti.qualcomm.com |
| Solomon Trainin | Qualcomm |  |  | strainin@qti.qualcomm.com |
| Carlos Cordeiro | Intel |  |  | carlos.cordeiro@intel.com |
| Oren Kedem | Intel |  |  | oren.kedem@intel.com |
| Carlos Aldana | Intel |  |  | carlos.h.Aldana@intel.com |
| Djordje Tujkovic | Facebook |  |  | djordjet@fb.com |
| Nabeel Ahmed | Facebook |  |  | nabeel@fb.com |
| Gang Lu | Facebook |  |  | ganglu@fb.com |
| Praveen Gopala | Facebook |  |  | gopalap@fb.com |

Abstract

This document proposes amendment to the transmission rules for ACK/BA and many immediate control response frames in accordance with 17/1647r0 (Ack/BA for mmWave Distribution Network).

**9.2.4.5.4 Ack Policy subfield**

***Add the following text to Table 9-9 (Ack Policy subfield in QoS Control field of QoS Data frames)***

|  |  |  |
| --- | --- | --- |
| Bits in QoS Control field | | Meaning |
| Bit 5 | Bit 6 |
| 0 | 0 | Normal Ack or Implicit Block Ack Request.  In a frame that is a non-A-MPDU frame or S-MPDU where either the originator or the addressed recipient does not support fragment BA procedure:  The addressed recipient returns an Ack or QoS +CF-Ack frame after a short interframe space (SIFS) period, according to the procedures defined in 10.3.2.10 (Acknowledgement procedure) and 10.24.3.5 (HCCA transfer rules). A non-DMG STA sets the Ack Policy subfield for individually addressed QoS Null (no data) frames to this value.  The addressed recipient that is a DMG STA operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)), returns an Ack frame according to the procedures defined in 10.3.2.9 (Acknowledgement procedure).  In a non-A-MPDU frame or S-MPDU containing a fragment where both the originator and the addressed recipient support the fragment BA procedure:  The addressed recipient returns an NDP BlockAck frame after a SIFS, according to the procedure defined in 10.3.2.11 (Fragment BA procedure.  Otherwise:  The addressed recipient returns a BlockAck frame, either individually or as part of an A-MPDU starting a SIFS after the PPDU carrying the frame, according to the procedures defined in 10.3.2.10 (Acknowledgement procedure), 10.26.7.5 (Generation and transmission of BlockAck frames by an HT STA or DMG STA), 10.26.8.3 (Operation of HT-delayed block ack), 10.30.3 (Rules for RD initiator), 10.30.4 (Rules for RD responder), 10.34.3 (Explicit feedback beamforming).  The addressed recipient that is a DMG STA operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)), returns a BlockAck frame, either individually or as part of an A-MPDU according to the procedures defined in 10.24.7.5 (Generation and transmission of BlockAck frames by an HT STA or DMG STA). |
| -- | -- | -- |

**10.3.2.9 Acknowledgement procedure**

***Add the following text***

Otherwise, upon reception of a frame that requires acknowledgement and, for an AP, with the To DS subfield equal to 1, a STA shall transmit an Ack or BlockAck frame after a SIFS, without regard to the busy/idle state of the medium. (See Figure 10-10 (Individually addressed data/Ack/BA frame).)

A non-AP and non-PCP STA operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)), upon reception of a frame that requires acknowledgement shall transmit an Ack or BlockAck frame at the start of the earliest occurring TDD slot the non-AP and non-PCP STA is assigned to, with access permission of the TDD slot set to simplex RX TDD slot, and with slot category of the TDD slot set to Basic TDD slot, as indicated in the TDD Slot Schedule element (see 9.4.2.268).

A DMG AP or DMG PCP operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)), upon reception of a frame from a non-AP and non-PCP STA that requires acknowledgement and, for an DMG AP, with the To DS subfield equal to 1, shall transmit an Ack or BlockAck frame at the start of the earliest occurring TDD slot the non-AP and non-PCP STA is assigned to, with access permission of the TDD slot set to simplex TX TDD slot, and with slot category of the TDD slot set to Basic TDD slot, as indicated in the TDD Slot Schedule element (see 9.4.2.268).

After transmitting an MPDU that requires an Ack or BlockAck frame as a response (see Annex G), the STA shall wait for an AckTimeout interval, with a value of aSIFSTime + aSlotTime + aRxPHYStartDelay, starting at the PHY-TXEND.confirm primitive. If a PHY-RXSTART.indication primitive does not occur during the AckTimeout interval, the STA concludes that the transmission of the MPDU has failed, and this STA shall invoke its backoff procedure upon expiration of the Ack Timeout interval.

A non-AP and non-PCP STA operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)) has AckTimeout interval value equal to the duration from the PHY-TXEND.confirm primitive of the current frame to the end of the earliest occurring TDD slot the addressed recipient of the MPDU is assigned to, with access permission of the TDD slot set to simplex TX TDD slot, and with slot category of the TDD slot set to Basic TDD slot, as indicated in the TDD Slot Schedule element (see 9.4.2.268).

A DMG AP or DMG PCP operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)) has AckTimeout interval value equal to the duration from the PHY-TXEND.confirm primitive of the current frame to the end of the earliest occurring TDD slot the addressed recipient of the MPDU is assigned to, with access permission of the TDD slot set to simplex RX TDD slot, and with slot category of the TDD slot set to Basic TDD slot, as indicated in the TDD Slot Schedule element (see 9.4.2.268).

**10.24.7.5 Generation and transmission of BlockAck frames by an HT STA or DMG STA**

Except when operating within a PSMP exchange, a STA that receives a PPDU that contains a BlockAckReq frame in which the Address 1 field matches its MAC address during either full-state operation or partial-state operation shall transmit a PPDU containing a BlockAck frame that is separated on the WM by a SIFS from the PPDU that elicited the BlockAck frame as a response. A STA that receives an A-MPDU that contains one or more MPDUs in which the Address 1 field matches its MAC address with the Ack Policy field equal to Normal Ack (i.e., implicit block ack request) during either full-state operation or partial-state operation shall transmit a PPDU containing a BlockAck frame that is separated on the WM by a SIFS from the PPDU that elicited the BlockAck frame as a response.

A non-AP and non-PCP STA operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)), that receives a PPDU that contains a BlockAckReq frame in which the Address 1 field matches its MAC address during either full-state or partial-state operation shall transmit a PPDU containing a BlockAck frame starting at the earliest occurring TDD slot the non-AP and non-PCP STA is assigned to, with access permission of the TDD slot set to simplex RX TDD slot, and with slot category of the TDD slot set to Basic TDD slot, as indicated in the TDD Slot Schedule element (see 9.4.2.268).

A DMG AP or PCP operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)), that receives from a non-AP and non-PCP STA, a PPDU that contains a BlockAckReq frame in which the Address 1 field matches its MAC address during either full-state or partial-state operation shall transmit a PPDU containing a BlockAck frame starting at the earliest occurring TDD slot the non-AP and non-PCP STA is assigned to, with access permission of the TDD slot set to simplex TX TDD slot, and with slot category of the TDD slot set to Basic TDD slot, as indicated in the TDD Slot Schedule element (see 9.4.2.268).

A non-AP and non-PCP STA operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)), that receives an A-MPDU that contains one or more MPDUs in which the Address 1 field matches its MAC address with the Ack Policy field equal to Normal Ack (i.e., implicit block ack request) during either full-state operation or partial-state operation shall transmit a PPDU containing a BlockAck frame starting at the earliest occurring TDD slot the non-AP and non-PCP STA is assigned to, with access permission of the TDD slot set to simplex RX TDD slot, and with slot category of the TDD slot set to Basic TDD slot, as indicated in the TDD Slot Schedule element (see 9.4.2.268).

A DMG AP or PCP operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)), that receives from a non-AP and non-PCP STA, an A-MPDU that contains one or more MPDUs in which the Address 1 field matches its MAC address with the Ack Policy field equal to Normal Ack (i.e., implicit block ack request) during either full-state operation or partial-state operation shall transmit a PPDU containing a BlockAck frame starting at the earliest occurring TDD slot the non-AP and non-PCP STA is assigned to, with access permission of the TDD slot set to simplex TX TDD slot, and with slot category of the TDD slot set to Basic TDD slot, as indicated in the TDD Slot Schedule element (see 9.4.2.268).

**10.36.6.2.2 SP with TDD Channel Access**

A DMG AP or DMG PCP shall set the Allocation Type subfield to 0 and the TDD Applicable SP subfield to 1 in an Allocation field within an Extended Schedule element to indicate a TDD SP allocation.

When allocating a TDD SP, the AP or PCP shall set both of the Source AID and Destination AID subfields in the corresponding Allocation field to 0.

If an Extended Schedule element includes at least one TDD SP, a DMG PCP or DMG AP shall include the Extended Schedule element in each transmitted DMG Beacon frame.

The structure of TDD SP is shown in Figure 89. A TDD SP consists of one or more consecutive identical TDD intervals. A TDD interval comprises one or more TDD slot.



**Figure 89---Example of TDD SP**

The parameters of the TDD structure and guard times that are used within a TDD SP are defined by the TDD Slot Structure element. A DMG AP or DMG PCP shall transmit a TDD Slot Structure element to each DMG STA that is expected to transmit or receive during a TDD SP. The TDD Slot Structure element may be included in DMG Beacon or Announce frames transmitted by the DMG AP or DMG PCP.

A DMG STA shall not transmit during a TDD SP unless it receives a TDD Slot Schedule element that indicates it is assigned to at least one TDD slot within the TDD SP by the DMG AP or DMG PCP. The DMG AP or DMG PCP shall transmit the TDD Slot Schedule element to each DMG STA that is assigned to access the TDD SP through an Announce frame or Association Response frame before the time indicated by the value of the Slot Schedule Start Time within the element. Upon reception of a TDD Slot Schedule element, a DMG STA shall adopt the schedule within the element at the time indicated by the value of the Slot Schedule Start Time subfield within the element.

The type of a TDD slot can be one of simplex TX, simplex RX or unassigned. Except for an unassigned TDD slot where no transmissions shall occur, the behavior of a DMG AP or DMG PCP in a TDD slot is different from the behavior of a non-AP and non-PCP STA depending if the TDD slot is simplex TX or simplex RX:

* At the start of a simplex TX TDD slot, the DMG AP or DMG PCP should initiate transmissions addressed to the non-AP and non-PCP STA assigned to the TDD slot, and the non-AP and non-PCP STA that is assigned to this TDD slot shall be beamformed towards the AP or PCP and remain in the receive state for the duration of the TDD slot in order to receive transmissions from the AP or PCP.
* At the start of a simplex RX TDD slot, a non-AP and non-PCP STA that is assigned to the TDD slot shall initiate transmissions addressed to the AP or PCP, and the DMG AP or DMG PCP shall be beamformed towards the assigned STA and remain in receive state for the duration of the TDD slot in order to receive transmissions from the STA.

Adjacent TDD slots shall be separated in time by the guard times identified in Figure 89 and defined in the TDD Slot Structure element.

Each TDD slot has one slot category, namely, a Basic TDD slot or a Data-only TDD slot. In a Basic TDD slot the transmission of all frame types defined in 9.2.4.1.3 (Type and Subtype subfields) shall be allowed. In a Basic TDD slot the transmission of a Control frame and a Management frame should be given priority over transmission of other frame types. In a Data-only TDD slot, only Data frames shall be allowed.

The reverse direction protocol (see 10.28) shall not be used in a TDD SP.

A DMG STA operating in a TDD slot, shall not transmit following frames of type Control:

- Grant

- Grant Ack

- Poll

- RTS

- SPR

- DMG CTS

- DMG DTS

- CF-End

NOTE: DMG CTS-to-self frame transmission is not prohibited in a TDD slot.

**9.4.2.268 TDD Slot Schedule Element**

The TDD Slot Schedule element defines the access assignment of DMG STAs to TDD slots within a TDD SP (see 10.36.6.2). The format of the TDD Slot Schedule element is shown in Figure 9-xxx4.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Element ID | Length | Element ID Extension | Slot Schedule Control | Bitmap and Access Type Schedule | Slot Category Schedule |
| Octets | 1 | 1 | 1 | 7 |  |  |

**Figure 76---TDD Slot Schedule element format**

The Element ID, Length and Element ID Extension fields are defined in 9.4.2.1.

The Slot Schedule Control field is defined in Figure 77.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Channel Aggregation | BW | Slot Schedule Start Time | Number of TDD Intervals in the Bitmap | Allocation ID | Reserved |
| Bits | 1 | 8 | 32 | 10 | 4 | 1 |

**Figure 77--- Slot Schedule Control field format**

The Channel Aggregation and BW subfields are defined in Table 36.

The Slot Schedule Start Time subfield indicates the lower 4 octets of the TSF timer at the start of the first TDD interval in which the schedule takes effect.

The Number of TDD Intervals in the Bitmap subfield indicates the number of TDD intervals in the bitmap following the time indicated by the Slot Schedule Start Time subfield.

The Allocation ID subfield is set to the same value of the Allocation ID subfield in Allocation Control field of the Extended Schedule element describing the SP allocation.

The Bitmap and Access Type Schedule field defines the type of a TDD slot and the access permission of a DMG STA to the TDD slots covered by this bitmap. Each pair of consecutive 2 bits indicates the type and access permission of the TDD slot. A value of 00 (binary) indicates that the TDD slot is unassigned. A value of 01 (binary) indicates the STA is assigned to a simplex TX TDD slot. A value of 10 (binary) indicates the STA is assigned to a simplex RX TDD slot. Value 11 (binary) is reserved. The size of the Bitmap and Access Type Schedule field is a function of the value of the Number of TDD Slots per TDD Interval subfield in the TDD Slot Structure element, *M*, and the value of the Number of TDD Intervals in the Bitmap subfield, *Q*.

The Slot Category Schedule field defines the TDD slot category. Each pair of consecutive 2 bits indicates the frame type(s) that are allowed to be transmitted in the corresponding TDD slot defined by the Bitmap and Access Type Schedule field. A value of 00 (binary) indicates Basic TDD slot and a value of 01 (binary) indicates Data-only TDD slot. Values 10 (binary) and 11 (binary) are reserved. The size of the Slot Category Schedule field is a function of the value of the Number of TDD Slots per TDD Interval subfield in the TDD Slot Structure element, *M*, and the value of the Number of TDD Intervals in the Bitmap subfield, *Q*.

**10.24.7.7 Originator’s behavior**

A STA may send a block of data in a single A-MPDU where each Data frame has its Ack Policy field set to Normal Ack. The originator expects to receive a BlockAck frame response immediately following the A-MPDU if at least one Data frame is received without error.

The DMG STA originator operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)) expects to receive a BlockAck frame response in the earliest occurring TDD slot with slot category of the TDD slot set to Basic TDD slot as defined in **10.24.7.5 (**Generation and transmission of BlockAck frames by an HT STA or DMG STA)if at least one Data frame is received without error**.**

The DMG AP or PCP originator operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)) shall not transmit more than one MPDU or A-MPDU that has an Ack Policy of Normal Ack to a non-AP and non-PCP STA per each occurrence of a TDD slot the non-AP and non-PCP STA is assigned to, with access permission of the TDD slot set to simplex RX TDD slot, and with slot category of the TDD slot set to Basic TDD slot, as indicated in the TDD Slot Schedule element (see 9.4.2.268).  
The non-AP and non-PCP originator operating in an SP with TDD channel access (see 10.36.6.2.2 (SP with TDD Channel Access)) shall not transmit more than one MPDU or A-MPDU that has an Ack Policy of Normal Ack to a DMG AP or PCP per each occurrence of a TDD slot the DMG AP or PCP is assigned to, with access permission of the TDD slot set to simplex TX TDD slot, and with slot category of the TDD slot set to Basic TDD slot, as indicated in the TDD Slot Schedule element (see 9.4.2.268).

References:

1. 11-17-1640-00-00ay-draft-text-for-scheduling-for-mmwave-distribution-networks.docx
2. 11-17-1647-00-00ay-Ack/BA-for-mmWave-Distribution-Networks.pptx
3. IEEE P802.11ay/D1.0, Nov 2017