IEEE P802.11
Wireless LANs

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| 30.5.7.3.3 Scrambler for MCS1 encoding |
| Date: 2017-06-13 |
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Abstract

This document proposes specification text for subclause 30.5.7.3.3 of the spec describing scrambler using in MCS1 encoding, [1].

**30.5.7.3.3 Scrambler for MCS1 encoding**

*Editor: add this section into the draft*

The repeated systematic part of LDPC codeword in MCS1 encoding shall be scrambled by XORing each bit in turn with a length 127 periodic sequence generated by polynomial . For the codeword length equal to 672 bits the 168 repeated systematic bits shall be scrambled in turn starting from bit 1 and ending with bit 168. For the codeword length equal to 1344 bits the 336 repeated systematic bits shall be scrambled in turn starting from bit 1 and ending with bit 336. The generation of the sequence and the XOR operation are shown in Figure 1.



Figure 1: MCS1 sequence scrambler

For each codeword, the transmitter shall reload the seed value to all ones (bits x1 through x7). Each data bit is then XORed with the scrambler output  and then scrambler content is shifted once.

**References:**

1. Draft P802.11ay\_D0.35