IEEE P802.11
Wireless LANs

|  |
| --- |
| 6.3.3.3.3 EDMG-Header-A Encoding and Modulation |
| Date: 2016-12-21 |
| Author(s): |
| Name | Affiliation | Address | Phone | email |
| Artyom Lomayev | Intel | Turgeneva 30, Nizhny Novgorod 603024, Russia | +7 (831) 2969444 | artyom.lomayev@intel.com |
| Yaroslav Gagiev | Intel  |  |  | yaroslav.p.gagiev@intel.com |
| Alexander Maltsev | Intel  |  |  | alexander.maltsev@intel.com |

Abstract

This document proposes specification text for sub-clause 6.3.3.3.3 of the SFD describing EDMG-Header-A encoding and modulation, [1]. It is proposed to remove current sub-clause 6.3.3.3.2.2 “Transmission.”

**6.3.3.3 EDMG portion of EDMG format preamble**

**6.3.3.3.1 General**

**6.3.3.3.2 EDMG-Header-A definition**

**6.3.3.3.3 EDMG-Header-A encoding and modulation**

For an EDMG SC mode PPDU or an EDMG OFDM mode PPDU, the EDMG-Header-A field is encoded and modulated using two SC blocks of 448 chips with 64 guard symbols. The bits are scrambled and encoded as follows:

1. The input 112 header bits are appended with 16 HCS bits calculated as defined in 20.3.7.
2. The header bits (including CRC) are scrambled as described in 20.3.9, starting from the first bit using a continuation of the scrambler bit sequence from the L-Header.
3. The scrambled bits are divided into two groups of 64 bits. The first 64 bits and the second 64 bits are each encoded and modulated as specified in steps 2-5 in 20.6.3.1.4.
4. Each of the resulting two SC blocks is prepended with 64 guard symbols. The second SC block is appended with appropriate number of guard symbols as described in sub-clause 6.5.6.2.

**References:**

1. 11-15-1358-09-00ay-11ay Spec Framework