

- IEEE 802.3cx specifies these capabilities in the Management Data Input/Output (MDIO) registers described in subclauses 45.2.1 (PMA/PMD), 45.2.2 (WIS), 45.2.3 (PCS), 45.2.4 (PHY XS), 45.2.5 (DTE XS), and 45.2.6 (TC) and via the management objects (which reference those MDIO registers) described in subclause 30.13 of IEEE 802.3cx.

1. For example, the Physical Coding Sublayer (PCS) sublayer has the following TimeSync PCS capability MDIO registers:

- a. 3.1800.13:12: Data delay measurement point ability
 - i. Indicates whether the PCS supports the beginning of the SFD or the beginning of the symbol after the SFD as the data delay measurement point (a.k.a. the PTP message timestamp point)
 - ii. A binary value of 11 indicates that both the beginning of the SFD and the beginning of the symbol after the SFD are supported as the data delay measurement point
 - iii. A binary value of x0 indicates that only the beginning of the SFD is supported as the data delay measurement point (this was the original specification for IEEE 802.3)
 - iv. A binary value of 01 indicates that only the beginning of the symbol after SFD is supported as the data delay measurement point
- b. 3.1800.11: Multilane ability
 - i. Indicates whether the IEEE 802.3cx method for dealing with dynamic multilane distribution and merging delays is supported
 - ii. A value of 1 indicates the IEEE 802.3cx method is supported and used
 - iii. A value of 0 indicates some other method is supported and used
- c. 3.1800.10: PCS dynamic path data delay ability
 - i. Indicates whether the IEEE 802.3cx method for accounting for the dynamic delays of alignment marker, codeword marker, and idle insertion and removal is supported
 - ii. A value of 1 indicates the IEEE 802.3cx method is supported and used
 - iii. A value of 0 indicates some other method, or no method, is supported and used
- d. 3.1800.3 and 3.1800.2: Tx/Rx path data delay with sub-nanosecond resolution
 - i. Indicates whether the PCS' path data delay is specified with sub-nanosecond resolution
 - ii. A value of 1 indicates that sub-nanosecond resolution is supported and used
 - iii. A value of 0 indicates that sub-nanosecond resolution is not supported

Prior to IEEE 802.3cx, the default value for all of the above PCS capability register bits was 0.

2. The TimeSync PCS configuration MDIO register is described below:
 - a. 3.1813.13 Data Delay Measurement Point
 - i. This configuration register is used to select either the beginning of the SFD or the beginning of the symbol after the SFD (if supported) as the data delay measurement point (a.k.a. the PTP message timestamp point)
 - ii. Reading this register shows whether the beginning of the SFD or the beginning of the symbol after the SFD (if supported, see above list item 1.a.ii) is selected as the data delay measurement point
 - iii. If supported (see above list item 1.a.ii), a value of 1 configures the PCS to use the beginning of the symbol after the SFD as the data delay measurement point
 - iv. A value of 0 configures the PCS to use the beginning of the SFD as the data delay measurement point

Question (2): Are the capabilities fixed or can they be configured?

- The selection of the data delay measurement point (a.k.a. the PTP message timestamp point) may be configurable (see above list item 2.a.i)
- Otherwise, if the IEEE 802.3cx capability is supported, then it is used. This is because the IEEE 802.3cx capability will either give better performance (see above list items 1.c.ii and 1.d.ii) and/or because the alternative is not defined (see above list items 1.b.iii and 1.c.iii).

Question (3): Are there other capabilities that IEEE 802.3 thinks are relevant for time-stamping accuracy?

- See the last 3 paragraphs (and the 2 numbered list items) at the end of 90A.7 in IEEE P802.3cx/D3.3. This draft (see attached document) has been submitted to IEEE RevCom for approval as an IEEE standard. Publication is expected later this year.

Please let us know if you have any follow-up questions regarding the IEEE P802.3cx Task Force's responses.

Sincerely,
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