Joint Capacitor Applications Paper Capacitor subcommittee (T&D)

Notes of interest

17 May 2011 in Lake buena vista, FL, The Switchgear Committee side met with 12 Members and 13 Guests.

Roy Presented the outline as developed in the Capacitor subcommittee (below).

It is primarily Section 3.1.1.1 “switchgear limitations” that Roy is seeking help on.

A “second showing” of the “prestrike arc shockwave theory” was given. (see C37.012 notes for details)

Mauricio Aristizabal Agreed to perform CFD analysis to check out the theory.

Other members will give a close review when the simulation work is complete.
A revised 3.1.1.1 will be sent out prior to the October 2011 meeting.

Grace & Peace

Roy Alexander

Joint Paper Outline

“Inductor applications for Capacitor switching technologies”

Capacitor - System Integration

1. Capacitor switching transient mitigation methods
    1.1 Controlled closing (synchronous closing)
    1.2 Temporary switching impedance
        1.2.1 closing resistor
        1.2.2 closing inductor

2. Outrush (what is it?) primarily an issue for a non capacitor breaker closing into a preexisting fault.

2.1 Outrush not impacted by closing control methods (neither is a restrike transient)

3. Fixed series inductors TLIs (Transient Limiting Inductors)
    3.1 uses
        3.1.1 limit inrush/outrush transients

3.1.1.1 Switchgear limits
3.1.1.1.1 capacitor switch
3.1.1.1.2 outrush to other breakers
3.1.1.2 transient ground rise
3.1.1.3 control system coupling
3.1.1.4 CT/LC secondary voltages
3.1.2 limit back to back restrike transients

3.2 drawbacks
3.2.1 If a fault occurs with the inductor as the major fault impedance it may cause excessive TRVs for circuit breakers

3.2.2 May cause undesirable tuning

3.2.3 losses / loss evaluation – initial cost

3.3 where in the circuit to locate the fixed inductors
3.3.1 bus side of breaker
3.3.2 load (capacitor side of breaker)
3.3.3 neutral end of capacitor bank
3.3.4 distributed throughout the bank (one inductor for each capacitor unit)
3.4 How to size the fixed inductor
3.4.1 switchgear limits (limiting outrush within switchgear limitations) RWAs postulation
3.4.2 CT secondary/control system limitations
3.4.3 other limitations

3.5 TRV delay capacitors for the TLI
3.5.1 location
3.5.1.1 line to ground
3.5.1.2 across TLI
3.5.2 sizing
3.5.2.1 Voltage rating
3.5.2.2 Capacitance

Surge Arrester Location