Working Group PC37.302 - "Guide for Fault Current Limiter Testing"
Sponsored by IEEE Switchgear ADSCOM

Las Vegas, NV
September 28th, 2010
Minutes

Mischa Steurer called the meeting of the Working Group to order at 8:00 AM EDT with 24 members and guests present.

1. Introductions of the attendees were made.

2. The IEEE required slides on Patents for Working Groups were discussed. Members were advised to abide by these requirements.

3. The agenda was approved.

4. The minutes of our April 27, 2010 meeting and August 18, 2010 web conference were approved with changes.

5. A SharePoint website is being used for our Working Group. Contact "Roger Leete" roger.leete@bishopgroup.net to request user name / password.

   You can access the website at http://www.bishopgroup.net/links.htm
   Click on "view" next to Advanced Electrical Power Systems
   Click "OK" on pop-up (Digital Certificate)
   Enter user name and password
   Navigate to "FCL Testing Task Force"
   Documents under "Shared Documents" can be checked out for editing.
   New documents can be uploaded but must be checked in for others to view

6. Chairman's Report:
   - The PAR for the "Guide for FCL Testing" was approved by NESCOM on June 17, 2010 and the Task Force has become a Working Group.
   - The WG approved a Panel Session on FCLs for IEEE – PES General Meeting, July 24-29, 2011. The session will be organized by Mischa Steurer and Ram Adapa. Final details will be discussed at a web conference in December 2010.

7. The following items / assignments were discussed:
   - Definition of FCL (for the purpose of this Guide) - Fault current limiter is defined as a device which offers rapid increase in resistive and/or reactive impedance to limit the prospective peak and RMS fault current in an alternating current power systems to the desired value. The change in the resistive and/or reactive impedance is due to the change in electrical conductivity or the magnetic permeability of the device or a combination of both.
   - **Action Item:** Request all manufacturers / laboratories to submit a waveform for their technology to describe the fault current for the worst case condition for fault inception in order to review definitions in Figure 6 below taken from CIGRE Technical Brochure 339.

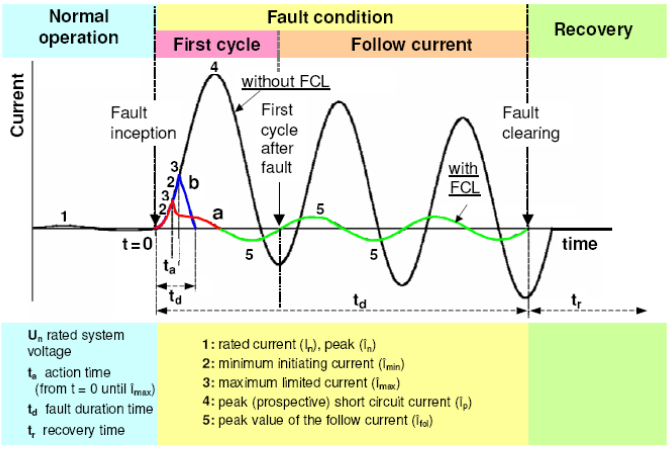

Figure 6 Typical fault current wave shape and characteristic data:
***a**: FCL without fault current interruption; **b**: FCL with fault current interruption*

- Paul Leufkens made a presentation on impulse test requirements for FCLs considering present standards on reactor / transformer (iron core) requirements. **Action Item:** Paul will work with Francisco DeLaRosa and revise the presentation to include actual laboratory experiences for the next meeting.
- Tim Chiocchio and Simon Bird made a presentation on surge testing requirements for power electronic equipment. Surge testing is designed to expose the device to drastic changes in current and voltage simultaneously. Low voltage testing standards include both powered and unpowered testing requirements and assume the internal arresters are in place. Terminal connections are important. External arresters should be removed for testing. Work is needed on how to scale up the requirements to medium and high voltage. **Action Items:** Pat DiLillo will help to add information on high voltage switched series capacitors (FACTS) with power electronic switching. Bill Hassenzahl will provide a list of applicable IEC TC 90 standards. A review of series reactor test requirements will be made by Jim van de Ligt and an update will be provided for the next meeting. Simon Bird will investigate the impact of a surge current through the Solid State FCL on the various components to provide a better understanding of the test requirements. Mischa Steurer will request the resistive superconductor FCL manufacturers to perform surge current through the device analysis.
- Mischa Steurer provided a review of the proposed C37.302 document outline. The document should include the following sections. The coordinators for each section are shown in parentheses.

  Section 4 – FCL Technologies (Ram Adapa)
  Section 5 – Specifications (Francisco DeLaRosa)
  Section 6 – Design (Type) Tests (Tim Chiocchio)
  6.1 BIL (Example)
  6.1.1 Test Setup
  6.1.2 Test Procedure
  6.1.3 Test Criteria
  6.X Exceptions (FCL Technology Specific Tests)
  Section 7 – Production (Routine) Tests (TBD)
  7.1 Common
  7.X Exceptions (FCL Technology Specific Tests)
  Section 8 – Field Tests (TBD)

  Action Item: Jim van de Ligt will review C37.09 and C37.100.1 and make recommendations to revise the structure.

- Both entries for resistive type superconducting FCLs will be combined in the matrix as the type of shunt impedance doesn't affect the testing requirements (Christian Schacherer and Robert Dommerque) – pending.
- Robert Dommerque will review literature to recommend lightning voltage waveshapes for liquid N_2 based insulation systems – pending.
- Tom Tobin will investigate control circuit test requirements in C37.11,), relevant relaying committee documents about surge testing for control circuitry, and fuse standards IEEE 37.41 regarding "rated minimum breaking current" (test duty 3) – pending.

8. Next meetings
    - A web meeting will be scheduled to review panel session details in December 2010.
    - Confirmed: at the Spring IEEE Switchgear Committee meetings (May 16-19, 2011) in Orlando, Florida (USA). The CIGRE WG A3.23 will meet on May 19th and 20th.
    - A Panel Session / WG meeting on FCLs for IEEE – PES General Meeting, July 24-29, 2011 was discussed. We will investigate the scheduling deadline.

The meeting was adjourned at 5:30 PM EDT.

Submitted by:
Frank Lambert

Approved by:
Mischa Steurer