RWA Proposed Performance standards for Capacitor switching transient reduction schemes.

Background

Generally trouble from capacitance current switching arises from connecting (or reconnecting) the capacitor to the circuit.

Connecting refers to the initial closure of the circuit breaker (switching device) to energize the capacitive load.

Reconnecting refers to reignitions or restrikes after having broken (for a short time) the capacitive circuit. Obviously, a switching device which continues after many attempts to "reconnect" the capacitive load has failed to open the circuit.

Two major phenomena are of interest: **Overvoltages**, and R**esonance Excitation**

1) The response of a largely inductive system to the capacitor connection (or reconnection) generates transient voltages and currents. This is most problematic when the system is underdamped as it usually is. An oscillation results which may produce overvoltages.

2) The quick voltage drop at the bus where the capacitor is connected sends traveling waves throught a power system. When no intentional inductance is used, a typical voltage step occurs in about 1μs (depends on source capacitance). When very large Transient Limiting inductors are used as in a harmonic filter, the voltage step is an order of magnitude slower, more like 10μs.
The step wave propagates on all lines connected to the bus and can excite natural frequencies, both local and remote. These can cause problems for some sensitive electronic equipment. Usually if extra zero crossings are produced by the voltage transient, the impact on power electronics is worse.

The seriousness of a connection or reconnection of a capacitive load can be defined in terms of the magnitude of the voltage collapse $V_{collapse}$ across the circuit breaker, the speed of the system voltage collapse; and the magnitude and speed (di/dt) of the inrush/outrush current which flows associated with the voltage collapse.

On closing, two approaches have been used to limit $V_{collapse}$

1) multi-step switching with a pre-insertion impedance

2) controlled point on wave closing

1) Multi-step closing energizes a capacitive load in two or more steps. The principle is to connect the capacitive load through an impedance to "pre-charge" the capacitance and then later shunt out the impedance, connecting the capacitive load directly. The most familiar and commonly used is the closing resistor on EHV circuit breakers. The size and duration of insertion of the impedance is carefully chosen to balance minimization of system disturbance on insertion of the impedance, and to minimize $V_{collapse}$ when shunting the impedance.

2) controlled point on wave closing attempts to energize the capacitive load when the instantaneous voltage across the breaker is close to zero. $V_{collapse}$ will be this instantaneous voltage.

{ combinations have been employed where a large pre-insertion resistance is used, and shunted when the instantaneous voltage across the resistance is zero. }

On opening the situation is somewhat different.

Multi-step opening can and has been used to drain the trapped charge on the capacitive load back into the source thus reducing the need for a large V_{CCR} .

More common is the design of an interrupter which rarely restrikes and either doesn't reignite , or reignites with a low $V_{collapse}$ and doesn’t reignite later .

Timed opening can be used to aid in this objective.

Rated Capacitance current switching Class

There are 5 classes of capacitance current switching

Class	Description	Opening performance	closing performance
C0		1 restrike per operation	1.0 uncontrolled
C1	"normal" circuit breaker Corresponds to C37.09 –1979 "Definite Purpose"	Voltage collapse < 1.0 p.u. 98% of time. (Probability of restrike < 1/50 operations)	1.0 < 1us {uncontrolled}
C2	Very low probability of restrike	Voltage collapse < 1.0 p.u. 99.8% of time. (Probability of restrike < 1/500 operations)	1.0 < 1us {uncontrolled}
C3.2	Capacitor "soft" switching High power quality Circuit Breaker	Voltage collapse < 0.37 p.u. 99.8% of operations. (probability of reignition after 50 degrees < 1/500 operations)	voltage collapse < .37 p.u. 98% of operations
C3.1	Capacitor "soft" switching High power quality Circuit Breaker (Just a little less precice than C3.2)	Voltage collapse < 0.37 p.u. 98% of operations. (probability of reignition after 50 degrees < 1/50 operations.	voltage collapse < .37 p.u. 95% of operations

Class C3.1 could be a class C1 switching device with controlled closing, and C3.2 would be a Class C2 switching device with controlled closing.

Justification for a $V_{collapse}$ of 0.37

A $V_{collapse}$ of .37 on closing corresponds to 1.0 ms from a true zero crossing which is a reasonably attained target for synchronous closing. In many cases a V collapse of 0.37 or less will not produce extra zero crossings. A $V_{collapse}$ of 0.37 will usually result in an overvoltage of <1.3 p.u. on closing and less on opening. [there are about 3 ms of damping time for closing and 5 ms on opening]

There can be a lot of discussion on the statistical performance.
It may be prudent to develop a multi level performance criterion.

For example, My experience with 69kV vacuum switches is about 99% of operations are within 1.0 ms of zero crossing ($V_{collapse}$ of 0.37) 90 % of operations are within 0.5 ms of zero crossing ($V_{collapse}$ = 0.19) about 0.5% of operations are "off the wall" i.e. $V_{collapse}$ = 0.8 to 1.0.

I haven't collected statistics on our synchronously switched circuit breakers, but I believe somewhat wider tolerances would be required.

For capacitor switching, the minimum theoretical transient current is 2.0 p.u. of the steady state current. So for a single bank with a natural frequency of 600 Hz a $V_{collapse}$ of 0.2 will produce the theoretical minimum transient so accuracies smaller than 0.5 ms from a zero crossing produce almost no additional improvement in transient reduction.

For a back to back case where the natural frequency is 3000 Hz, a transient improvement is attained all the way down to a $V_{collapse}$ of 0.04 , or a timing accuracy of 100 µs from a true zero crossing!

For schemes using a "pre-insertion" impedance the impedance must be selected for the application, and ultimately the impedance will be bypassed. Neither the insertion $\mathbf{V_{collapse}}$ or the bypassing $\mathbf{V_{collapse}}$ should exceed the standard values. A very gradual slope of the dv/dt could allow a larger $\mathbf{V_{collapse}}$ on insertion . Probability of incorrect insertion or bypassing needs to be considered.

Capacitance Current Rating Structure

The capacitive switching current ratings (line charging, cable charging, and shunt capacitor bank) has three associated ratings and a class of rating:

1. Rated peak capacitive inrush current, which determines the circuit breaker's suitability for switching back-to-back applications;
2. Rated shunt capacitor bank switching endurance, which determines the circuit breaker's suitability for long-term repetitive switching of capacitors.
3. Rated peak capacitive recovery voltage, which determines the circuit breaker's capability to switch ungrounded capacitor banks.

Class of shunt capacitor bank switching current rating: Class C1, C2, and C3; as defined by differences in the specified test procedure in Clause C37.09a – 4.10 Shunt Capacitor Switching Tests; Class C3, being most severe with respect to reignitions and closing, Class C2 being somewhat less severe, requiring a very low restrike probability, and Class C1 having a low probability of restriking.

5.11.5 Rated Shunt Capacitor Bank Switching Current I_C

The rated shunt capacitor bank switching current is the maximum rms symmetrical power-frequency capacitor bank current that the circuit breaker shall be required to make and interrupt at its rated maximum voltage (within its rated differential capacitance voltage). Filter bank switching requires special consideration and is not currently covered by this document

Notes:

Grounded systems have lower transient recovery voltage requirements. Circuit breakers with a V_{CRR}/Vrated <3.1 may not be used in non-grounded systems at their rated voltage.

The harmonic content of the rated switching current shall be <10% and should cause no extraneous current zeros.

5.11.6 Rated Peak Capacitive Inrush Current I_{CP}

The rated peak capacitive inrush current is the maximum instantaneous value of transient inrush current that the circuit breaker shall be required to make when energizing either single or parallel capacitor banks. (See figures **Error! Bookmark not defined.** & **Error! Bookmark not defined.**, Clause 8)

Note: Expected maximum ratios of (rated peak capacitive inrush current) / (rated capacitive switching current) are in the range of 200 for back-to-back capacitors. For single capacitors the ratio is normally less than 20.

Generally: for single banks (or cables) $I_{CP} < 20 \times I_C$
for back to back banks (or cables) $I_{CP} > 20 \times I_C$ and may be $>200 \times I_C$

I_{CP} has a mimimum frequency requirement of 4250Hz and no upper limit.

5.11.7 Rated Peak Capacitive Recovery Voltage V_{CCR}

The rated peak capacitive recovery voltage is the maximum instantaneous value of recovery voltage (power frequency +dc offset) which the circuit breaker shall be required to withstand, when interrupting any value of capacitance current below or equal to its rated capacitance current ratings .

V_{CCR} will determine whether a circuit breaker is suited for grounded or ungrounded operation, large pole disparities, clearing charging of healthy phases on faulted ungrounded lines, etc.

5.11.8 Shunt Capacitor Switching Endurance

The shunt capacitor switching endurance is the number of shunt capacitor switching operations that the circuit breaker shall be capable of successfully performing, without requiring internal maintenance.

Rated outrush current crest and di/dt combination **[need this rating for all circuit breakers]**
I suggest that this be a related capability and be equal to the rated close and latch current crest, and that there be no limits on di/dt.