Overview of CMOS Device Behavior and Modeling for Mixed-Signal/RF Circuit Design

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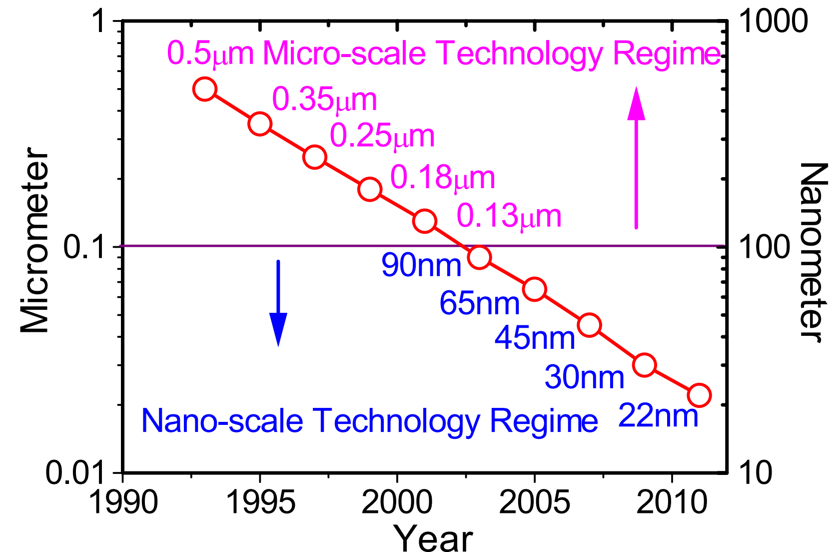
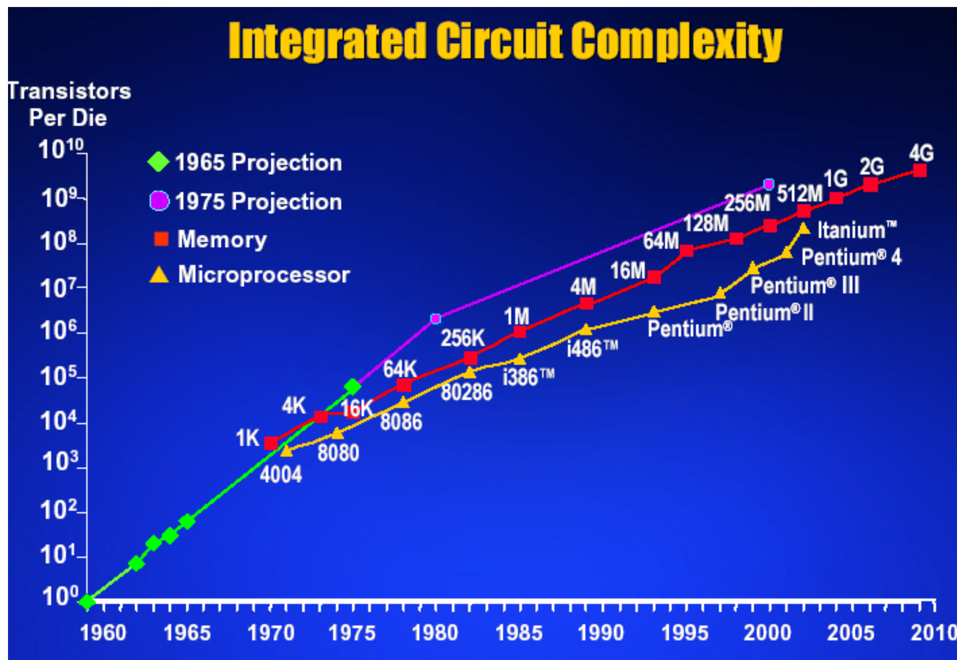
Outline

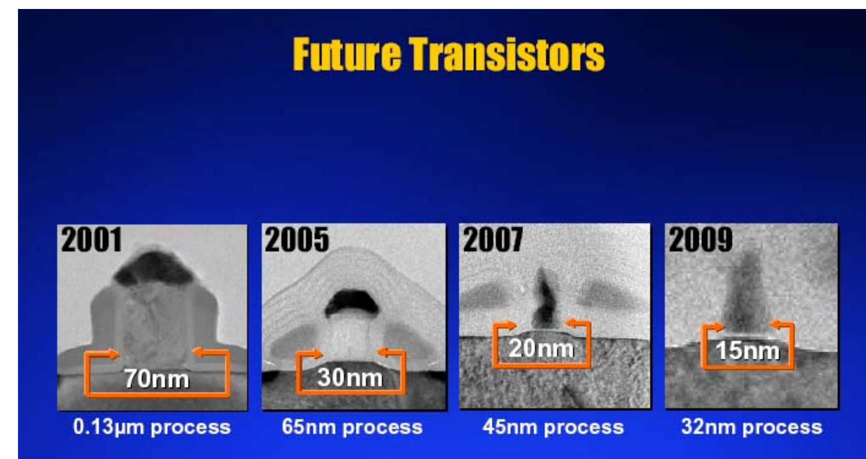
- CMOS Technology Trends
- Device Behavior Overview
- Device Modeling Challenges
- Figures of Merit and Model Validation
- Summary

CMOS Technology Trends -- Nano-scale

- CMOS has been in nanoscale era.
- Silicon CMOS is still the mainstream IC technology in the next 7-10 years before other nano devices play roles.







Source: Intel

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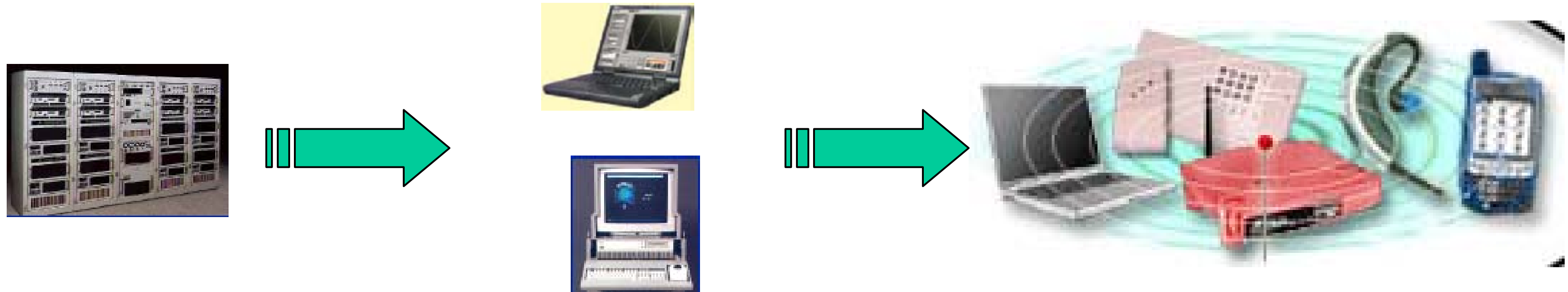
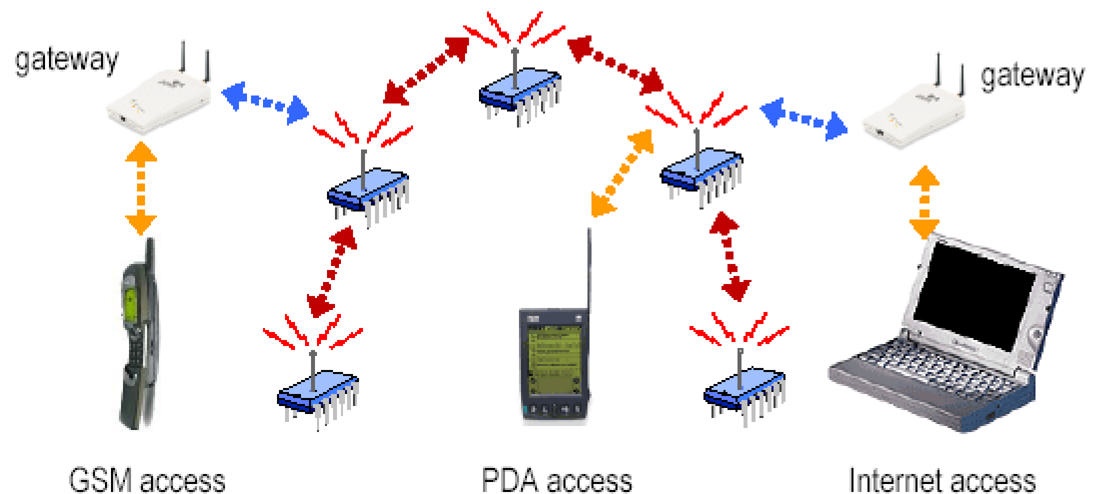
Semiconductor Industry (SI) Trend

PC -> Communication (wireless)



- The data of voice, video and other information will be exchanged through any media at any time and any places

  by wireless devices!



Intel Inside Communication Everywhere

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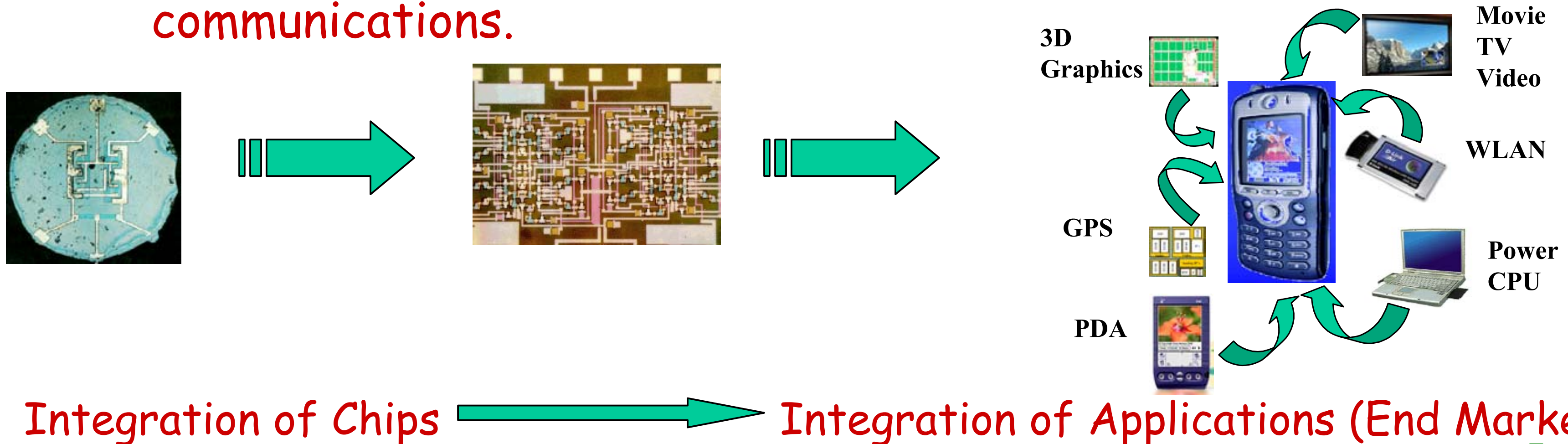
SI Trend (CONT.)

IC -> Application Integration

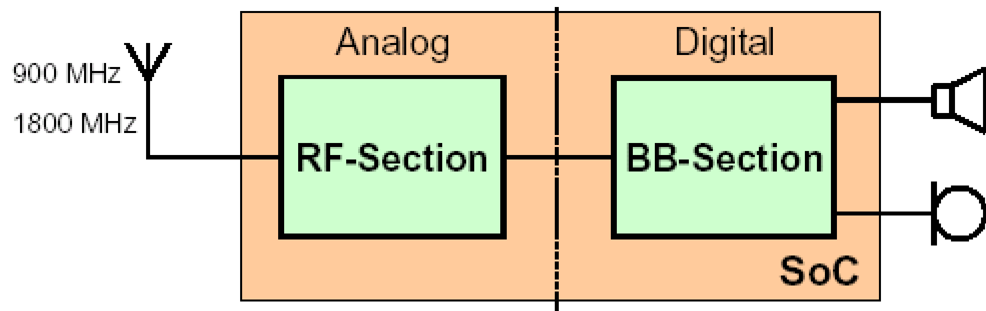
- The revenue ratio of the system chip to overall semiconductor industry will increase to 21.9% (with a total revenue of 65.6 billions) in 2008 from 16.6% in 2002
- Product integration is to integrate different products such smart phone, camera, cell phone, PDA, TV, music player, based on one platform such as cell phone.
- The integration of end market will be the merge of markets such as computer, consumer, wired and wireless communications.



Integration of Chips → Integration of Applications (End Market)

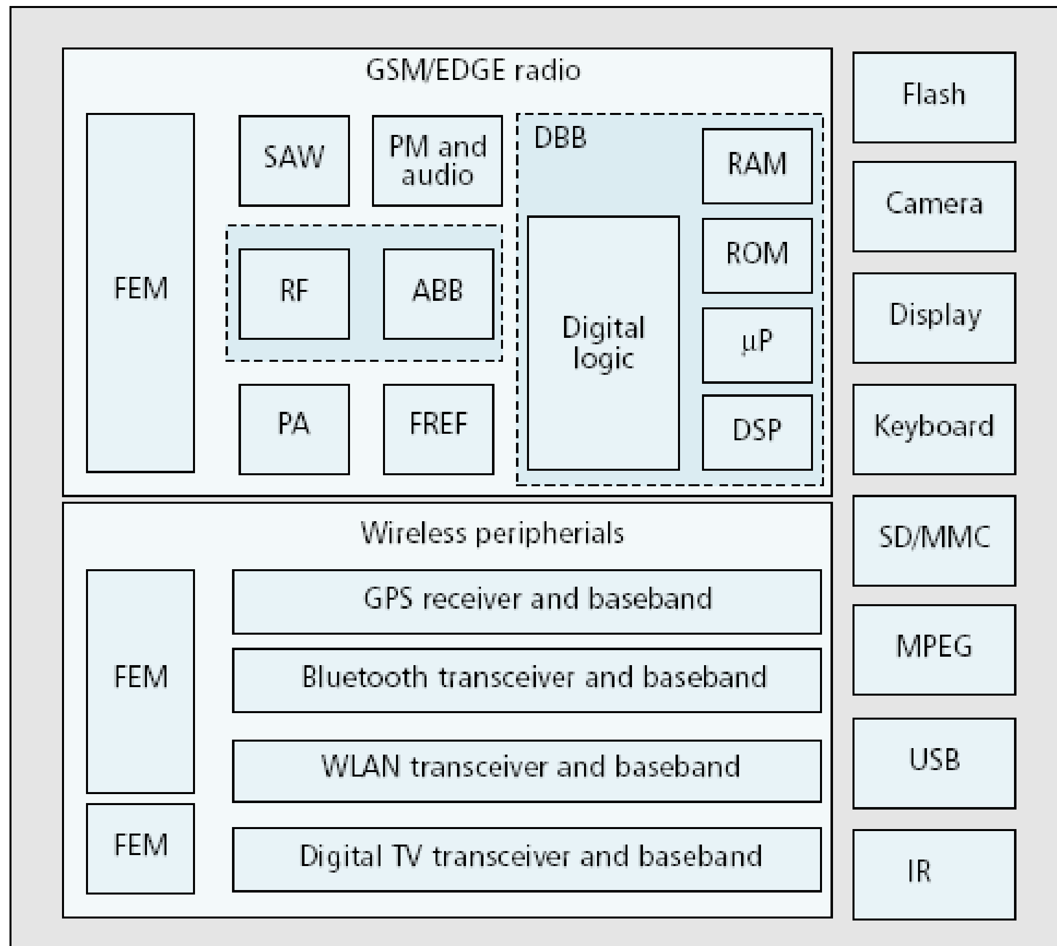
CMOS Technology Trends -- RF CMOS

- Recent speed improvements and better noise behavior of CMOS transistors have made it feasible to implement RF circuits for wireless products, such as cell phones, Global Positioning System, and Bluetooth.
- CMOS is one of the best suitable technologies to ingrate RF circuits with analog and base-band digital circuits.
- Tremendous research effort is dedicated to RF CMOS, driven by System-on-Chip (SoC).



CMOS:
High integration density
High yield
Low power consumption
Low cost

An Illustration of RF SoC on CMOS



- RF SoC - Integrate a chipset system onto a same chip:
  - RF Front End (RFFE)
  - Analog Based-band (ABB)
  - Power Management and Audio Codecs (PMAC)
  - Digital Base-band (DBB)
- RFCMOS implementation challenges:
  - low cost
  - high performance

K. Muhammad et al. "Digital RF Processing: Toward Low-Cost Reconfigurable Radios," IEEE Communication Magazine, Vol. 43, pp. 105-113, 2005.

Design IC in Nano-scale/RF Era

Need to Well Understand the Device Behavior in Advanced Technology Nodes

Need to Develop Physical and Accurate Device Models for RF/Analog Design

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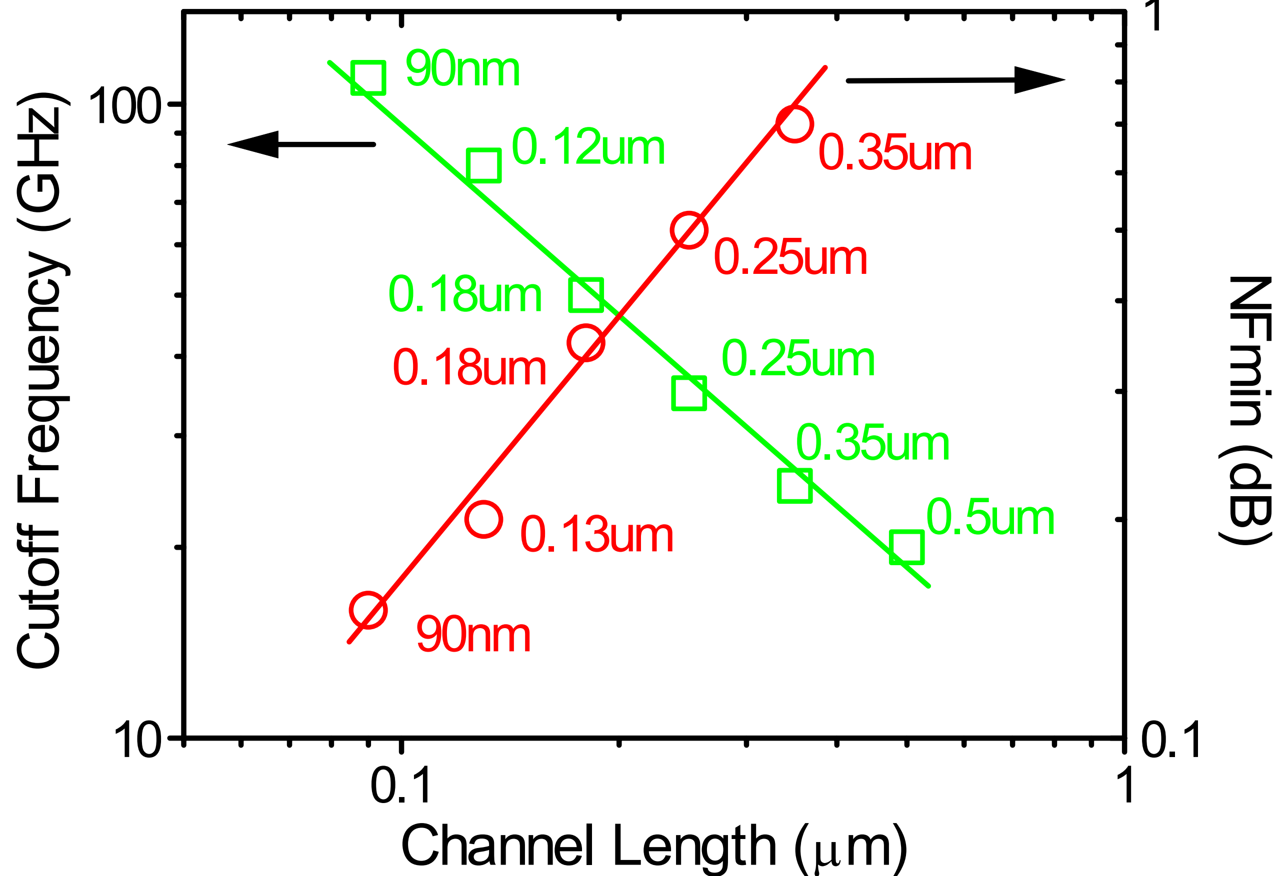
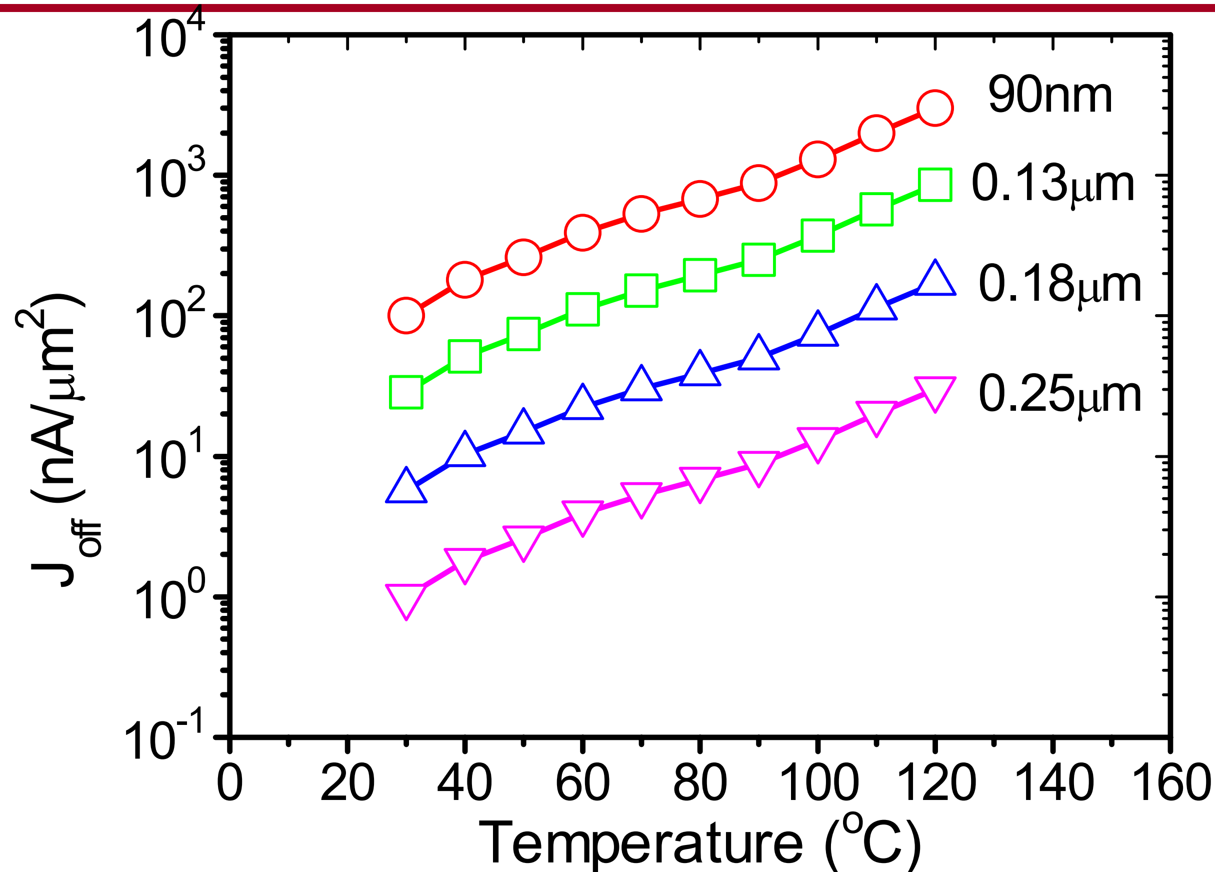
MOSFET High Frequency Behavior



(Yuhua Cheng, "Challenges in Bridging Manufacturing and Design for RF applications-An Overview of Advanced Device Modeling for RF Circuit Design", RFIC/IMS workshop, June 2004)

- Today's MOSFETs show high Ft and low NF

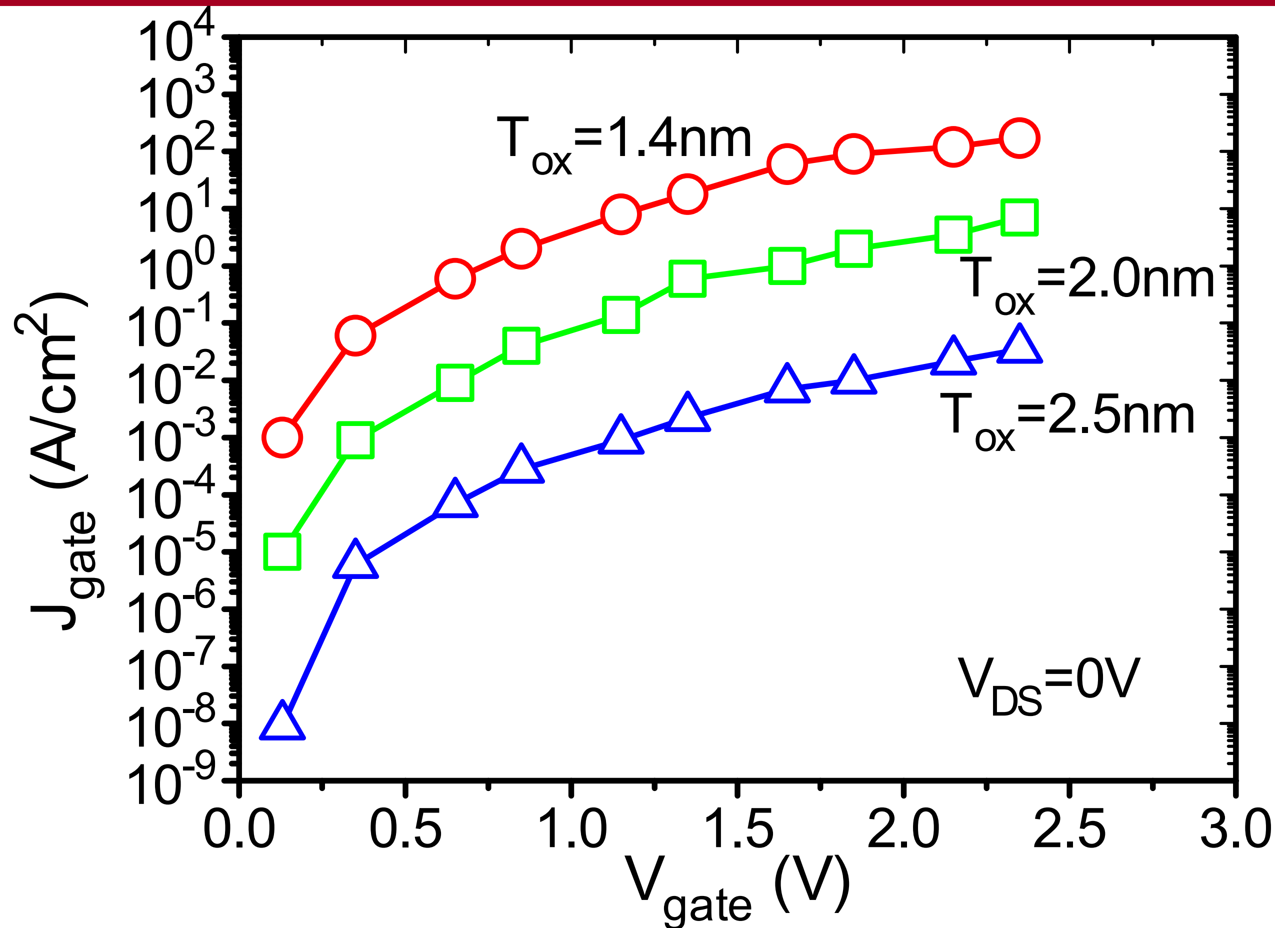
Leakage in Different Technology Node



(Yuhua Cheng, "Challenges in Bridging Manufacturing and Design for RF applications-An Overview of Advanced Device Modeling for RF Circuit Design", RFIC/IMS workshop, June 2004)

- Leakage increases significantly as technology advances.

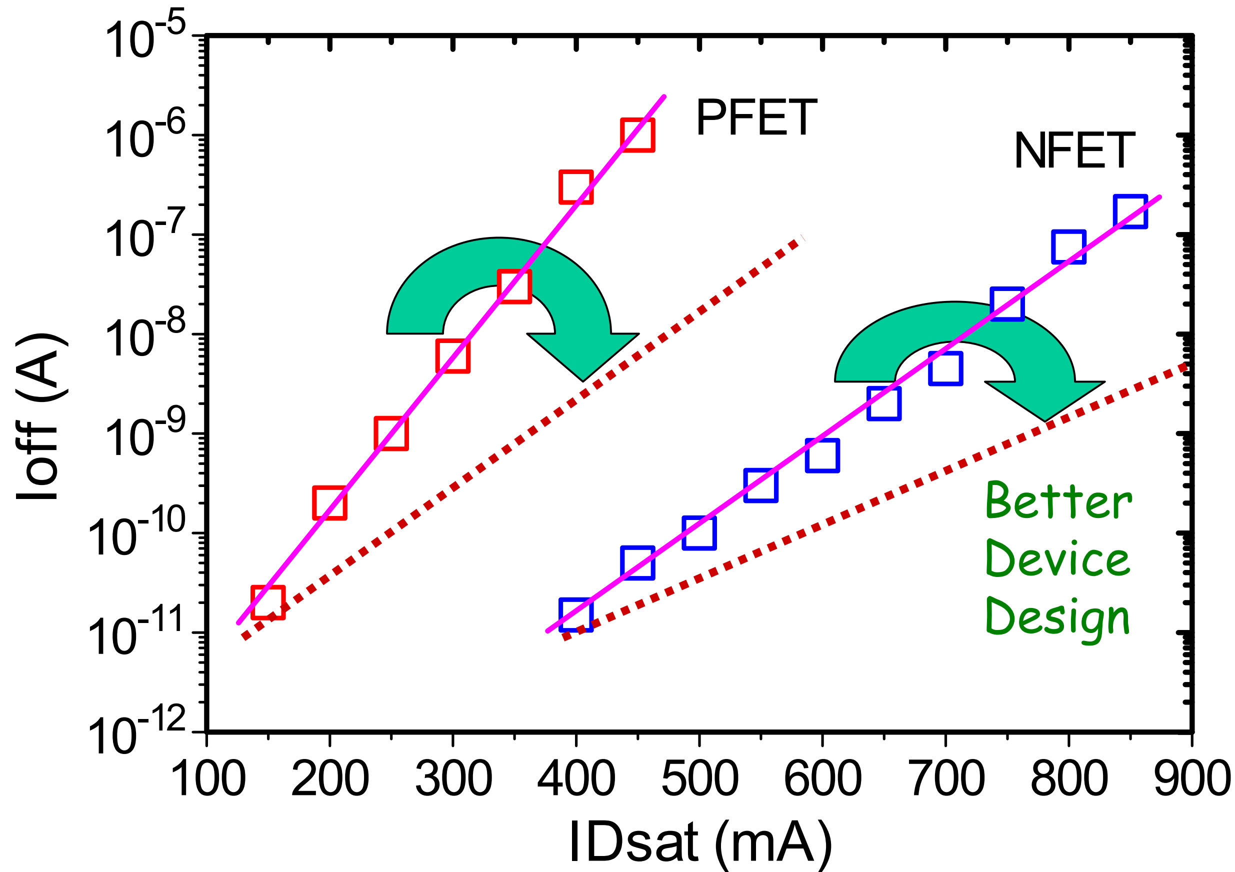
MOSFET Gate Leakage



(Yuhua Cheng, "Challenges in Bridging Manufacturing and Design for RF applications-An Overview of Advanced Device Modeling for RF Circuit Design", RFIC/IMS workshop, June 2004)

- In today's MOSFETs, gate leakage increases by orders for the decrease of Tox

I_{Dsat}/I_{off} Universal Curves



- A trade-off between I_{Dsat} and I_{off}.
- Better device design and material selection to reduce the slope of the universal curves.

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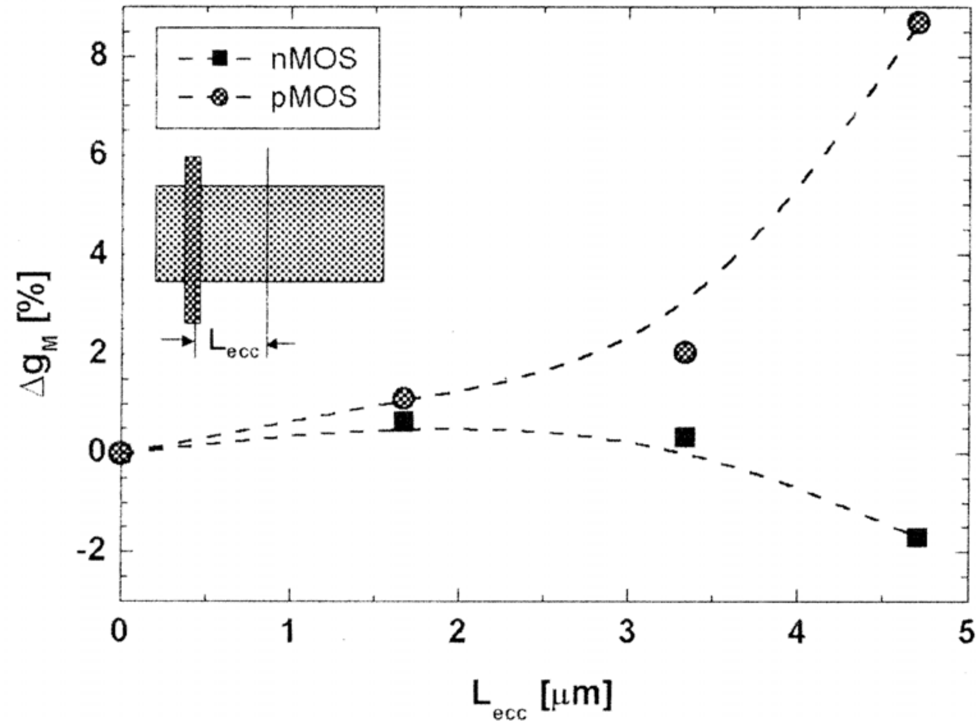
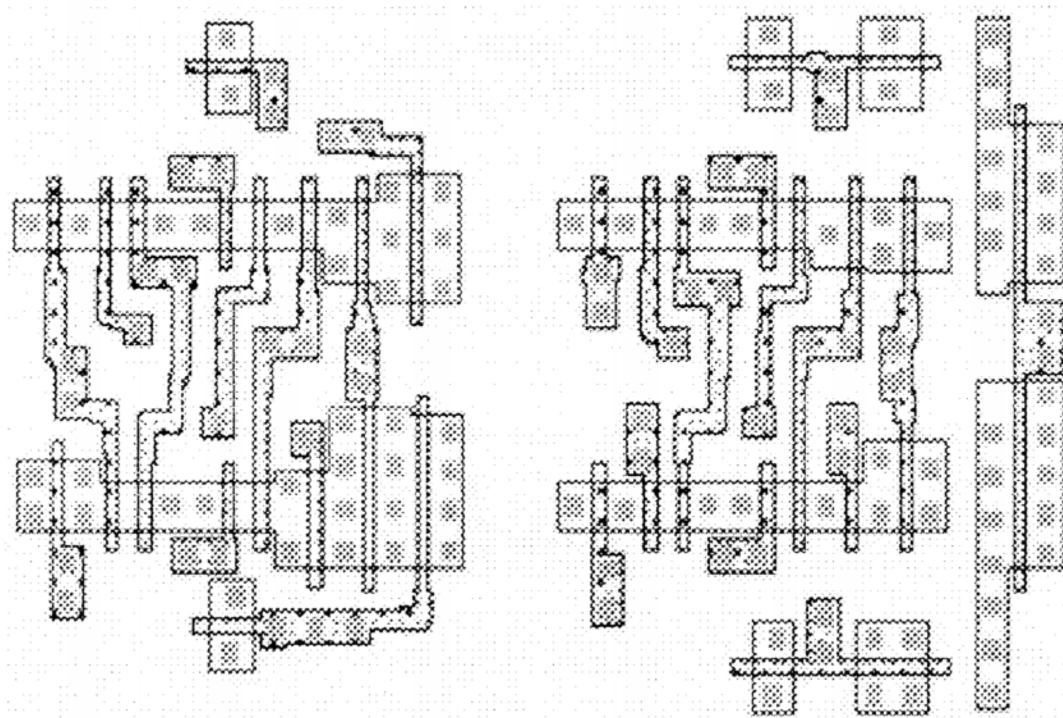
Layout Dependent Device Performance



(C. H. Diaz et al., "Process and circuit design interlock for application-dependent scaling tradeoffs and optimization in the SoC era,", IEEE J. of Solid-State Circuits, Vol. 38 , Pages:444-449, 2003)

- Effects different to nfet and pfet.
- Impact both digital (changing drive current) and analog (changing both Gm and matching).

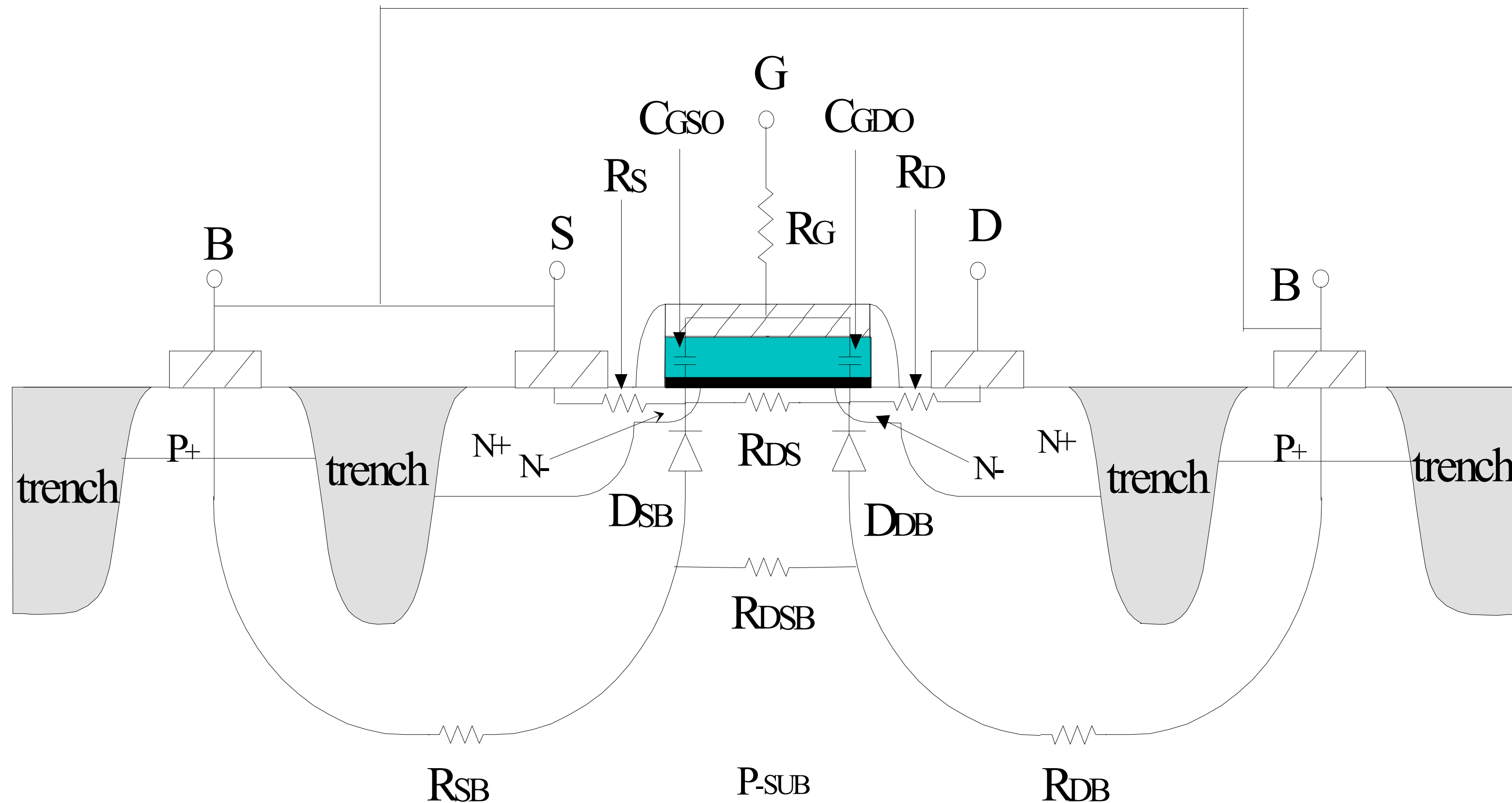
Layout Dependent Device Performance (CONT.)



(C. H. Diaz et al., "Process and circuit design interlock for application-dependent scaling tradeoffs and optimization in the SoC era,", IEEE J. of Solid-State Circuits, Vol. 38 , Pages:444-449, 2003)

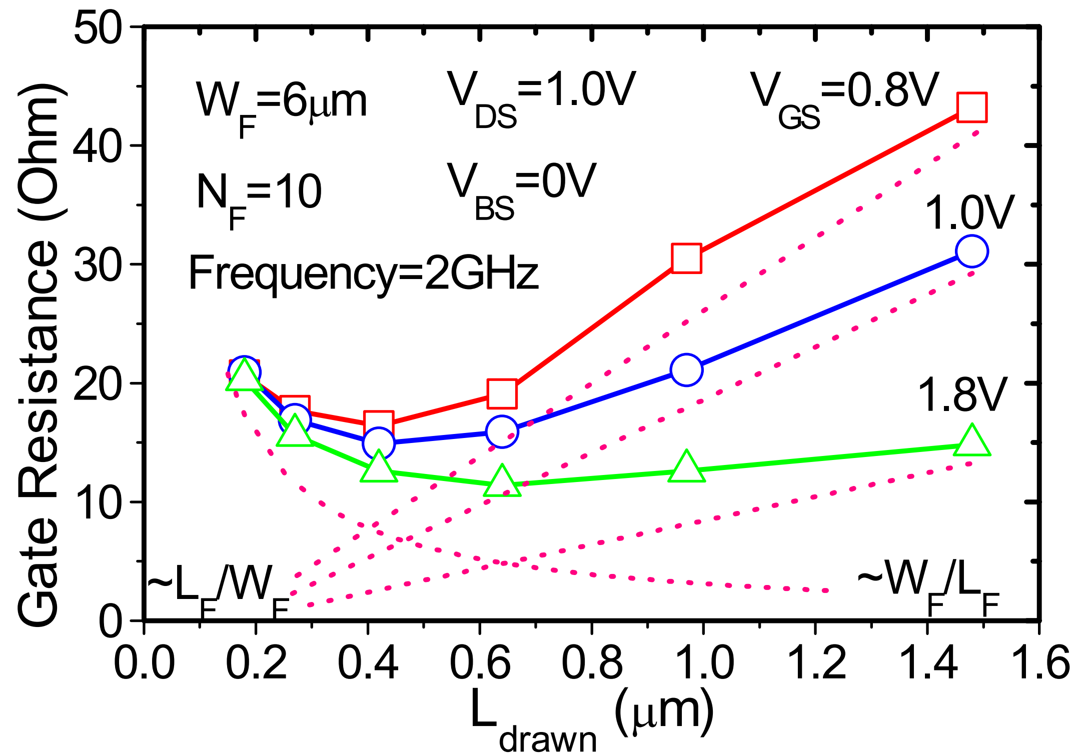
- Irregular device layouts are used in digital (even analog) cell libraries.
- The layouts of the devices in the cell libraries may be different from those for device modeling

HF Behavior - Parasitic Effects



- Parasitic components need to be well understood at HF.

HF Behavior: Effective Rg



(Yuhua Cheng et al., "High frequency characterization of gate resistance in RF MOSFETs", IEEE Electron Device Letters , Vol. 22, pp. 98-100, 2001.)

- Effective R_G extracted by:

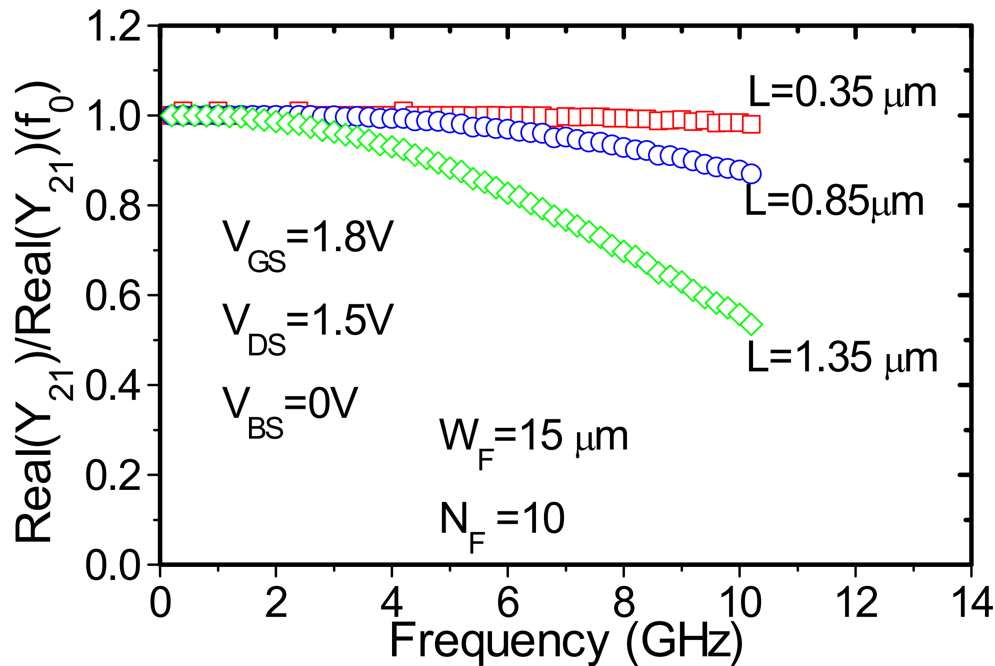
$$R_G = \left| \frac{\mathrm{Re}\{Y_{12}\}}{\mathrm{Im}\{Y_{11}\}\,\mathrm{Im}\{Y_{12}\}} \right|$$

- Effective R_G does not follow equation below when L_f is long:

$$R_{G,poly} = \frac{R_{Gsh}}{N_f L_f}\left(W_{ext} + \frac{W_f}{\alpha}\right)$$

- Significant increase in effective R_G due to non-quasi-static (NQS) effect.

HF Behavior: NQS Effects (1)



(Yuhua Cheng et al., "Frequency-dependent resistive and capacitive components in RF MOSFETs ," IEEE Electron Device Letters , Vol. 22, pp. 333 -335, July 2001.)

- Effective $G_{m,\ normalized}$:

$$G_{m,\ normalized} = \frac{\mathrm{Re}(Y_{21})}{\mathrm{Re}(Y_{21(f0)})}$$

- Short L, G_m is "constant" over f.
- Longer L, G_m becomes frequency dependent;
- The longer the L, the stronger the frequency dependence.

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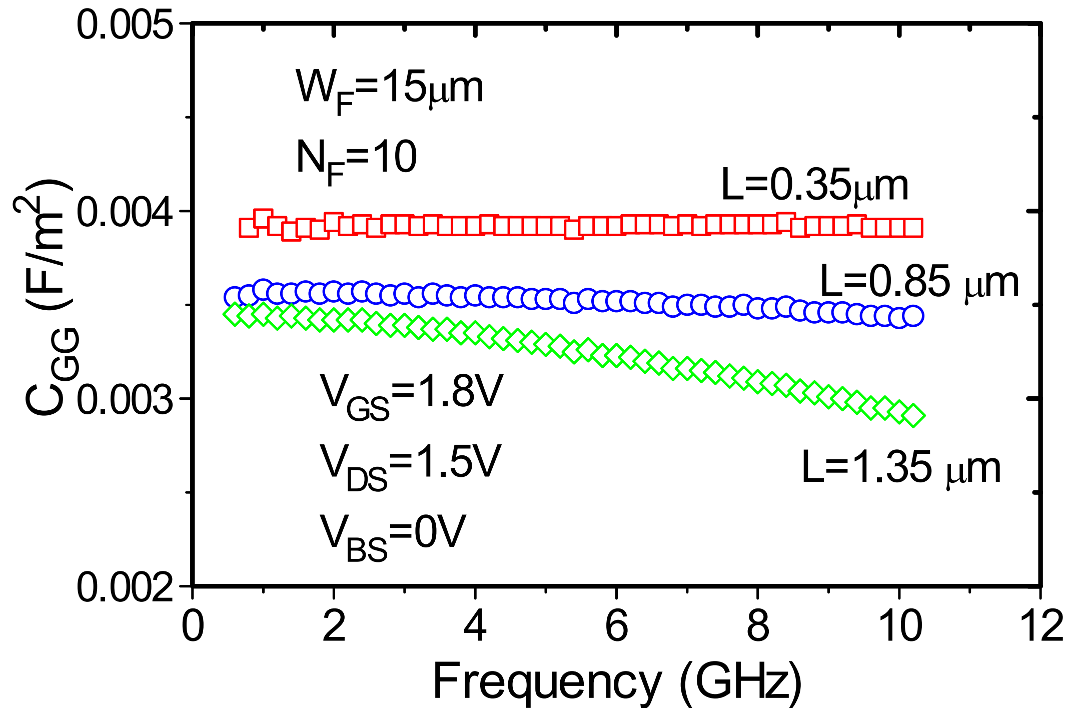
HF Behavior: NQS Effects (2)



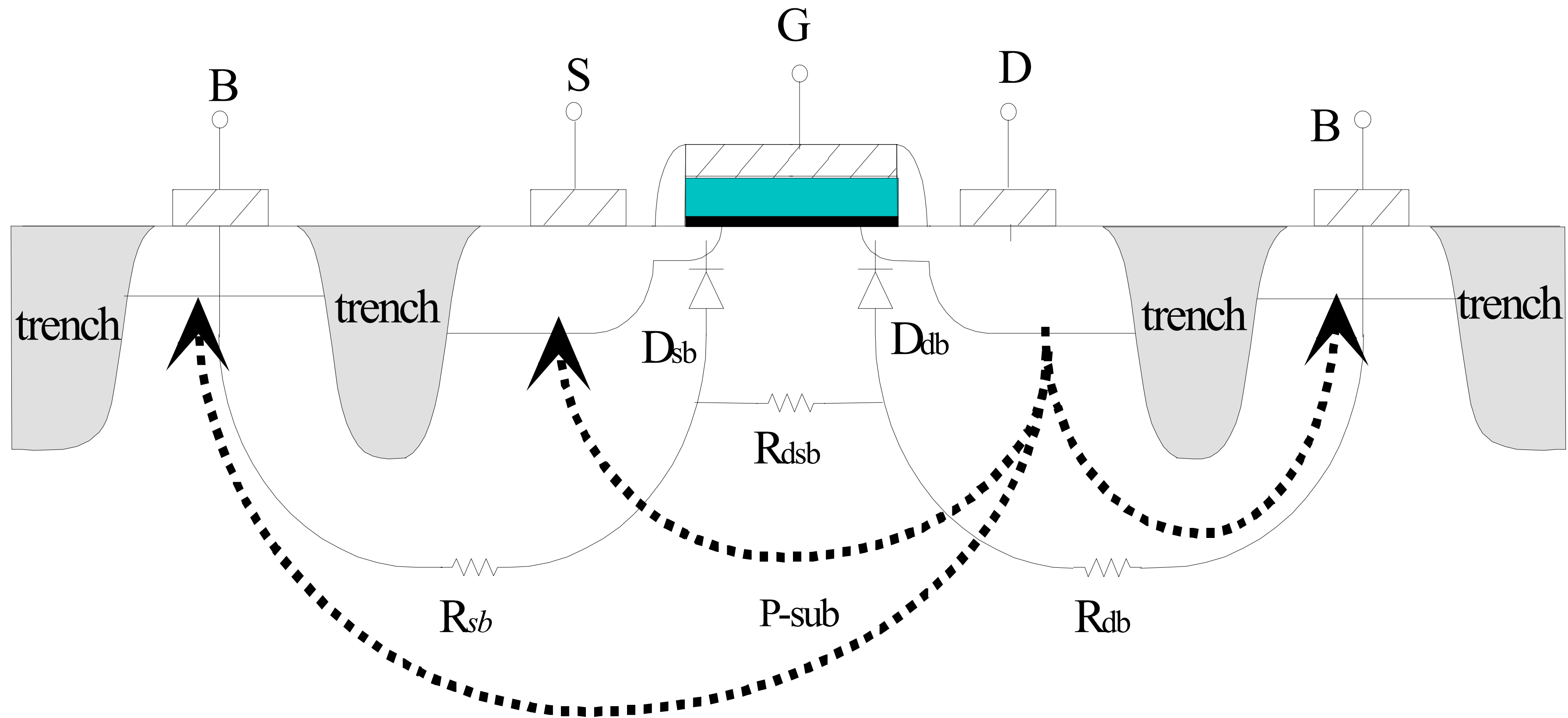
- (Yuhua Cheng et al., "Frequency-dependent resistive and capacitive components in RF MOSFETs ," IEEE Electron Device Letters , Vol. 22, pp. 333 -335, July 2001.)

- Effective Gate Capacitance $C_{gg,eff}$:

$$CGG,eff = \left|\frac{\mathrm{Im}\{Y11\}}{\omega}\right|$$

- Short L, $C_{gg,eff}$ is "constant" over f.
- Longer L, $C_{gg,eff}$ becomes frequency dependent.
- The longer the L, the stronger the frequency dependence.

HF Behavior: Substrate Coupling



- At HF, signal is coupled to substrate through junction capacitance.
- This effect impact mainly the output impedance.

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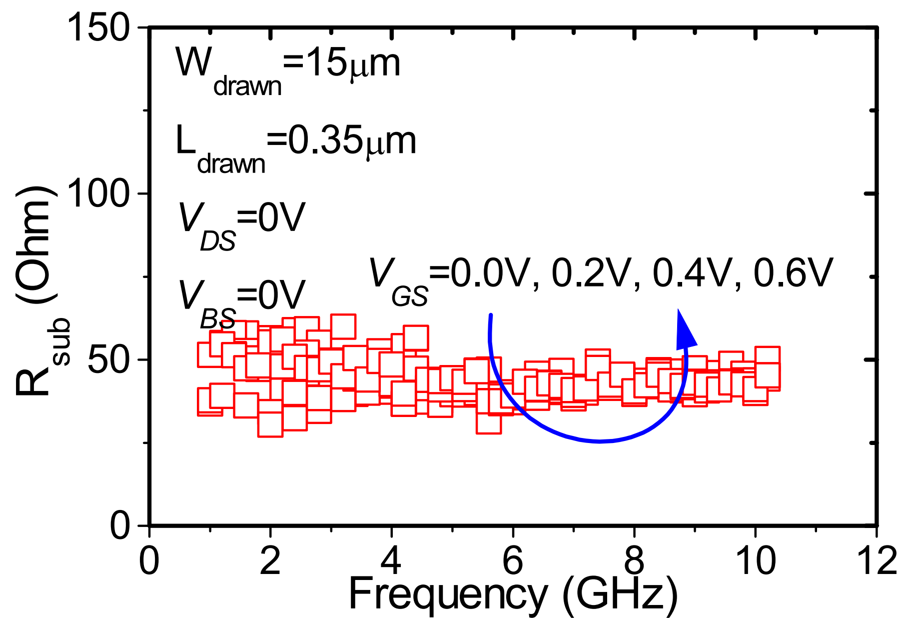
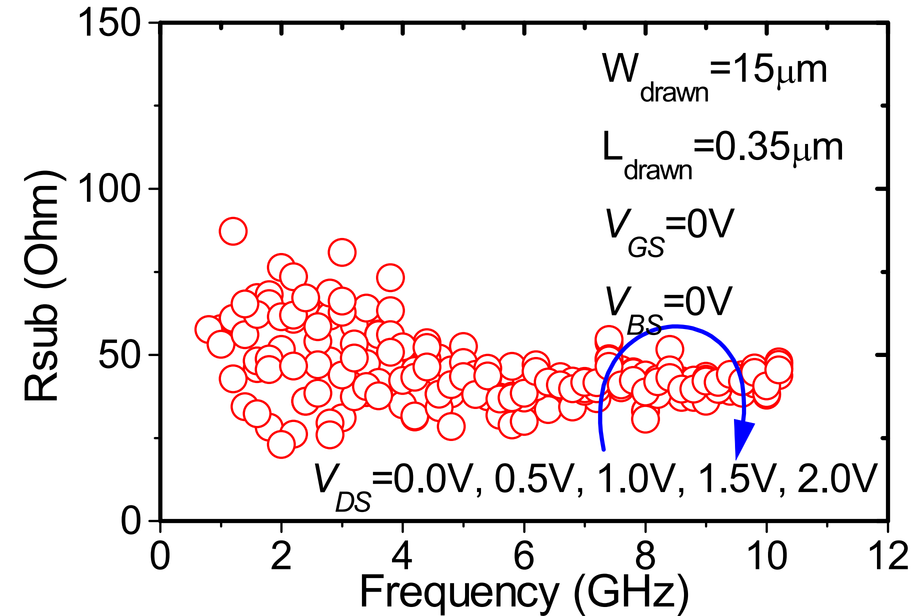
HF Behavior: Bias and f Dependence of R_{sub}

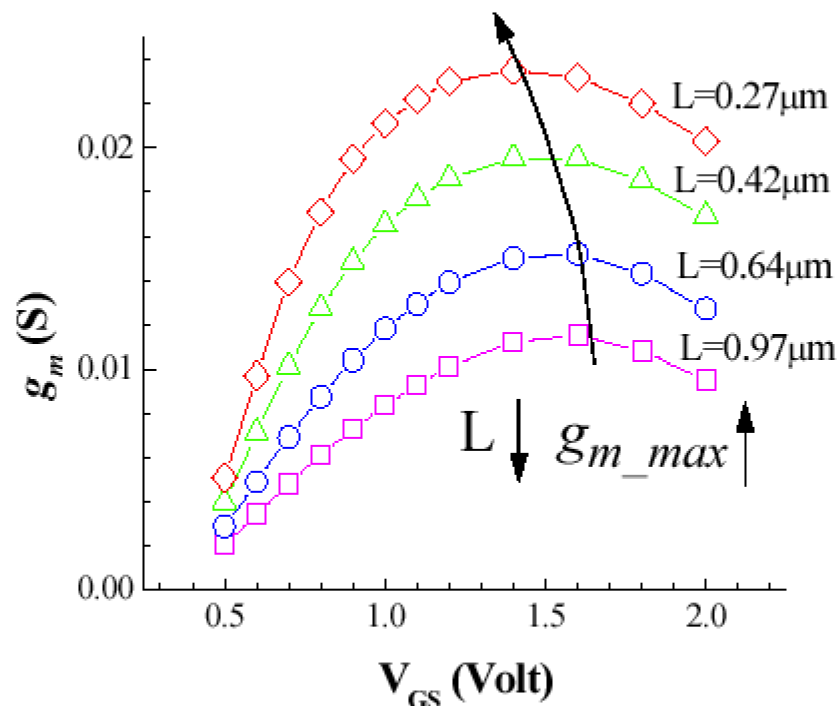


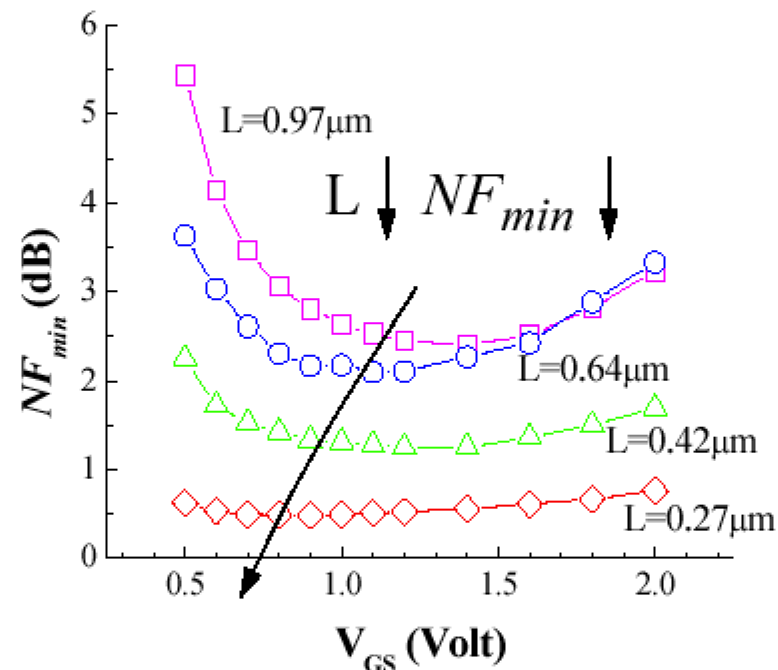


(Yuhua Cheng et al., "On the high-frequency characteristics of substrate resistance in RF MOSFETs " IEEE Electron Device Letters , Vol. 21, Page(s): 604 -606, 2000)

- Substrate resistance is a very weak function of biases at the gate and drain.
- Up to 10GHz, substrate resistance is not sensitive to frequency.

HF Behavior: Thermal Noise





(Jamal Deen, Chih-Hung Chen; Yuhua Cheng; "MOSFET modeling for low noise, RF circuit design" Proceedings of the IEEE 2002 Custom Integrated Circuits Conference, pp. 201 - 208, May 2002.)

- HF noise reduces as the technology advances (and shorter L).
- Higher Gm, lower HF noise.
- Low Nf (<1dB) can be obtained at normal gate biases.

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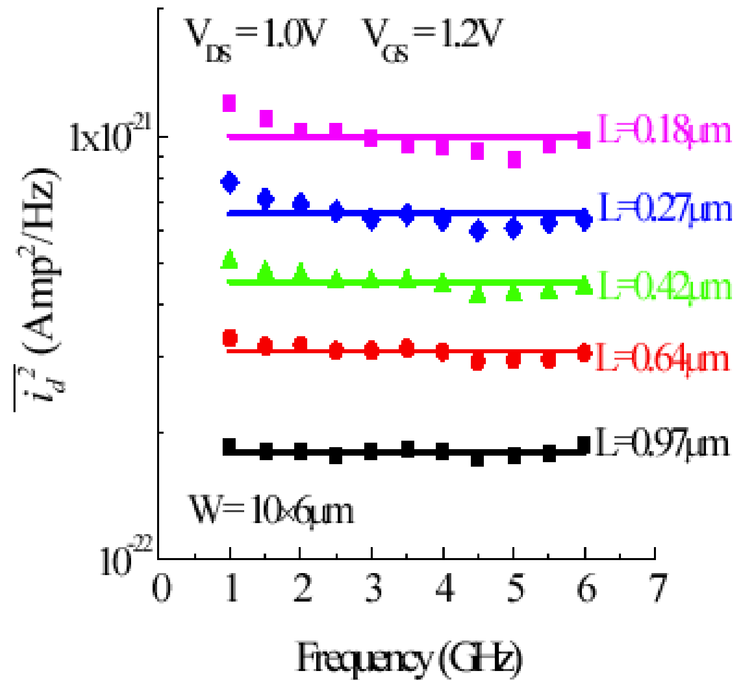
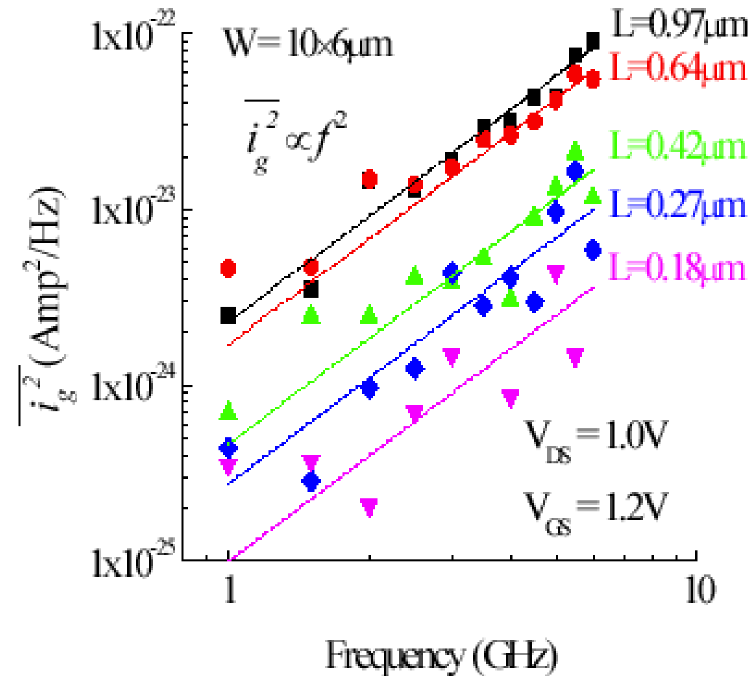
HF Behavior: Induced Gate Noise

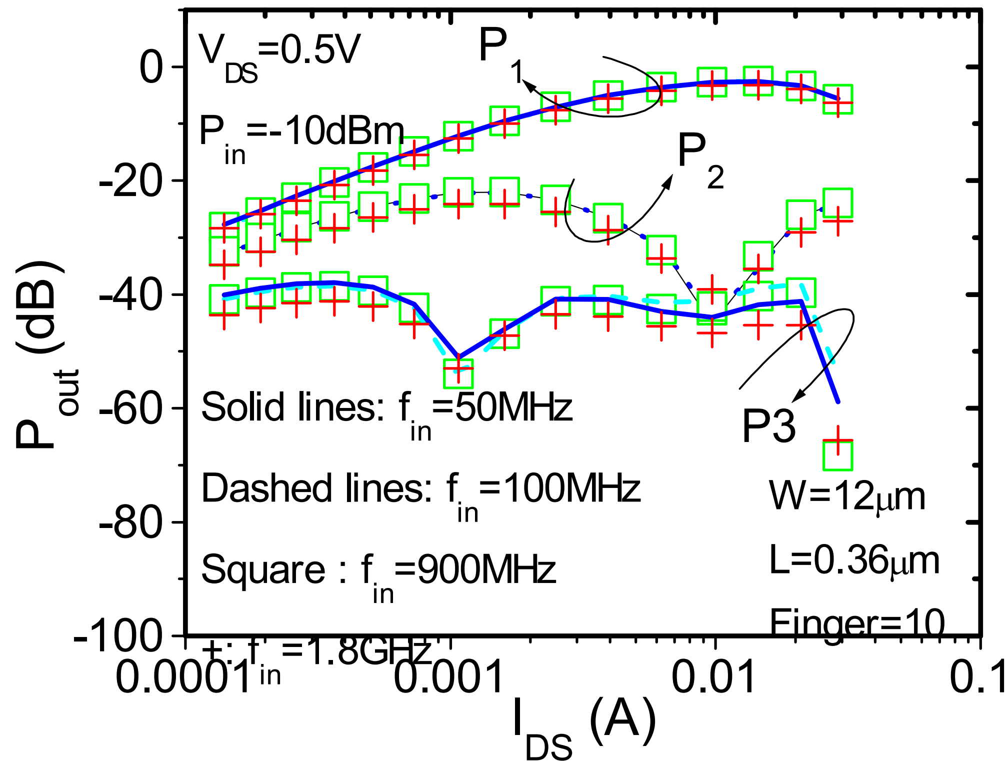




(Jamal Deen, Chih-Hung Chen; Yuhua Cheng; "MOSFET modeling for low noise, RF circuit design" Proceedings of the IEEE 2002 Custom Integrated Circuits Conference, pp. 201 – 208, May 2002.)

- Channel noise is frequency independent and induced gate noise is frequency dependent.
- Induced gate noise is not negligible in devices with long L or devices with short L but at very high frequency.

HF Behavior: High "Low Frequency Limit"



(Tzung-Yin Lee, and Yuhua Cheng, "High-Frequency Characterization and Modeling of Distortion Behavior of MOSFETs for RF IC Design", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 9, pp. 1407 – 1414, 2004.)

- MOSFET has much higher "low frequency limit" (LFL)
- HF distortion characteristics (<f_{LFL}) can be described by its low-frequency behavior

Device Modeling for RF Applications

- Device Modeling at HF should at least include the modeling for:
  - MOSFET
  - Passive devices (R, C, inductor,varactors)
  - Special devices (LDMOS and PNP BJTs)
  - Interconnect
  - Substrate
  - Circuit blocks (behavior modeling)

- Today, we will mainly talk about MOSFET modeling.

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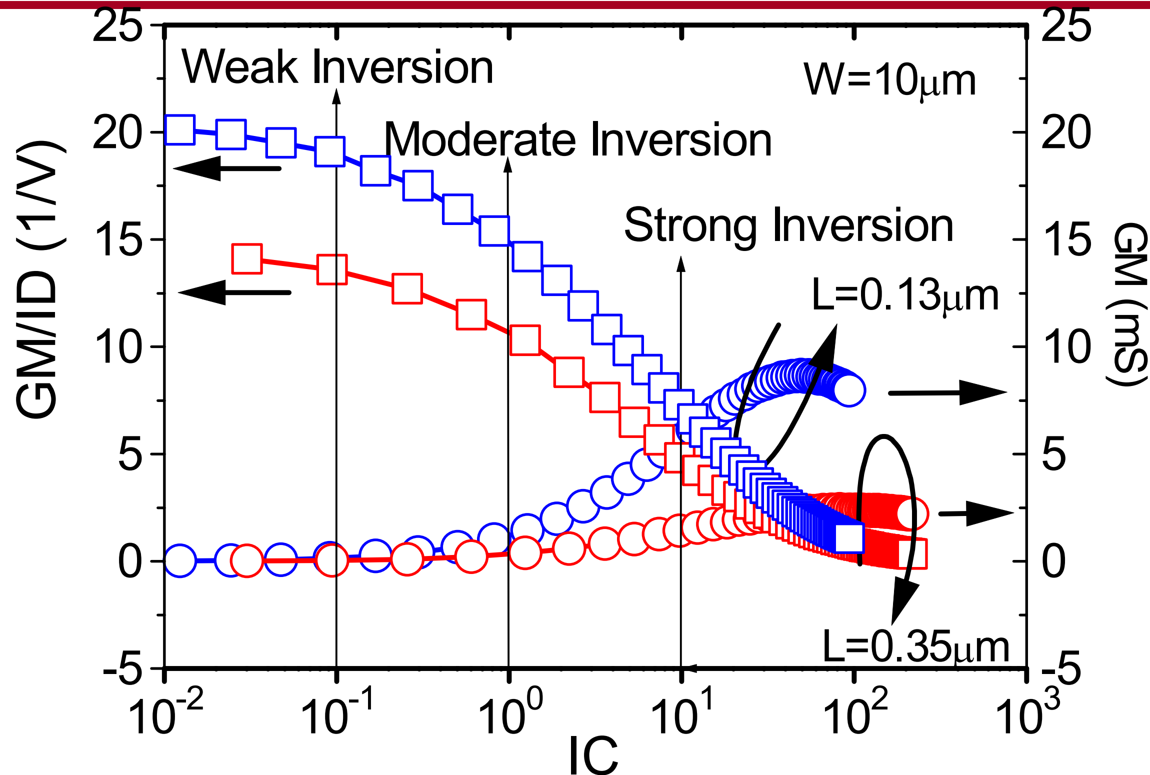
MOSFET Modeling Challenges

- Core model with good continuity, accuracy and scalability over wide biases, temperatures and geometries.
- Modeling of classic well-known short channel and narrow width effects and recent advanced physical effects such as velocity overshoot, self-heating, channel charge quantization, tunneling, layout dependent behavior, …
- Scalable parasitic capacitance and resistance models.
- Predicts accurately the small signal AC and noise and the distortion behavior.
- Non-quasi static (NQS) effects.
- Statistical modeling

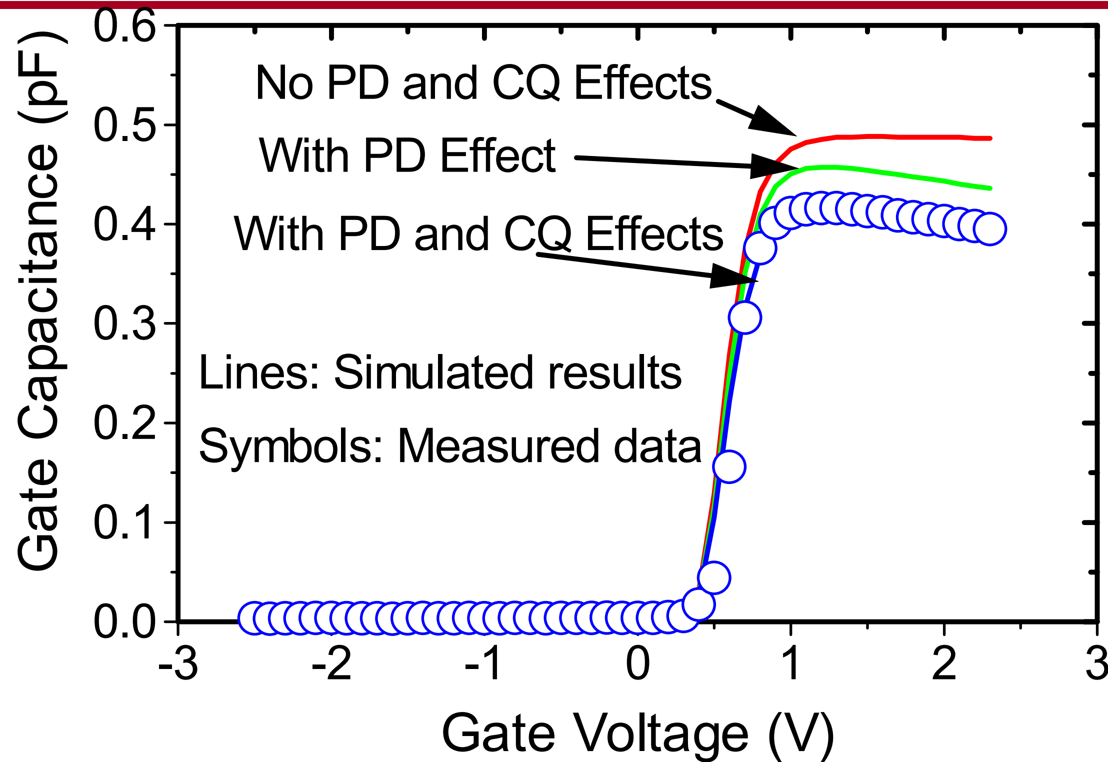
Modeling Challenges – G_m & G_m/I_D



(Yuhua Cheng, "A study of figures of merit for the high frequency behavior of MOSFETs in RF IC applications", Eighth International Conference on modeling and Simulation of Microsystems, Anaheim, May 8-12, 2005)

- G_m, the most important parameters in analog design.
- G_m/I_D, a universal characteristic of MOSFETs to evaluate the transconductance efficiency.
- Inversion Coefficient (IC), ratio of I_D/I_S, is proposed as a measure of MOS inversion level.

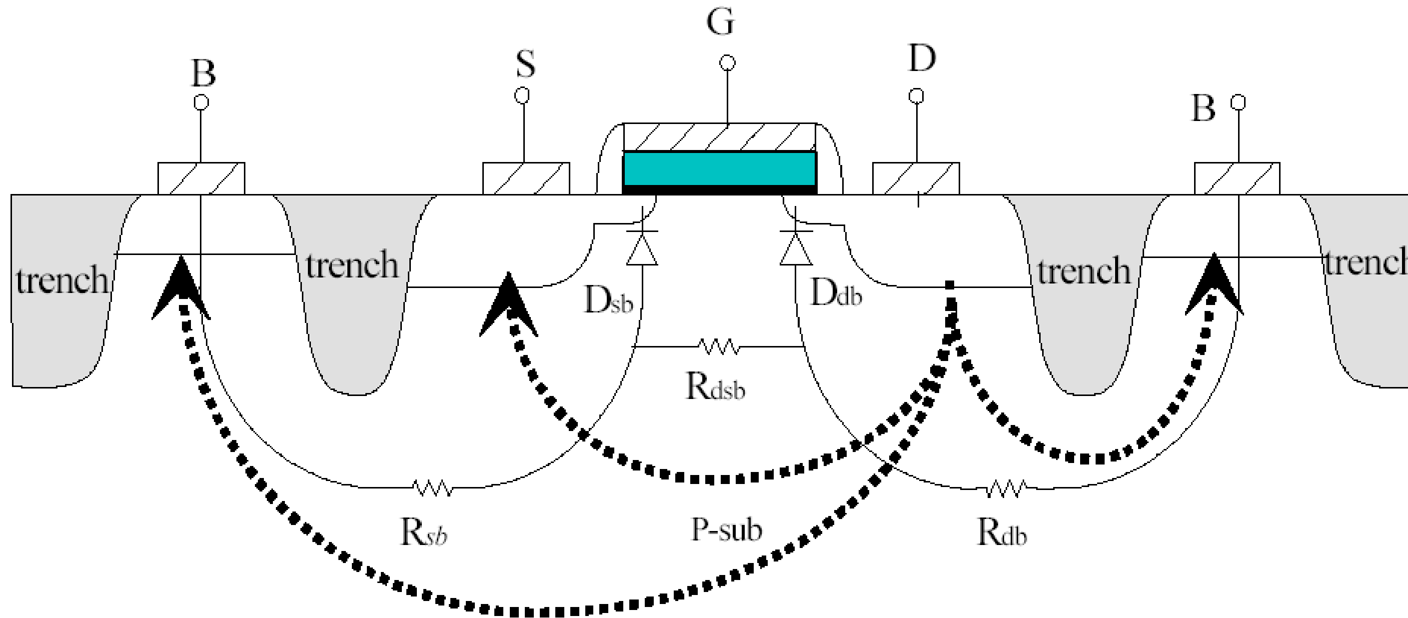
Modeling Challenges - Capacitance



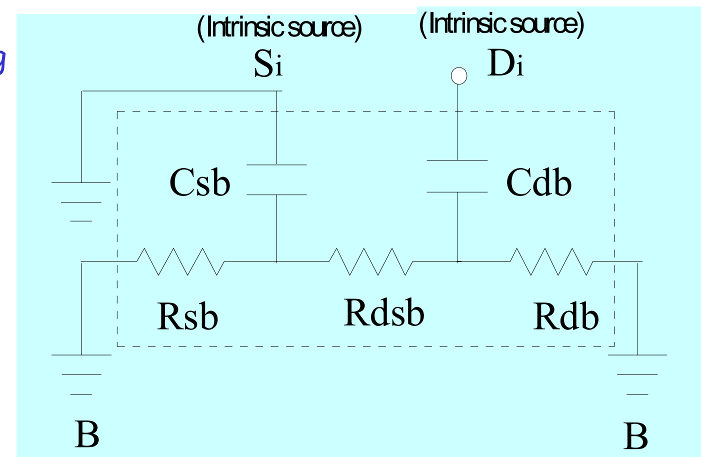
(Yuhua Cheng et al.," ICM-an analytical inversion charge model for accurate modeling of thin gate oxide MOSFETs," Simulation of semiconductor Processes and Devices,Page(s) 109 -112, 1997.)

- Gate Capacitance is not constant in strong inversion.
- Bias dependence is caused by Poly-depletion effect.
- Both poly-depletion (PD) and channel quantization (CQ) effects will impact Cgg.

Modeling Challenges – Scalable Rsub

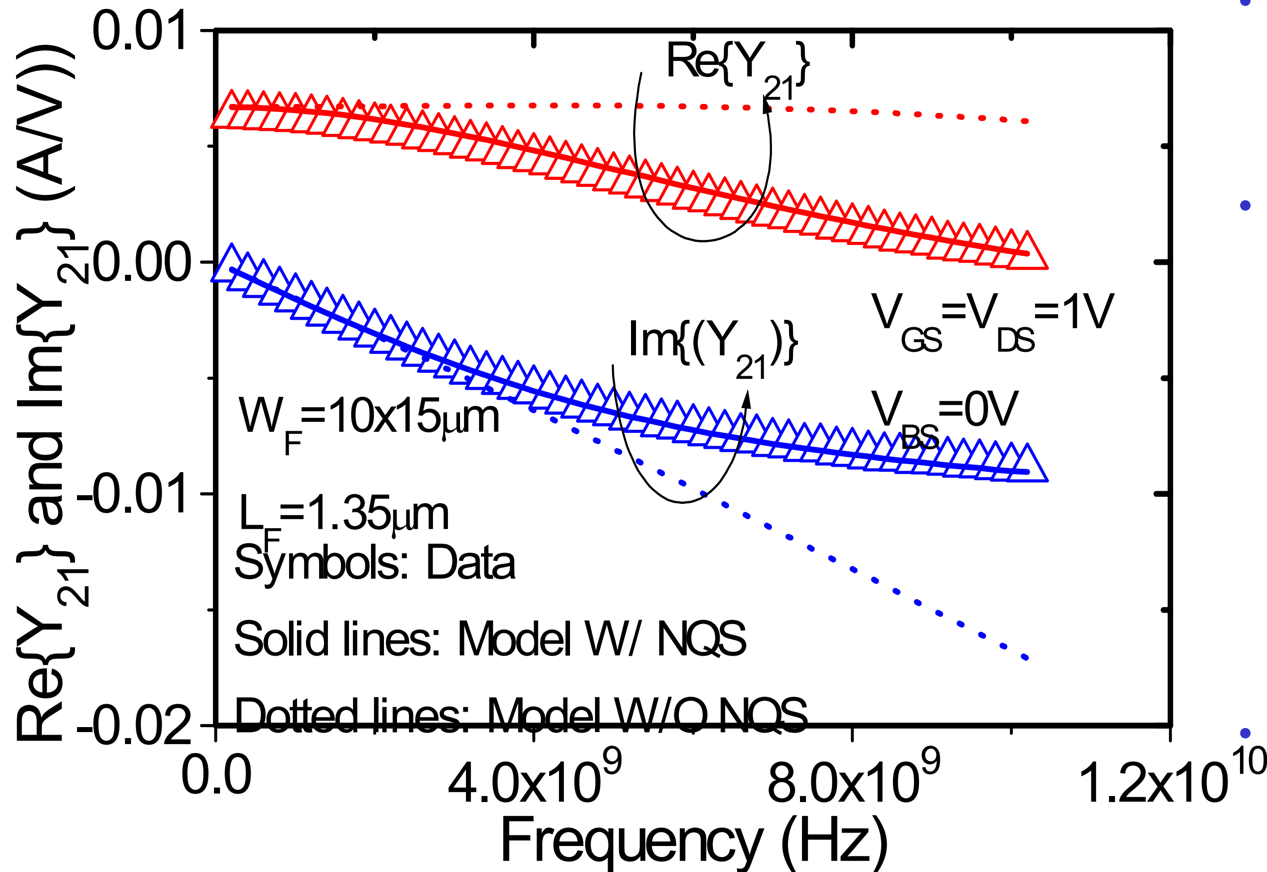


(Yuhua Cheng, "An Overview of Device Modeling in Bridging Manufacturing and Design for RF applications", International Conference on Solid-state Integrated Circuits and Technologies, D4.3-1 – D4.3-6, Beijing, China, Oct 2004)



- Rsub should be scalable in terms of channel width, length and fingers.
- All parameters should be extracted easily.

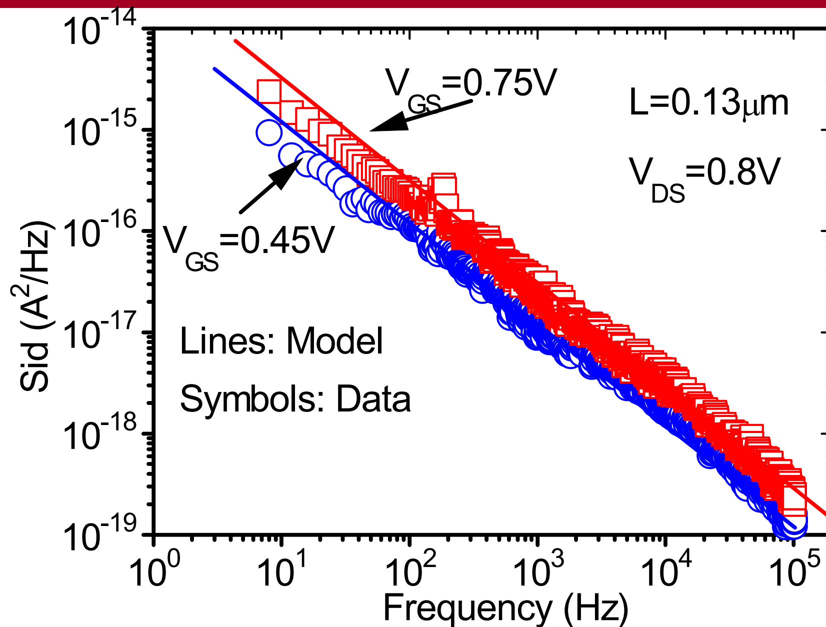
Modeling Challenges - NQS Effects

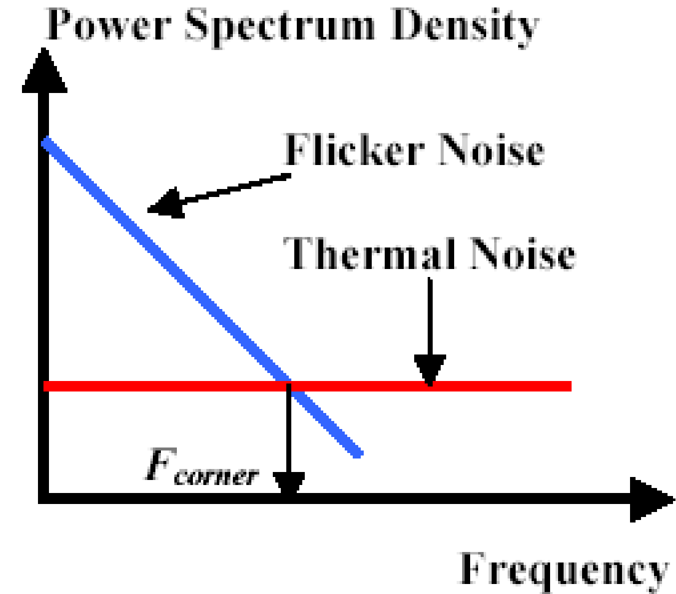


(Yuhua Cheng et al. , "Frequency-dependent resistive and capacitive components in RF MOSFETs ," IEEE Electron Device Letters , Vol. 22, pp. 333 -335, July 2001.)

- NQS will significantly impact Y_{11} and Y_{21} behavior.
- Many approaches are proposed to model this effect:
  - Multi-segment approach
  - Relaxation time
  - Rg/Ri equivalent circuit approach
- Efficient built-in NQS effect in intrinsic core model is preferred.

Modeling of Flicker noise





(Yuhua Cheng, "A study of figures of merit for the high frequency behavior of MOSFETs in RF IC applications", Eighth International Conference on modeling and Simulation of Microsystems, Anaheim, May 8-12, 2005)

- Downscaling may degrade flicker noise behavior.
- Modeling of flicker noise in nano-scale devices becomes more challenging.
- Accurate prediction of corner frequency, Fcorner, is critical for circuit design.

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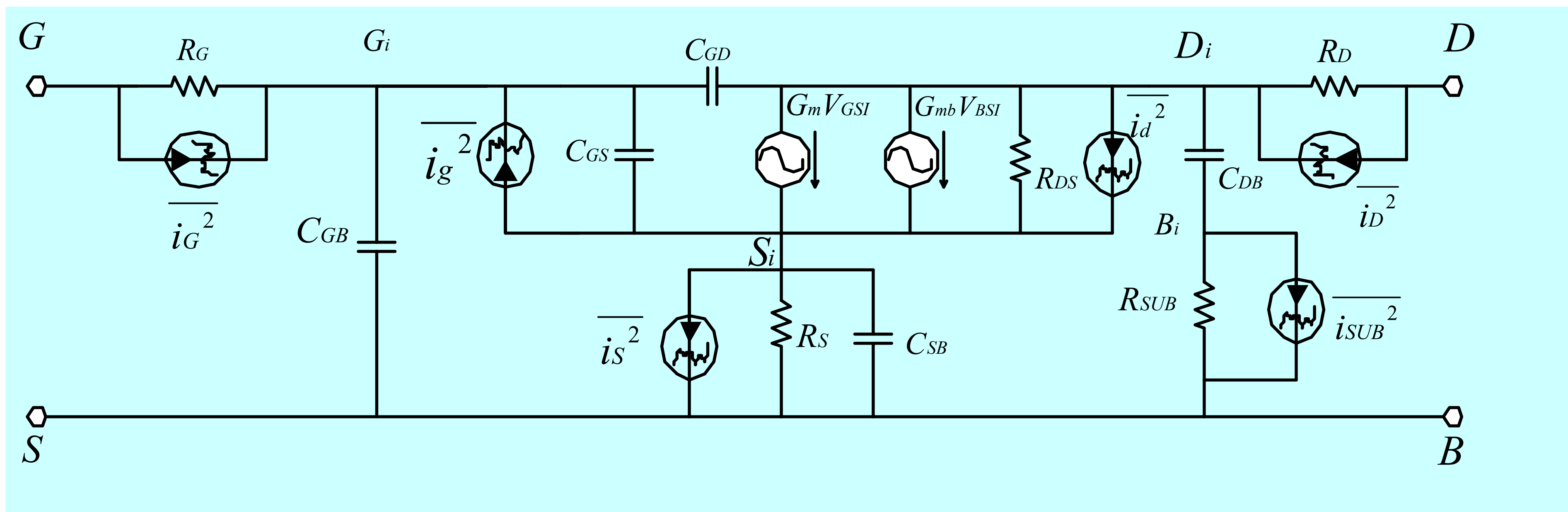
Modeling Challenges - HF Noise



- Parasitic resistance at gate, source, drain and substrate generate thermal noise
- Channel thermal noise is the dominant noise source at HF.
- Understanding of noise sources is important.
- Modeling of channel thermal noise and induced gate noise is the most challenging job.

Statistical Modeling

- Process variation (even within a wafer) in today's advanced technologies becomes more significant.
- Need physical statistical models to predict process variation and local mismatch to optimize analog/RF circuits with high yield.
- Correlations between statistical modeling with considerations of both frontend and backend process variations and yield modeling/prediction should be developed.
- In nano-scale technologies, statistical model is more meaningful than traditional corner models.

RF Modeling in Nano-scale Era

Continuity

Scalability

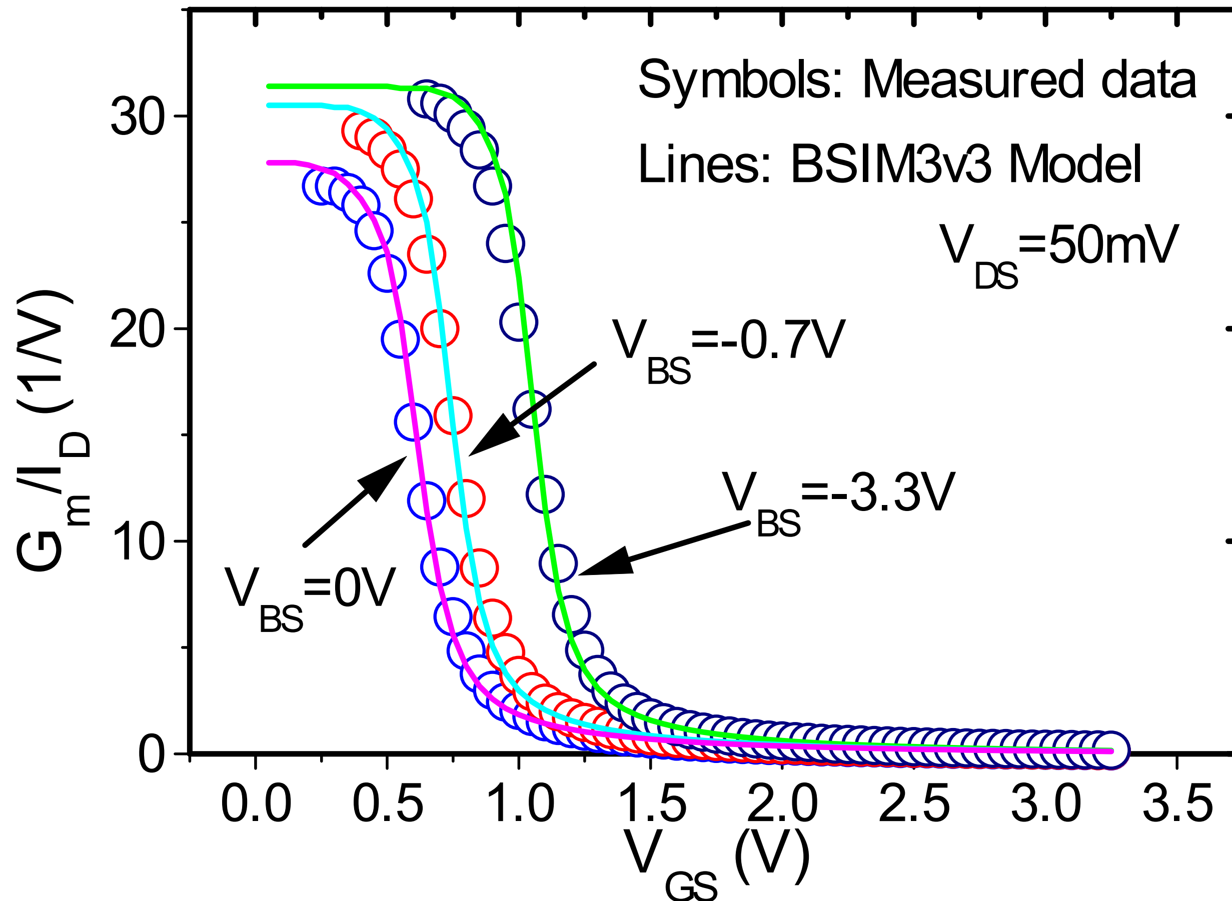
Accuracy

New
Physical Effects

Computation
Efficiency

Modeling of Small Signal, Noises,
Large Signal Distortion
For RF Applications

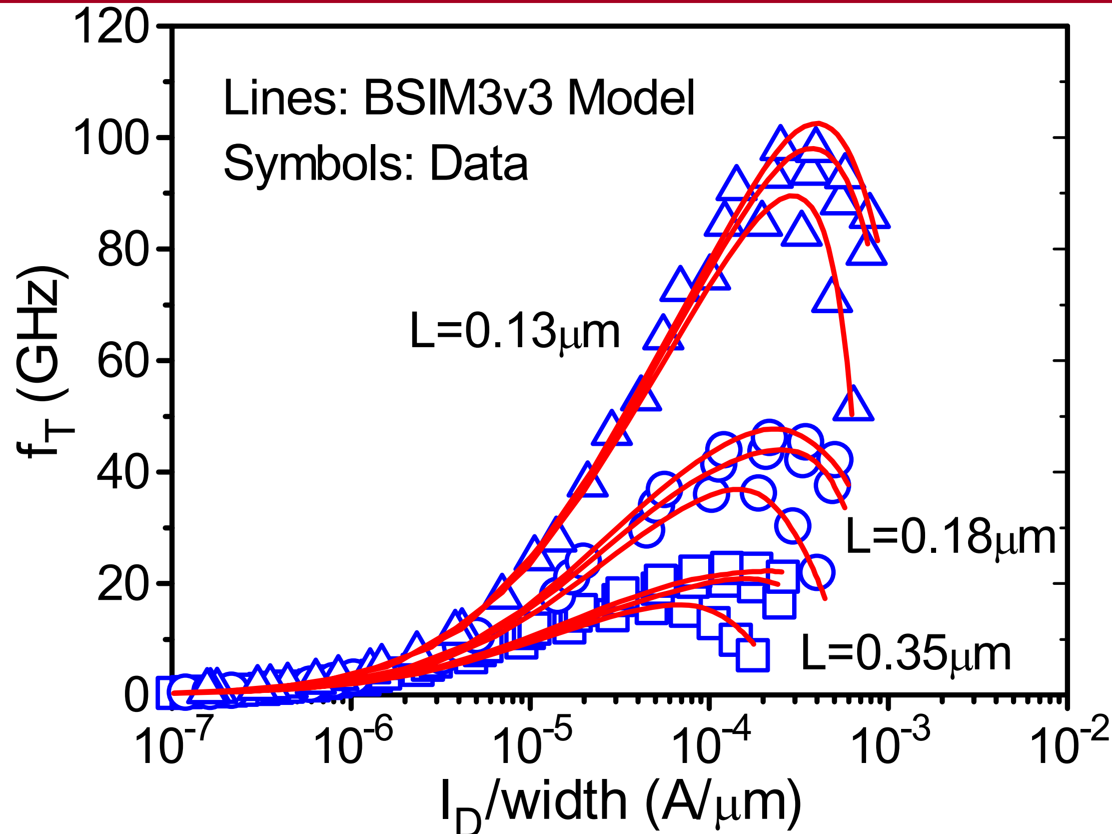
G_m/I_D: Measured vs. Fitted



(Yuhua Cheng, "A study of figures of merit for the high frequency behavior of MOSFETs in RF IC applications", Eighth International Conference on modeling and Simulation of Microsystems, Anaheim, May 8-12, 2005)

- G_m/I_D has been proposed a FoM for model validation for analog applications.

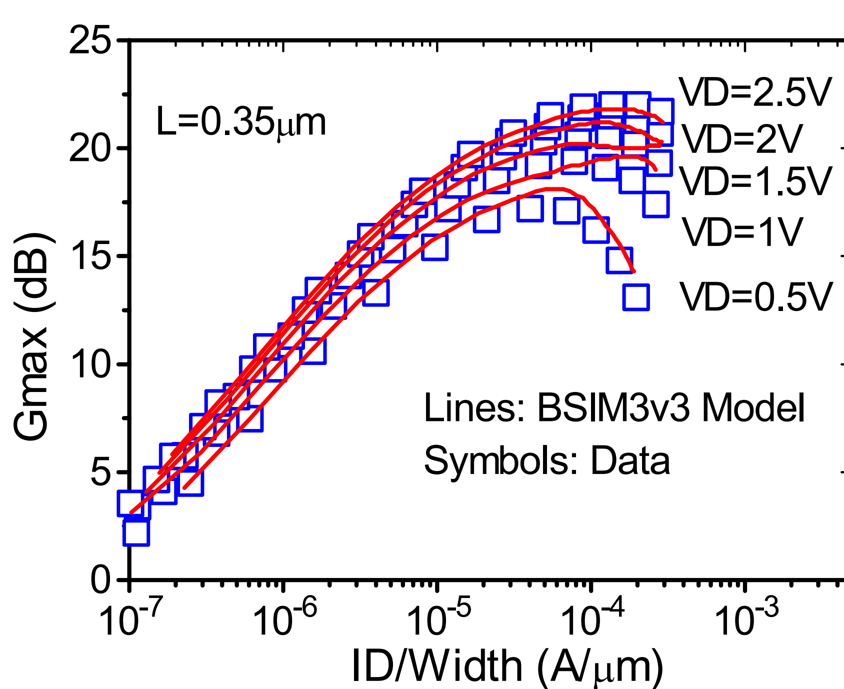
f_T: Measured vs. Fitted

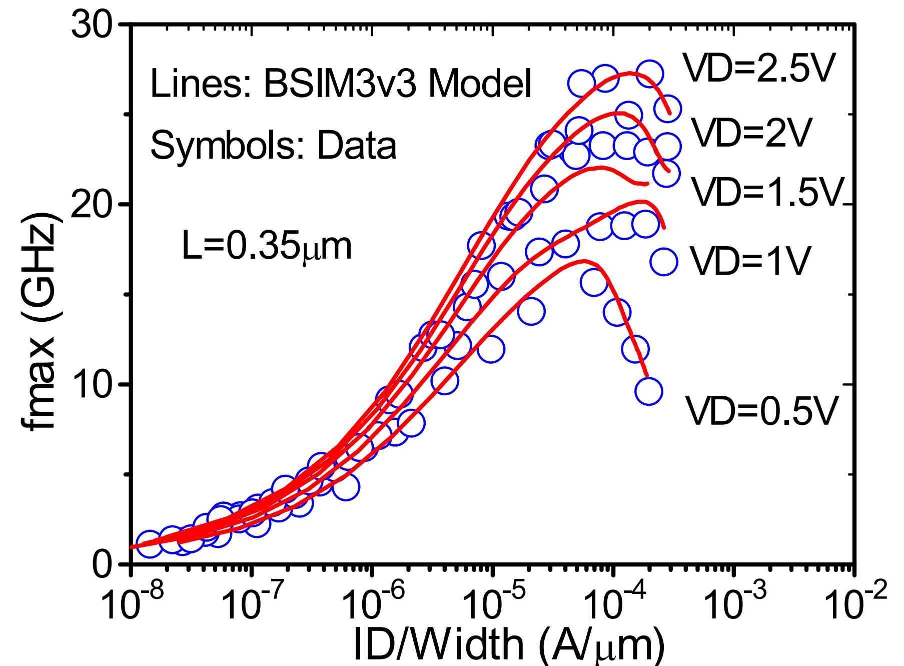


(Yuhua Cheng, C. H. Chen, M. Matloubian, and M. J. Deen, "High frequency small signal AC and noise modeling of MOSFETs for RF IC design," *IEEE Transactions on Electron Devices*, Vol. 49, pp. 400 – 408, March 2002.)

- A standard device parameter for model validation.
- However, only f_T is not enough to describe HF behavior of MOSFETs, especially at technology nodes such as 0.13um and below.

G_{max} and f_{max}: Measured vs. Fitted





(Yuhua Cheng, "A study of figures of merit for the high frequency behavior of MOSFETs in RF IC applications", Eighth International Conference on modeling and Simulation of Microsystems, Anaheim, May 8-12, 2005)

- f_{max} contains the impacts from parasitics such as gate and substrate resistance and is a better FoM than f_T

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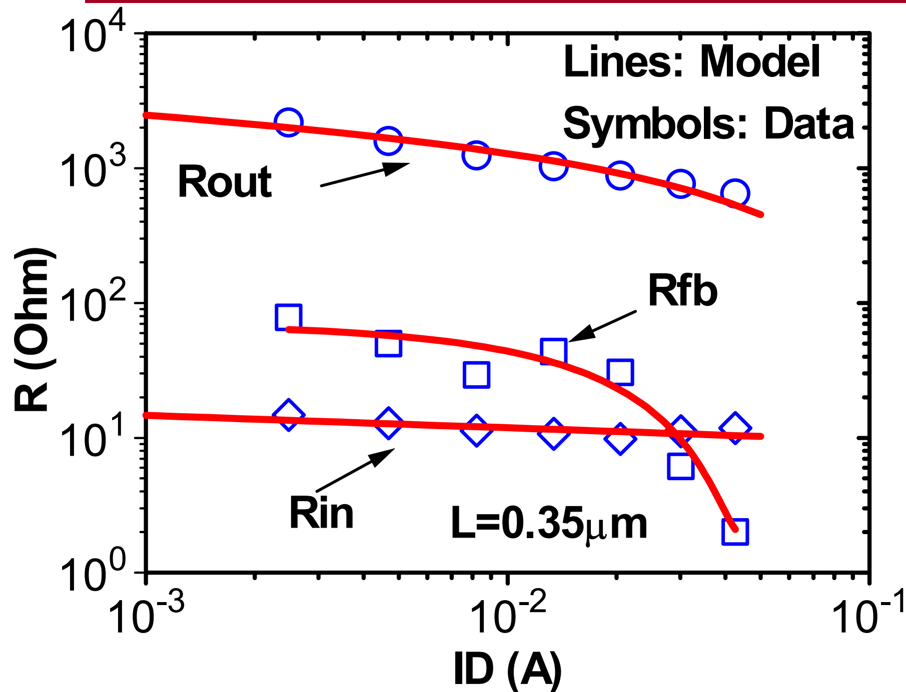
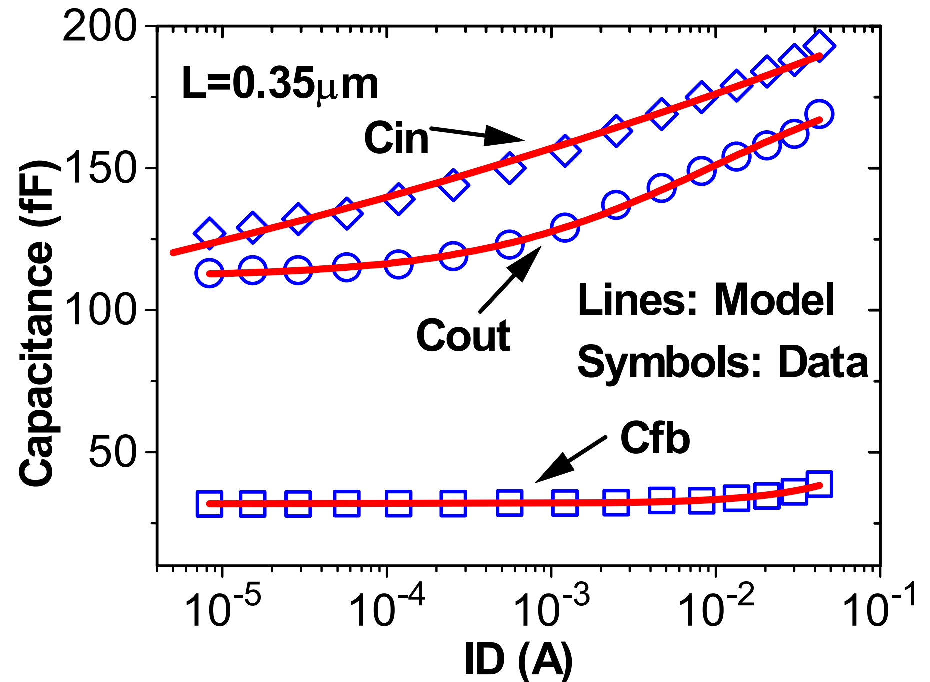
C-parameters: Modeled vs. Fitted





(Yuhua Cheng, "A study of figures of merit for the high frequency behavior of MOSFETs in RF IC applications", Eighth International Conference on modeling and Simulation of Microsystems, Anaheim, May 8-12, 2005)

- C-parameters are more sensitive to the bias dependence of gate resistance and capacitance.
- Useful FoMs for model validation.

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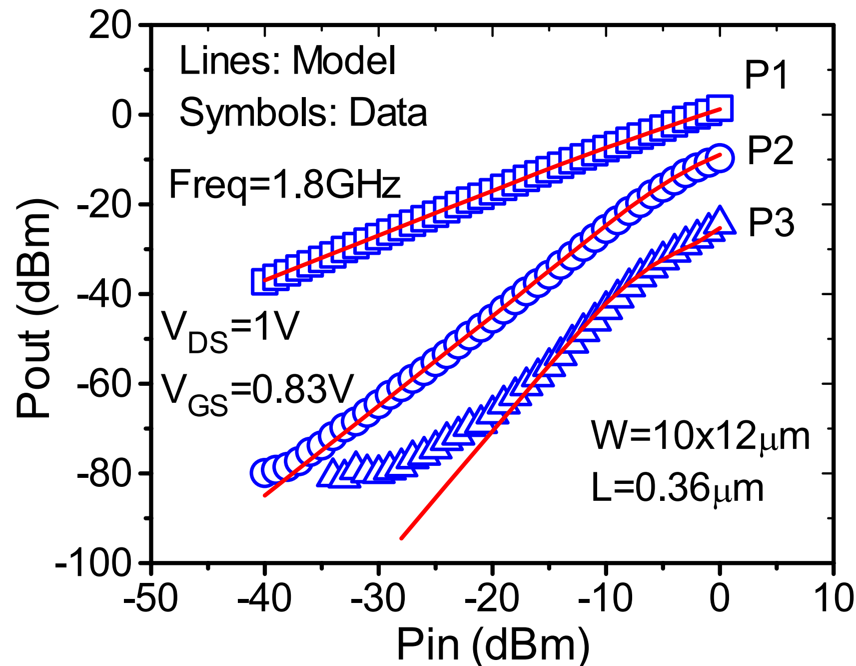
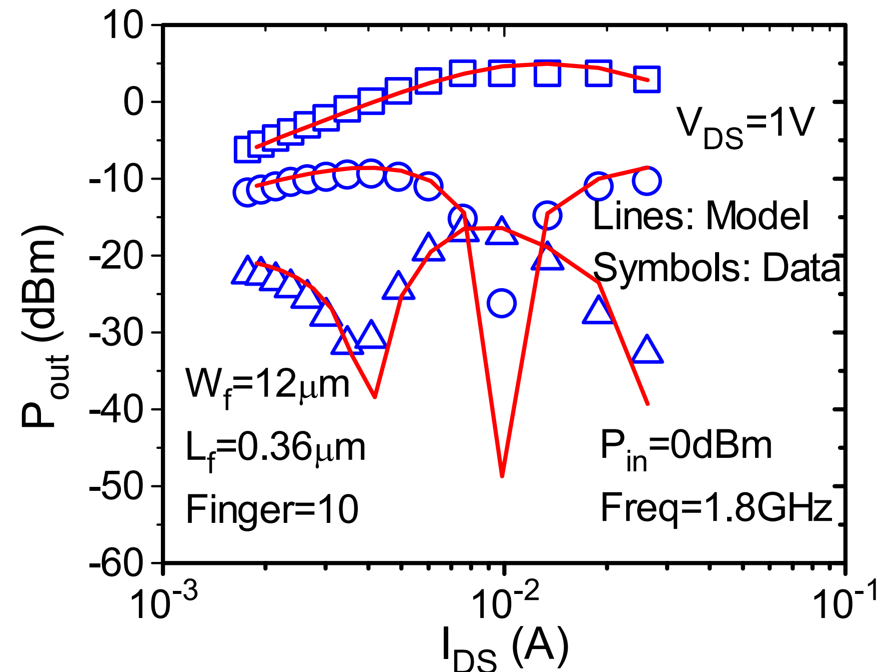
Large Signal Behavior: Measured vs. Fitted





(Tzung-Yin Lee, and Yuhua Cheng, "High-Frequency Characterization and Modeling of Distortion Behavior of MOSFETs for RF IC Design," *IEEE Journal Of Solid-State Circuits*, VOL. 39, NO. 9, pp. 1407 – 1414, September 2004)

- Below certain (the "LFL") frequency, the distortion behavior of MOSFETs is primarily determined by transconductance and capacitances.
- With careful parameter extraction at DC and HF small signal, a model can well predict the large signal distortion behavior.

Something worth mentioning in RF Modeling

Validate Models
Based On Meaningful
Figures-of-Merit

Summary

- While all the requirements for continuity, scalability, accuracy and computation efficiency need to be met for device models for circuit simulation, the new physical effects in nano-scale devices make compact model development very challenging.

- A lot of additional modeling efforts to predict HF noise and large signal distortion behavior are needed for RF circuit design.

- It would be desirable in the future the modelers use certain FoMs at HF to qualify the device models targeted for analog/RF applications.

- Device modeling has become very critical component in the technology platform for RF SOC design in nano-scale technologies.

Thank you for your attention

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