Designing CMOS Wireless System-on-a-chip

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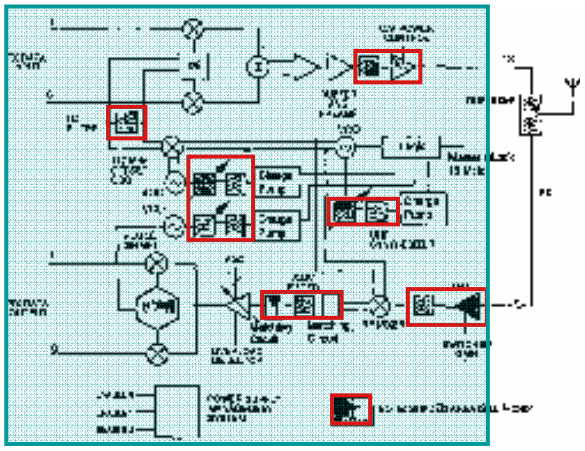
Outline

- **Introduction**
- **CMOS Transceiver Building Blocks**
  - **LNA and PA**
- **System-on-a-chip Integration issues**
  - **Digital Assistance and Interference**
- **Conclusion**

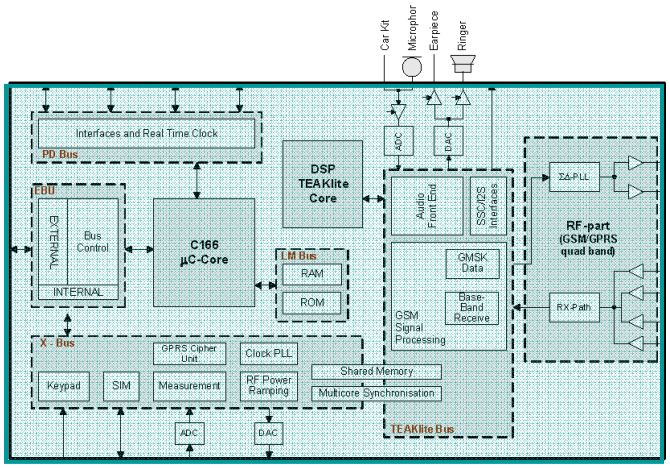
SoC Trends: GSM (1995)



Stetzler et al, ISSCC 95 (AT&T)

Integrated Transceiver with external components (e.g. filters)

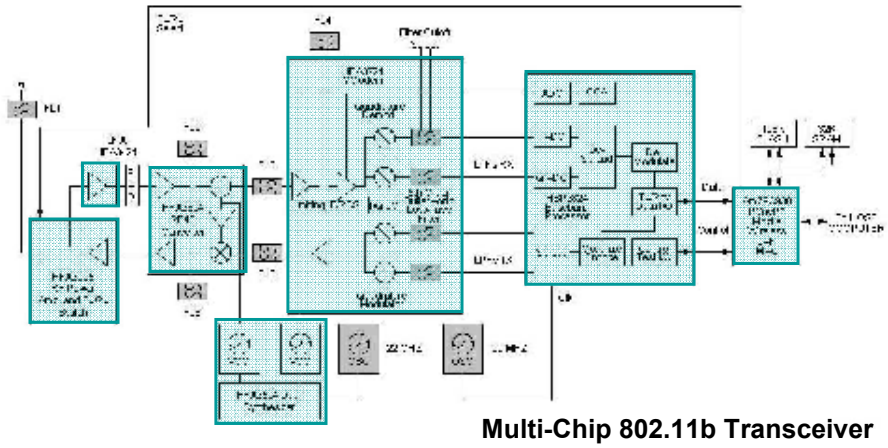
SoC Trends: GSM (2006)



Bonnaud et al, ISSCC 06 (Infineon)

SoC with integrated transceiver and CPU.

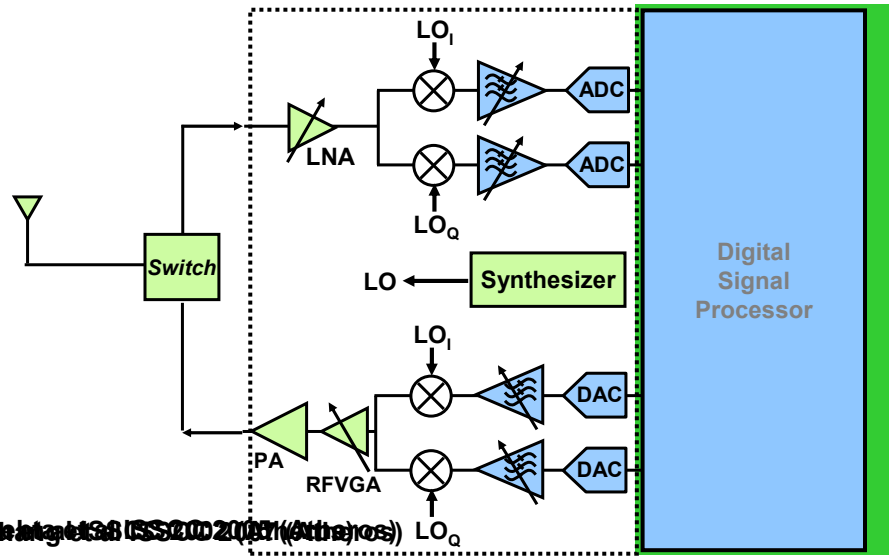
SoC Trends: WLAN (1996)



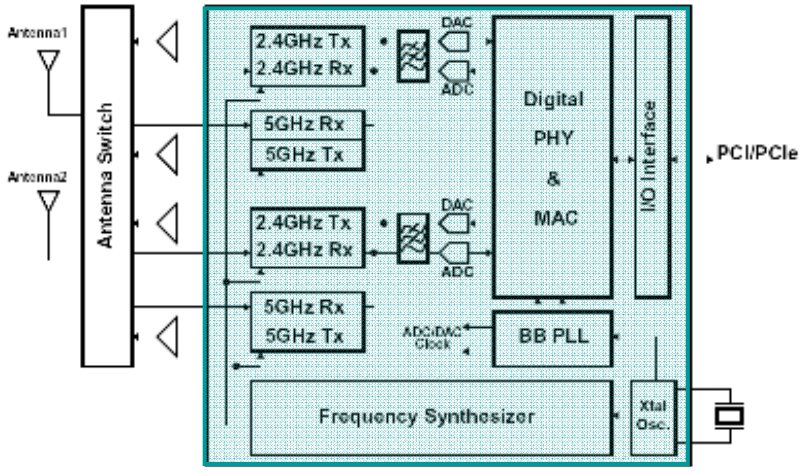
Multi-Chip 802.11b Transceiver

Prism WLAN chipset (Harris Semi) AMD App Note (www.amd.com)

WLAN Integration Story



SoC Trends: WLAN (2008)



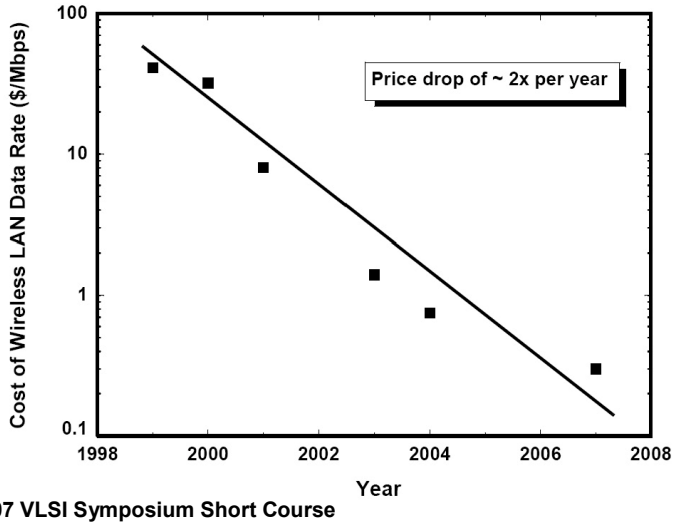
Nathawad et al, ISSCC 08 (Atheros)

11a/b/g/n (2x2 MIMO) Radio SoC

Advantages of SoC Integration

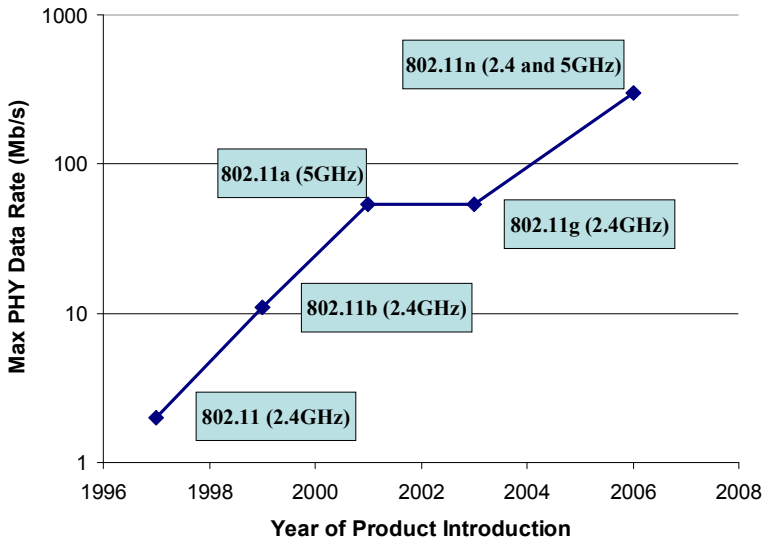
- **Increased functionality**
- **Smaller Size / Form Factor**
- **Lower Power**
  - **On-chip interface**
- **Lower Cost**
  - **Single package**
  - **Ease of manufacture**
    - **Minimum RF board tuning**
    - **Reduced component count → Improved reliability**

Cost of WLAN Throughput

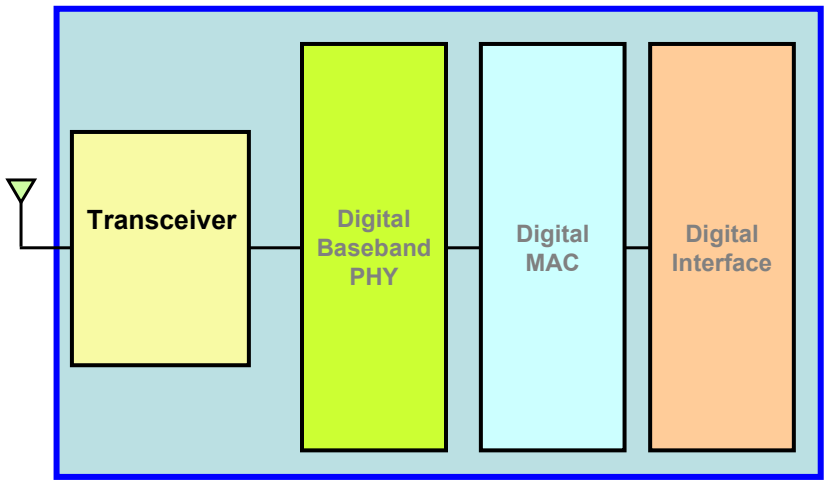


Zargari, 2007 VLSI Symposium Short Course

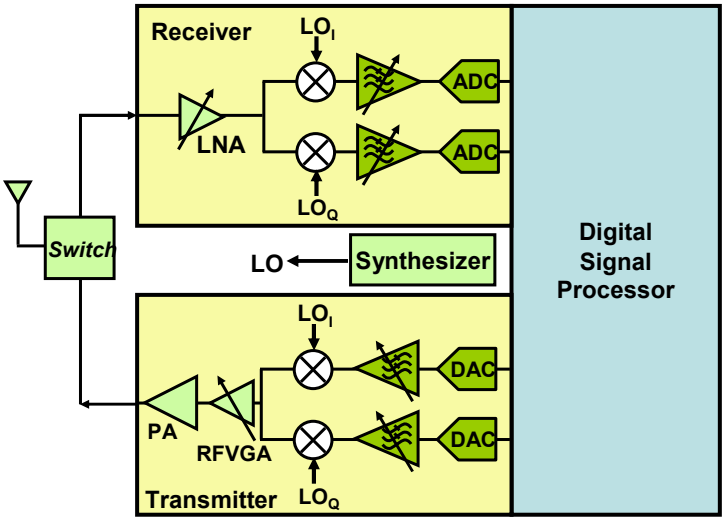
Evolution of 802.11 WLAN PHY Rates



Single-chip Radio Block Diagram



Transceiver Block Diagram



CMOS Transceiver Building Blocks

- **Signal Amplification**
- **Frequency Translation**
- **Frequency Selectivity**

CMOS RF Design

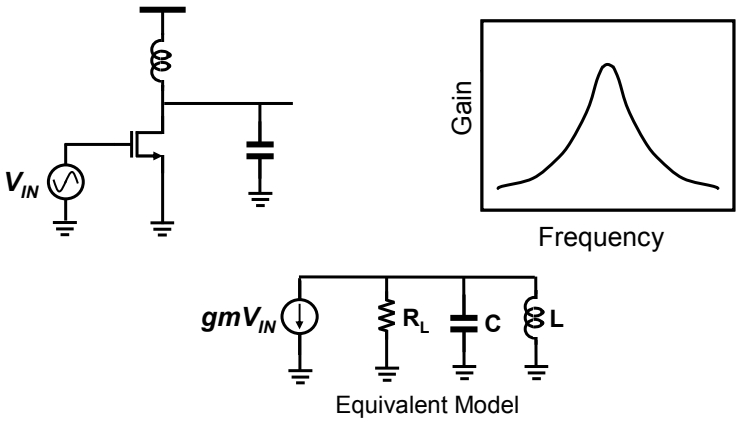
Advantages

- **Low-cost, high-yield**
- **Multi-layer interconnect makes *decent* inductors**
- **High-level of integration supports sophisticated digital signal processing**

Challenges:

- **Multi-GHz: narrowband design with inductors**
- **No high-Q BPF: architecture + dynamic range**
- **Process/Temp Variation: DSP algorithms**
- **Reduced supply headroom: IO devices**
- **Noise coupling: careful design & layout**

Tuned CMOS RF Gain stage

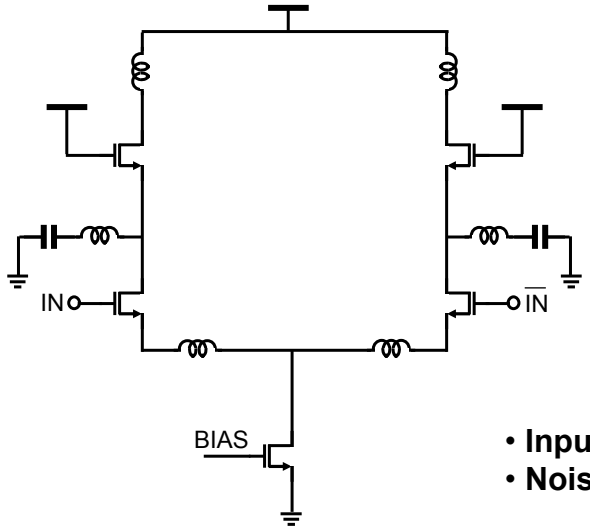


Use of Inductor
→ Narrowband tuned circuit with higher gain

LNA Design Goal

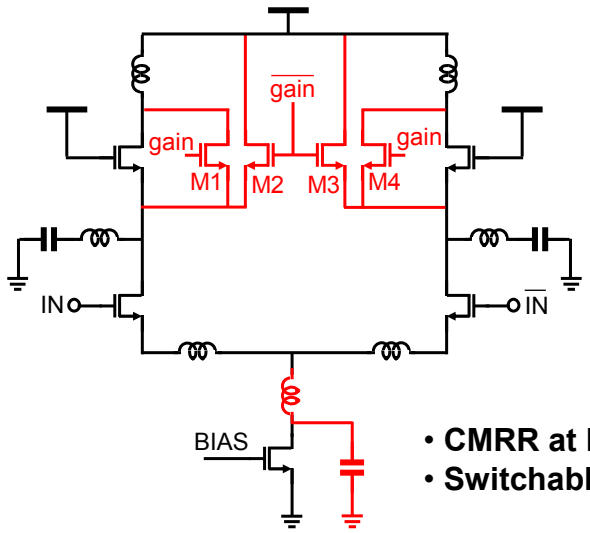
- **Low Noise Figure**
  - **Sufficient gain**
- **Able to accommodate large blockers**
  - **Large Dynamic Range**
  - **Large Common-mode Rejection**
  - **High Linearity**

LNA with Cascoded Diff Pair



- **Input match**
- **Noise Figure**

LNA with Switchable Gain



- **CMRR at RF**
- **Switchable gain for high DR**

Zargari et al, JSSC Dec 2004 (Atheros)

Linear PA for High Data Rate

Modern digital modulation attempts to transmit at highest data rate within a given signal bandwidth.

- **Nonlinear PA:**
  Information in phase only. Transmit with constant envelope for power efficiency – GSMK, FSK
- **Modestly Linear PA:**
  Information in phase only. Reduce signal bandwidth with non-constant envelope signal – π/4 QPSK, OQPSK
- **Linear PA:**
  May encode information in both amplitude and phase. Non-constant envelope; high SNR – 64 QAM

PA Peak to Average Ratio

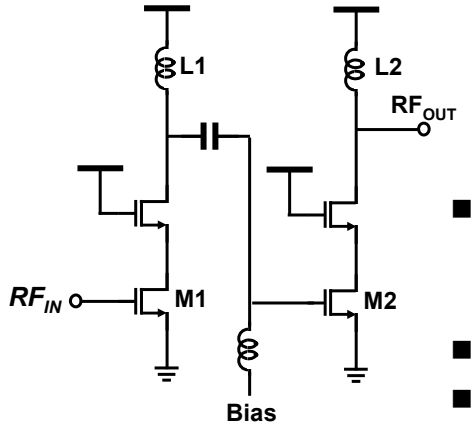
- **Improved spectral efficiency (higher bits per Hz)**
  → Large peak to average ratio
  → reduces power efficiency of the PA
- **Example: 802.11a/g OFDM has PAR of 17dB**
  - **Class A efficiency of ~ 1%**
  - **Infrequent signal peaks**
    - **16-QAM OFDM, PAR of 6dB degrades SNR by only 0.25dB***
      → Class A Efficiency ~ 12%
    - **64-QAM OFDM, PAR of 12dB is needed**
      → Class A Efficiency ~ 3%

* Van Nee & Prasad, OFDM for Wireless Multimedia Communications, Artech House, 2000

Linear Design

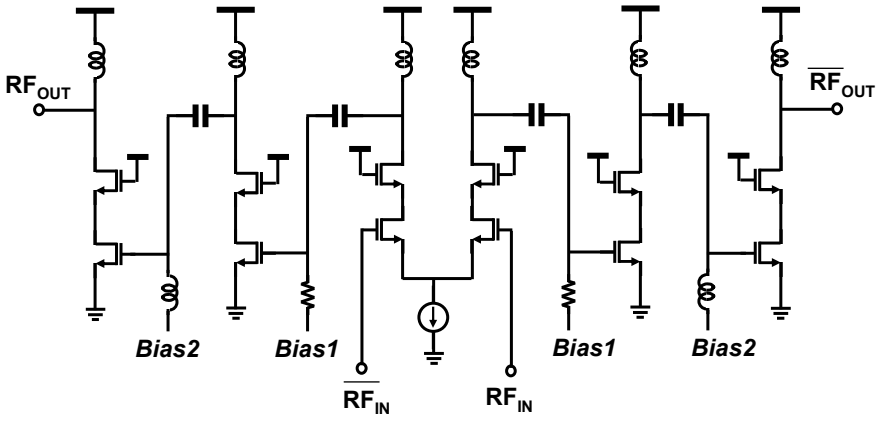
- Design for $P_{SAT} = P_{AVE} + PAR + \ldots$
  - Low R output match
- Stability
  - Cascoding
- Linearity
  - Avoid V_{GS} overdrive
  - Inter-stage capacitive level-shift

Cascoded Power Amplifier



- Cascoding advantages
  - 3.3V supply voltage
  - Stability
- Capacitive Level-shift
- Differential
  - Off-chip balun

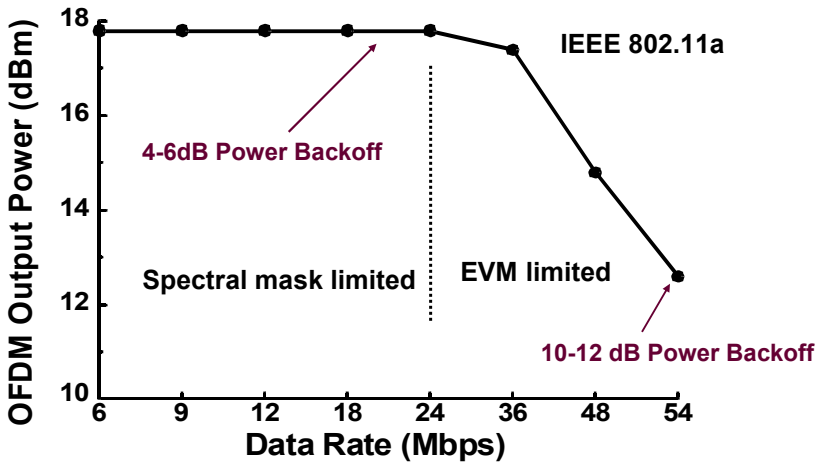
Cascoded Power Amplifier



P_{MAX} = 22 dBm P_{OFDM} = 17.8 dBm (BPSK)

Zargari et al, JSSC Dec 2002 (Atheros)

Measured Power vs Data Rate



Leveraging Integration for RF PA

Transistors are *cheap.*

- **LARGE Output Power: Nonlinear PA**
- **HIGH Efficiency: Nonlinear PA**
- **GOOD Linearity: Use linearization circuits so that the output stage does not need to be linear.**

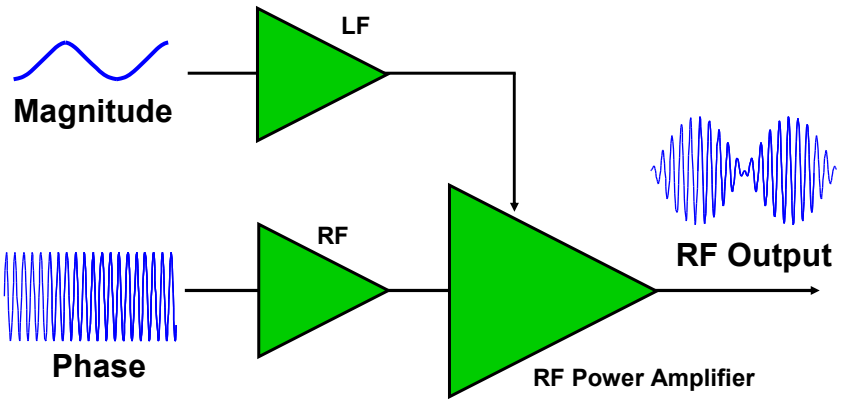
SOLUTION:
Switched-mode (non-linear) output stage + linearization.

PA Linearization

- **Concept:**
  - **Use efficient nonlinear PAs for amplification**
  - ***Techniques* to improve linearity**
- **An active research area for over half a century!**
  Some examples:
  - **Feedforward**
  - **Predistortion**
  - **Cartesian feedback: Rectangular I-Q**
  - **Outphasing / Chirex / LINC: Phase-Phase**
  - **Polar: Phase-magnitude, EER**

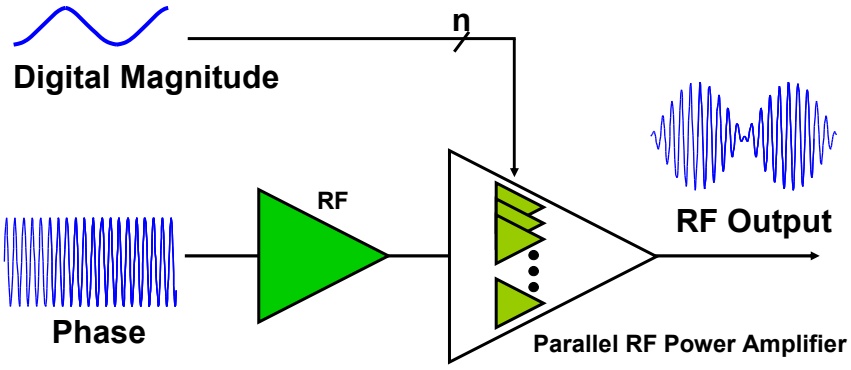
  … (many many more)

Polar

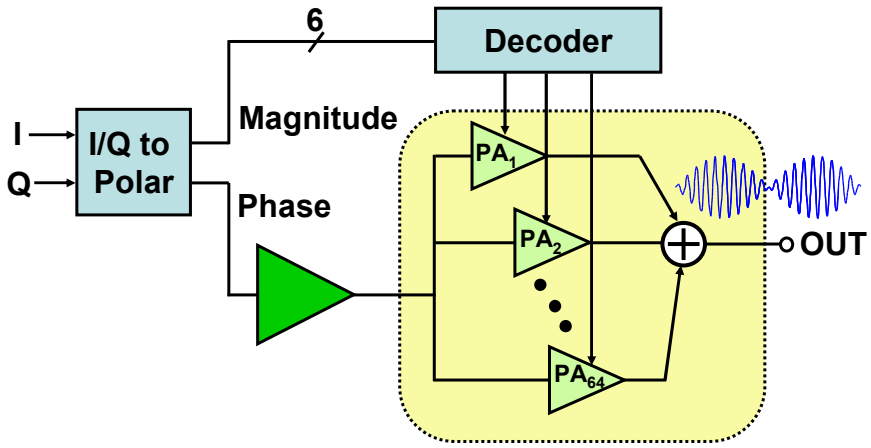


- Input = PHASE and MAGNITUDE
- Amplified separately and then combined
- Ref: L. Kahn, Proc. IRE, July 1952.

Digital Polar

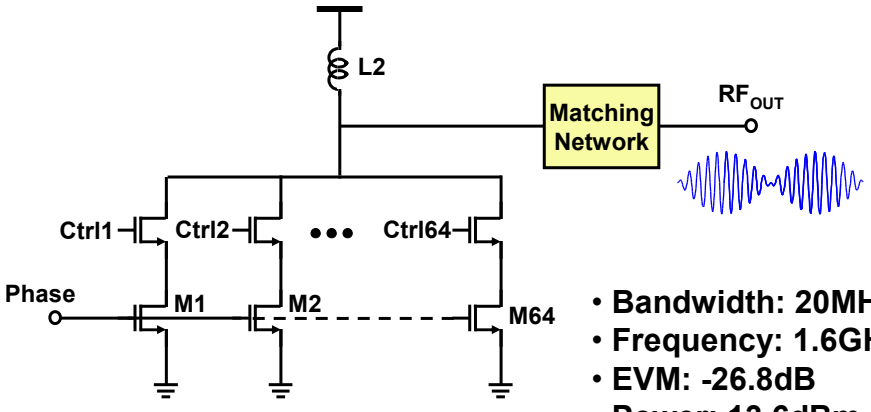


Digitally Modulated Polar Power Amplifier



Kavousian et al, ISSC 2007 (Stanford)

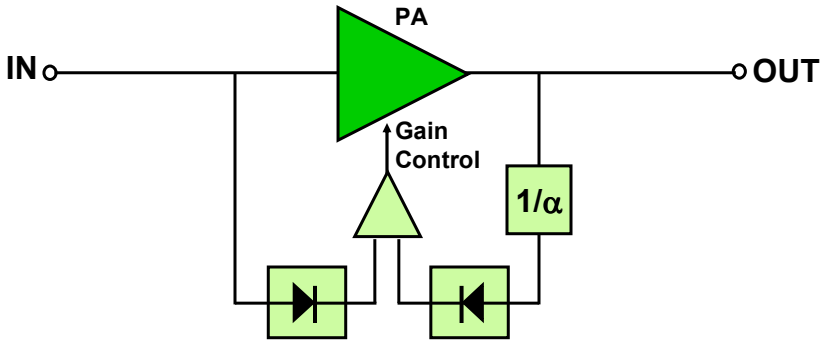
Digitally Modulated Polar Power Amplifier



- Bandwidth: 20MHz
- Frequency: 1.6GHz
- EVM: -26.8dB
- Power: 13.6dBm

Kavousian et al, ISSC 2007 (Stanford)

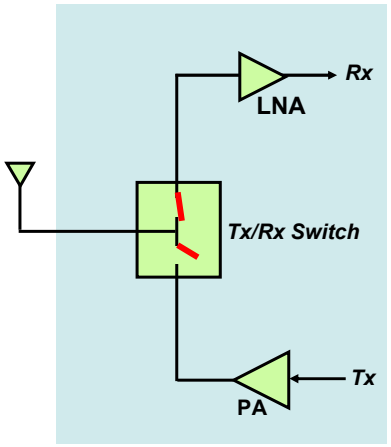
RF PA with Envelope Feedback



- **Linearizes Gain**
- **Fixes gain variation over process and temperature**

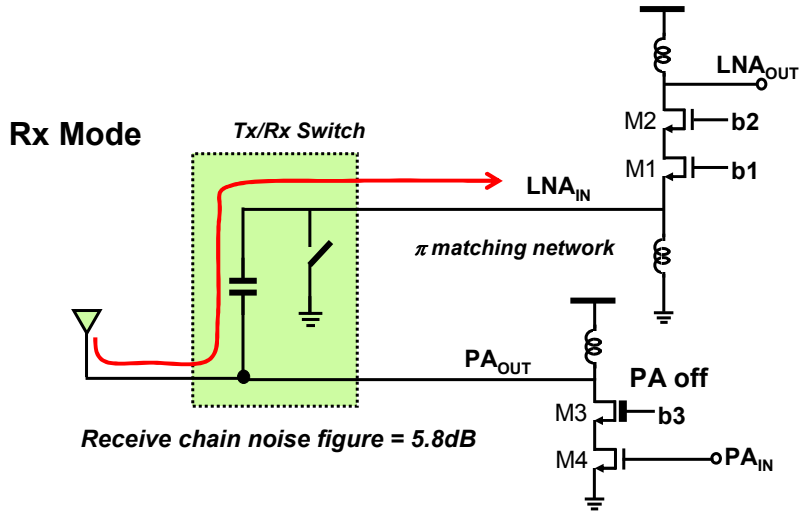
Terrovitis et al, ESSCIRC Sept 2009 (Atheros)

Integrating RF Tx/Rx Switch in CMOS



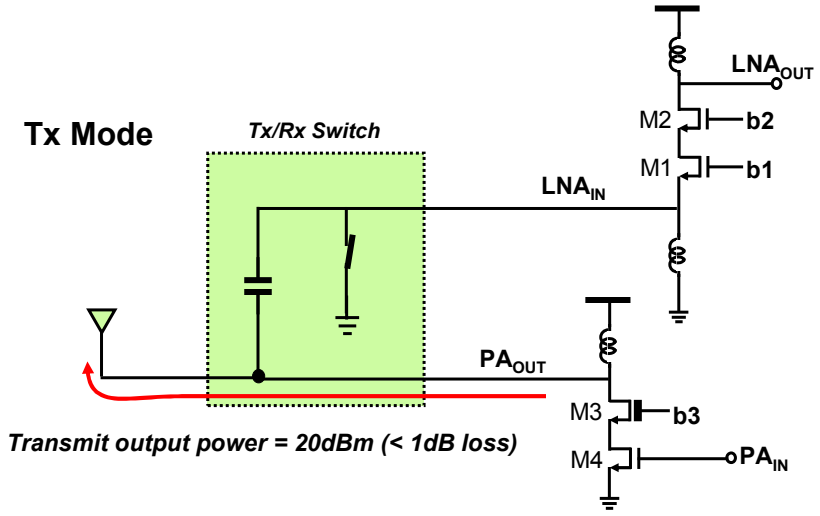
- MOS pass transistors as switches has too much loss and may not be able to support required voltage breakdown

Integrated RF Tx/Rx Switch



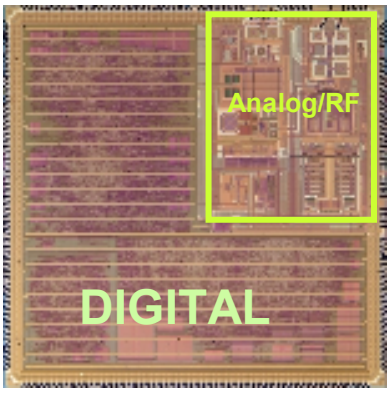
Chang et al, ISSCC 2007 (Atheros)

Integrated RF Tx/Rx Switch



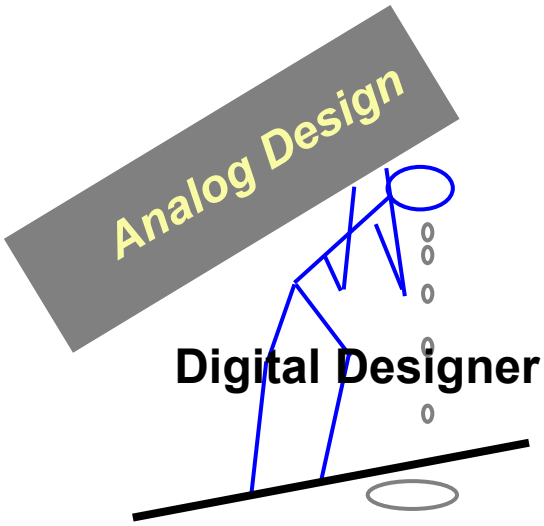
Chang et al, ISSCC 2007 (Atheros)

System-on-a-Chip Integration



- ✓ Digital Assistance: Calibration Techniques
- Digital Interference: Noise Coupling

Digital Assisted Analog Design



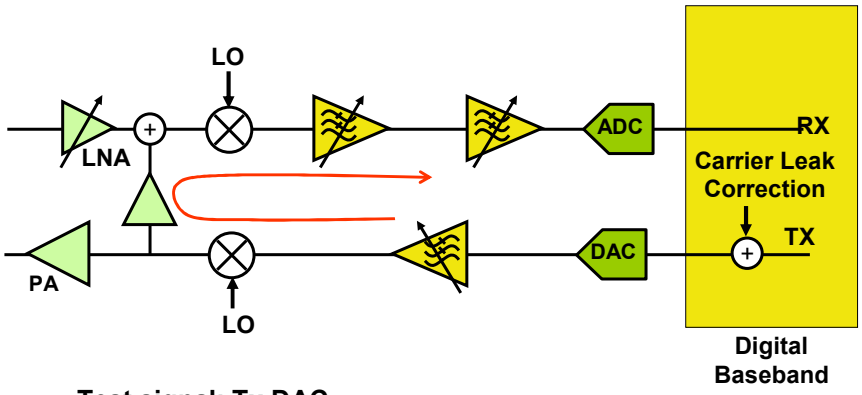
Digital Assistance: Calibration Issues

- Digital logic to compensate/correct for imperfections of analog and RF circuits can enable:
  - Lower power, smaller area, improved reliability of analog/RF
- Desired properties of calibration:
  - Independent of temperature, aging, frequency
  - Inexpensive (in area and power) to implement
  - Do not interfere with system performance
- Wireless SoC advantage:
  - Calibration building blocks already exist on-chip: transmitter and receiver, data converters, and CPU
  - No package pin limitation

Calibration Techniques

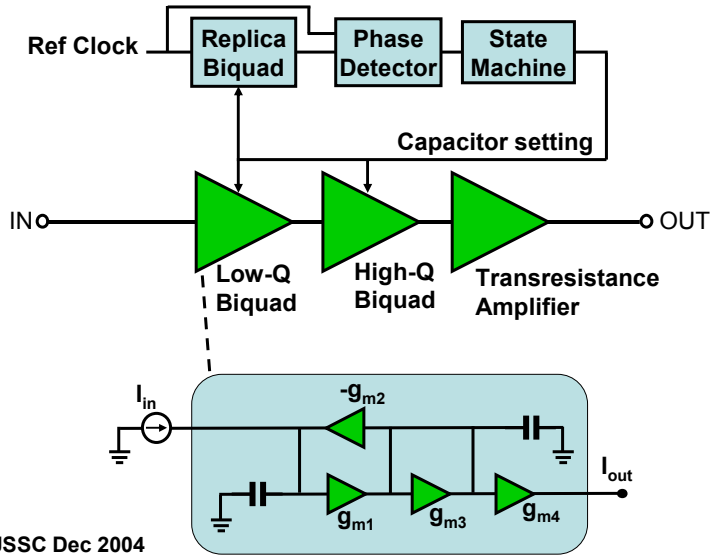
- Test Signal
  - Dedicated test signals from DAC: Tx carrier leak
  - RF loop back: Receive filter bandwidth
  - Thermal noise: Rx Gain
  - Live Rx (signal) traffic: Rx I/Q mismatch
- Observation Signal
  - Dedicated ADC
  - Implicit ADC: Comparator
- Tuning Mechanism
  - Dedicated DAC
  - Implicit DAC:
    Selectable capacitors, resistors, transistors

RF loop back: Tx Carrier Leak



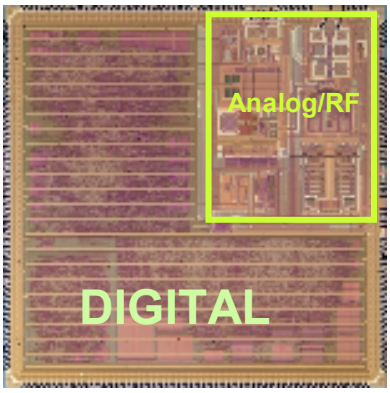
- Test signal: Tx DAC
- Observation signal: RF loop back to Rx ADC
- Tuning: Carrier Leak Correction at Tx DAC input

Calibrating Low-pass gm-C Filter



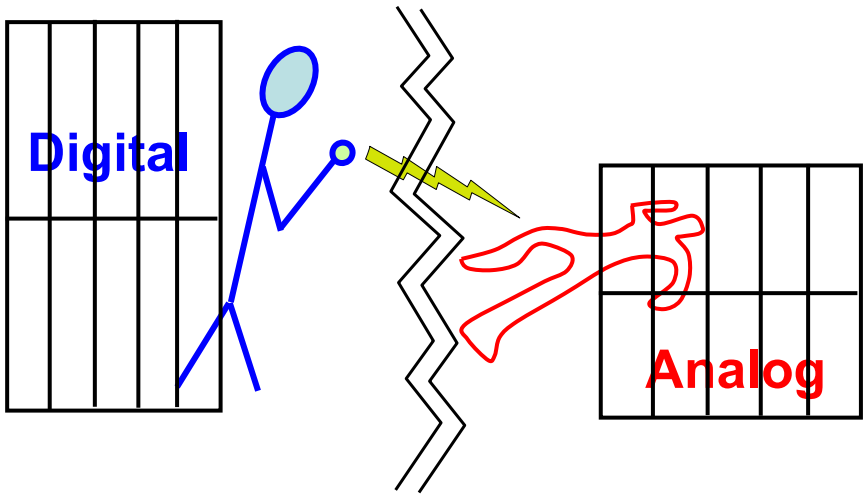
Zargari et al, JSSC Dec 2004

System-on-a-Chip Integration

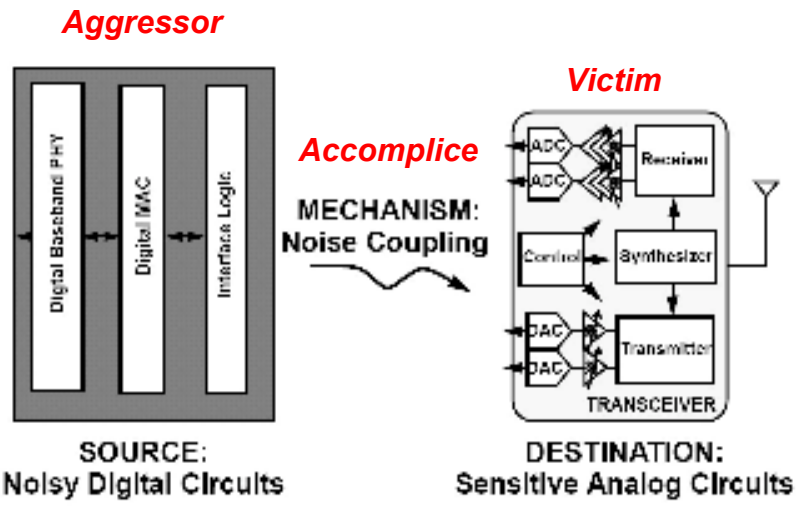


- Digital Assistance: Calibration Techniques
- ✓ Digital Interference: Noise Coupling

Digital Interference



Digital Interference: Noise Coupling



Noise Source

Pacify the aggressor

- **Reduce noise by turning off unused digital**
  - **Clock gating**
  - **Avoid oversized digital buffers**
- **Stagger digital switching**
  - **Avoid large number of digital pads switching simultaneously**
  - **Avoid switching digital logic at the same sampling instance of sensitive analog**

Noise Destination

Strengthen the victim

- Increase immunity of sensitive analog and RF circuits
  - Common-mode noise rejection:
    → Fully differential topology
  - Power Supply noise rejection:
    → Good PSRR
    → Dedicated on-chip voltage regulators
- Avoid package coupling by keeping sensitive nodes on chip
  (Example: VCO control voltage)

Coupling Mechanism

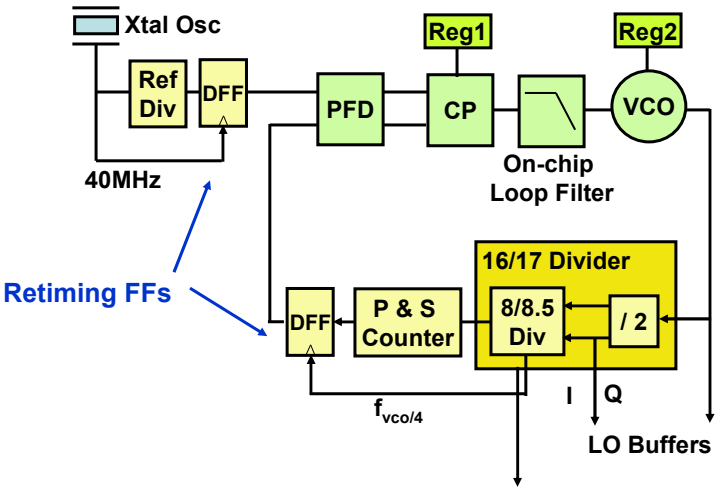
Deter the accomplice

- Supply noise coupling
  - Separate or star-connected power supplies
- Capacitive or inductive coupling to sensitive signals and bias voltages
  - Careful routing of signal traces to reduce parasitic capacitive/inductive coupling
  - Use ground return-path shields

Coupling Mechanism (Cont'd)

- Epi vs non-epi substrate
- Substrate coupling induced V_{TH} modulation
  - Low-impedance substrate connection
  - Guard rings
  - Physical separation
  - Deep Nwell

Frequency Synthesizer



Terrovitis et al, ISSCC 2004 (Atheros)

Conclusions

- CMOS has become the technology of choice for integrated radio systems
- Integrating a radio in mixed-Signal System-on-a-Chip is no longer a dream but a reality
- Wireless SoC can provide significant advantages in size, power, and cost

Continuing Challenges

- Multi-mode radios to support several wireless standards
- RF design in scaled CMOS
  - Reduced supply voltage: voltage, current, time
  - nanometer transistors: leaky, low gm.ro
  - How to reduce analog/RF area and power: less analog and more digital
- Challenge of radio designers will still be:
  - Power consumption / Battery life
  - Range
  - Data rate
  - Cost

Acknowledgments

- **Many of the slides are based on previous presentations from Atheros Communications and Stanford University, especially those by:**

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