Challenges in achieving first-silicon success for 10M-gate SoCs: A silicon engineering perspective (Updated & Expanded)

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IEEE Solid State Circuits Society - Santa Clara Valley
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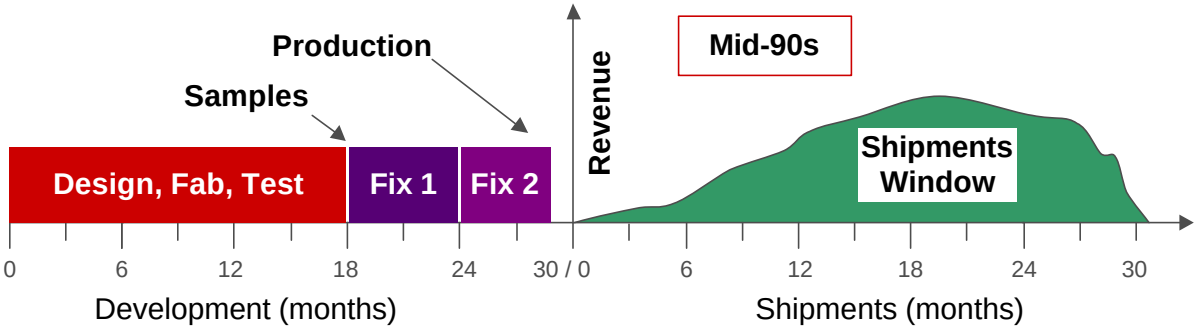
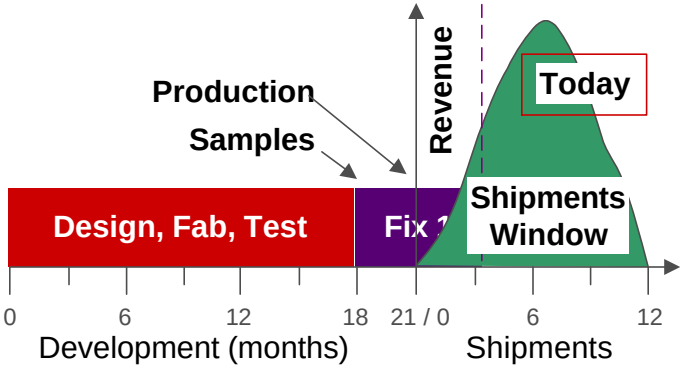
Topics

- Motivation
- Design challenges
- Silicon Engineering focus
- Design approach
  - Design challenges and solutions
  - Innovative design technology
- Results
- Summary

There is no market …for a second-to-market

Market Trends	2002	2006
SoC semiconductor revenues	$ 23B	$ 53B
SoC design starts (% ASIC)	59%	80%



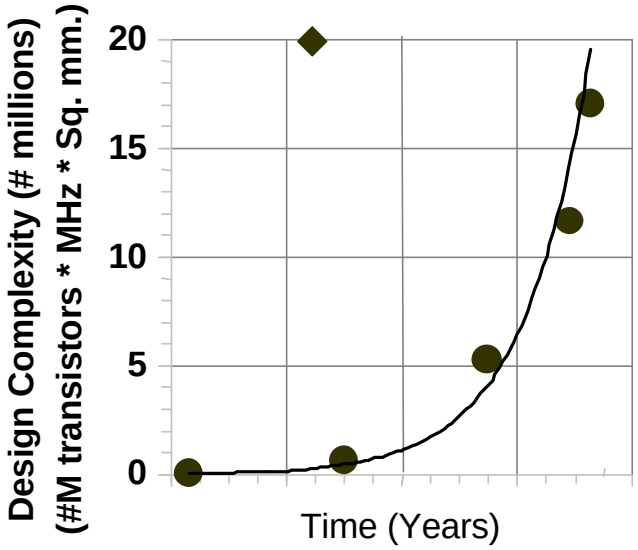


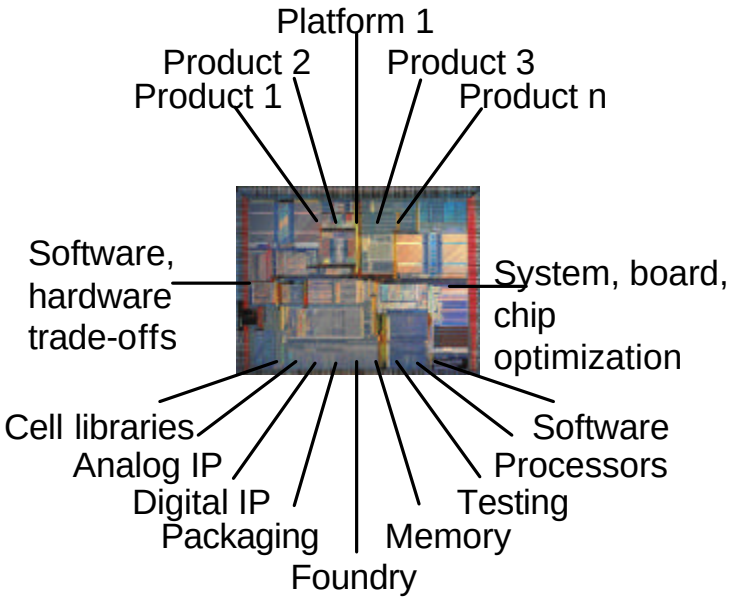
- Mid-90s
  - 6 months late → ~31% earnings loss
- Today
  - 3 months late = $500M loss

First-to-Market and First-to-Volume SOCs → Business Success
1st Silicon Success® critical

Dataquest 2002

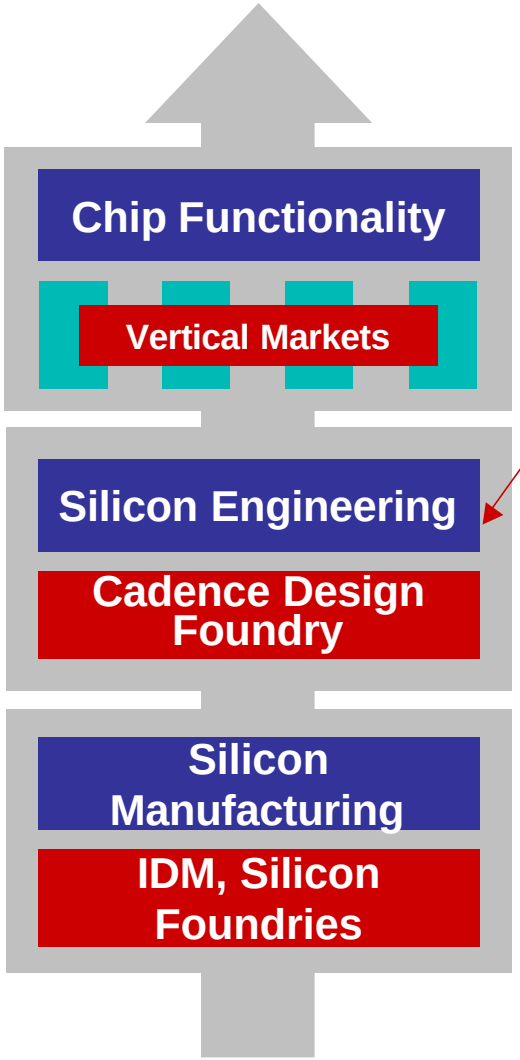
Design complexity intensifies challenge





- IC integration density and content
  - Integration (# transistors) ~30M – 300M
  - Die Size (sq. mm.) ~12x12 – ~22x22
  - Clock Rate (MHz) 200 - 900
  - Memory Instances (#) ~100 - 600
  - Analog Blocks (#) ~1 – 10
  - Routed Nets (#) ~8M - 20M+
- Functional design modes
  - Operational Modes (#) 1 – 13
- Package, board technology
  - Package Types Flip-chip BGA, EBGA
  - I/O Ckt. Types (#) ~1 – 10
  - I/Os (total #) ~2,000+
  - I/O Frequency 200 MHz – 3.125+ Gb/s
  - Power (W) ~5 – 25
  - Board Layers ~2 – 50
- Supply chain
  - IP Providers (#) 1 – 10
  - Supply chain Providers 3 – 5

Specialize and partner to build the product delivery value chain



- …to achieve First-to-Market and First-to-Volume with increasing design complexity
- Differentiated value

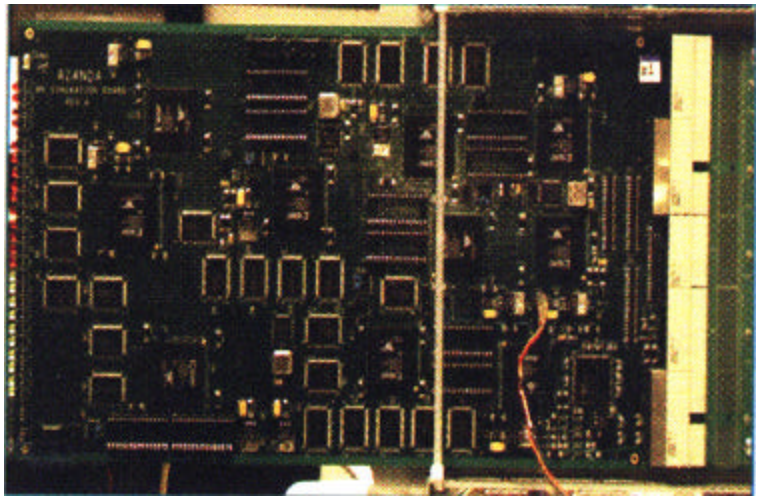
- Broad and deep Silicon Engineering expertise
  - Analog, IP, IC, package, board; DFT, DFM
- Design-proven methodology (mixed-signal)
- Design-proven technologies
- Design-proven IP (supply, integration)
- Supply chain management

- **"…We have reached the point where back-end physical design and verification takes far longer than front-end system, architecture and logic design!"**

Dr. H Samueli; Co-Chairman & CTO, Broadcom Corp.;
Invited Keynote Address; ISSCC, 2/99

Customers focus on architecture, logic design challenges

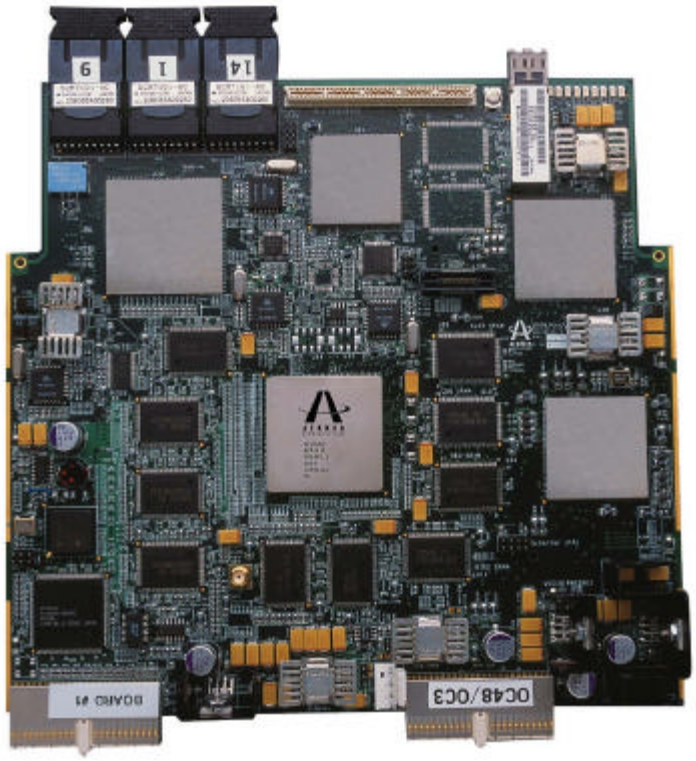
- Design verification
  - Custom FPGA-based system
- Accelerate system bring-up
  - RTL, apps. verified prior to silicon



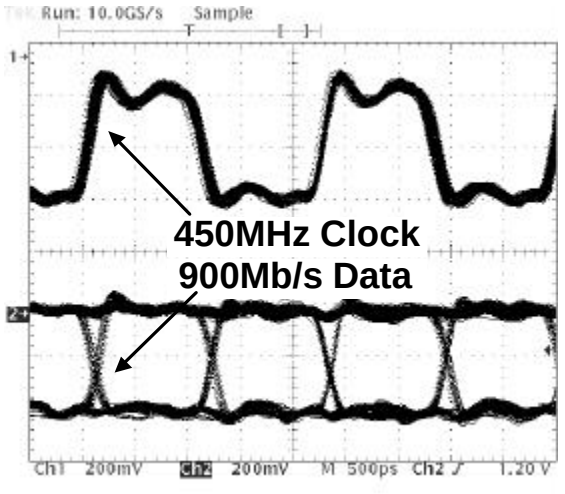
Azanda Network Devices, Inc. material used with permission

We focus on Silicon Engineering

- Azanda Network Devices Scimitar™ AZ61100
  - Industry-First Single-Chip,Full-Duplex, OC-48 Traffic Manager and ATM Segmentation and Reassembly SoC



- 1M simultanous traffic flows
- 5 Gb/s bandwidth
- 900 Mb/s data rate
- ~78M transistors
- 1,800+ I/Os



1st Silicon Success®

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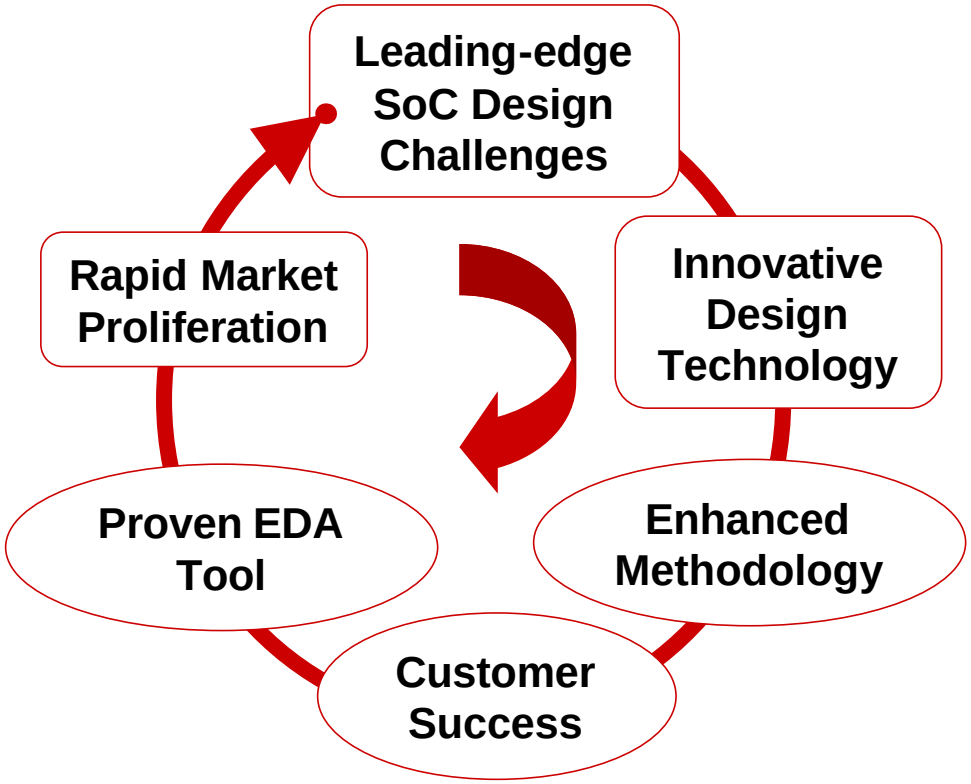
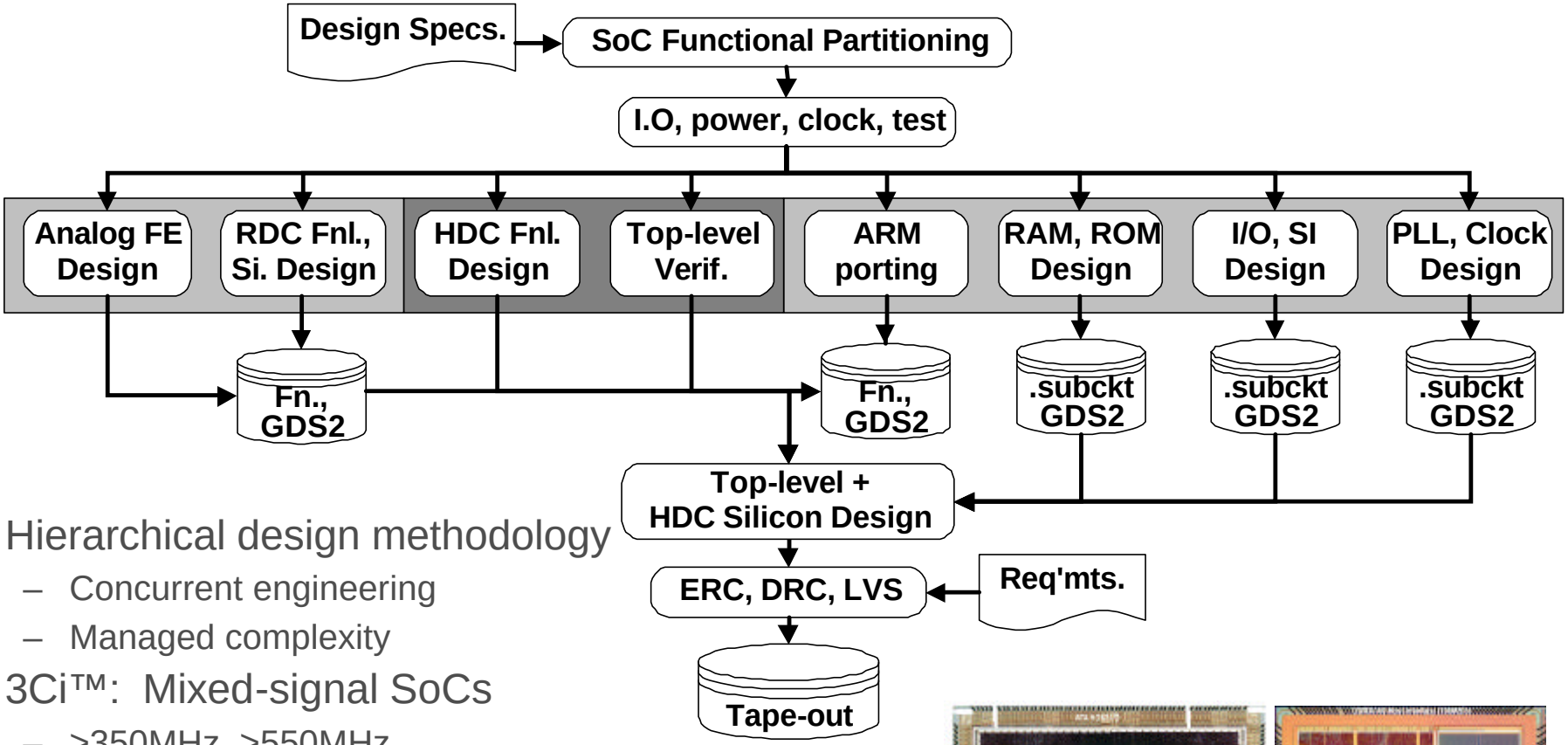
Leading by Design

- Accelerate / focus innovative design methodology, technology by creating leading-edge SoCs



- Silicon engineering
  - Architectural, functional design & verification
    - Unified verification
  - Electrical & physical design
    - Mixed-signal Soc design methodology
    - Hierarchical design
    - Wiring-centric design
    - Timing, clocking, power, SI
  - IP
    - Analog, digital IP development, reuse
    - Third-party IP integration
  - Technology Readiness
    - IC/package/board co-optimization
  - Supply chain

Top-level design methodology (example)



- Hierarchical design methodology
  - Concurrent engineering
  - Managed complexity
- 3Ci™: Mixed-signal SoCs
  - >350MHz, >550MHz
  - Same BER/SNR for VLSI, SoC
  - 1st Silicon Success®
  - EDN "Innovation of the Year"
  - IDC "Top Ten"
  - 1999ISSCC MP2.5

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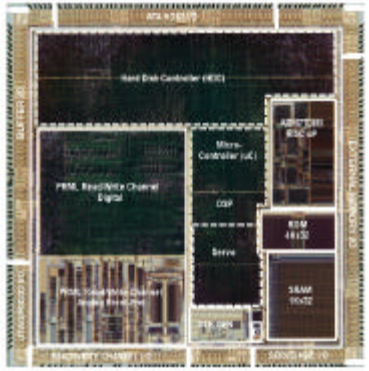
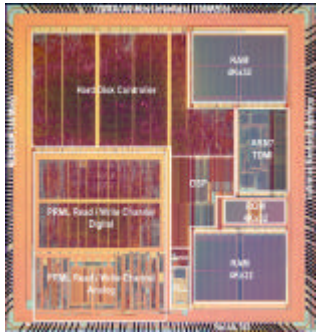
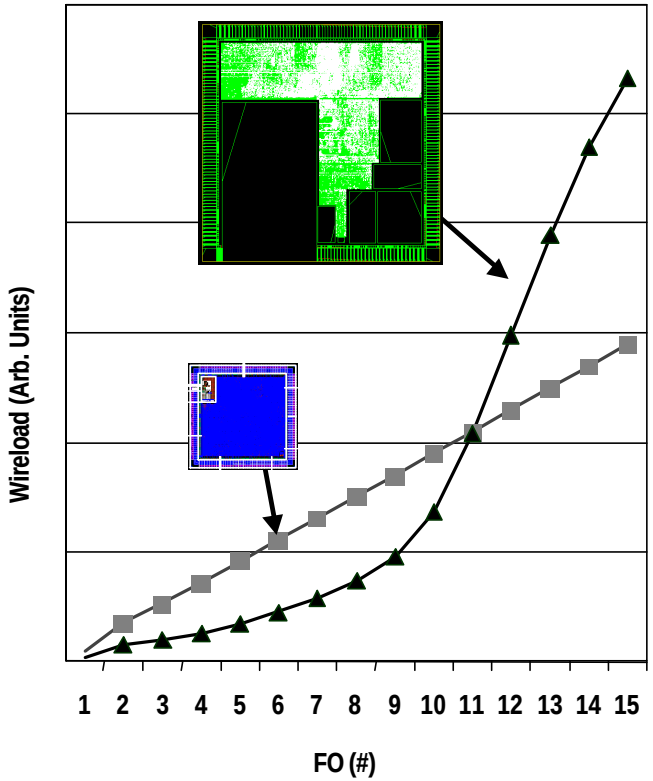
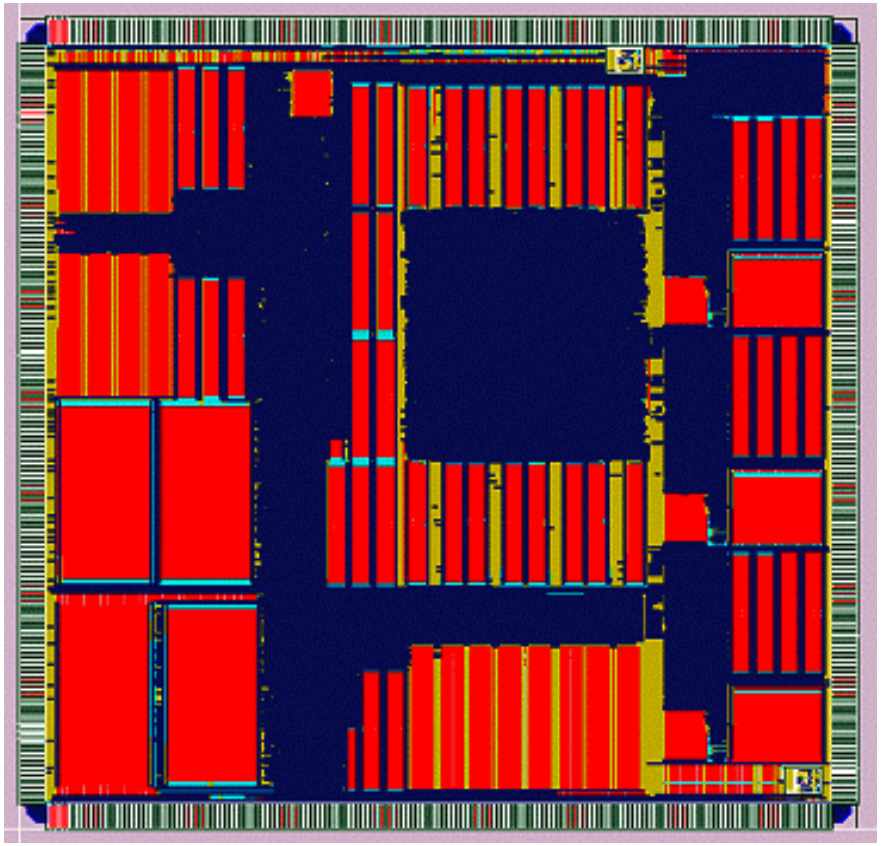




Cirrus Logic, Inc. 3Ci™ material used with permission

Wireload models → Physical synthesis

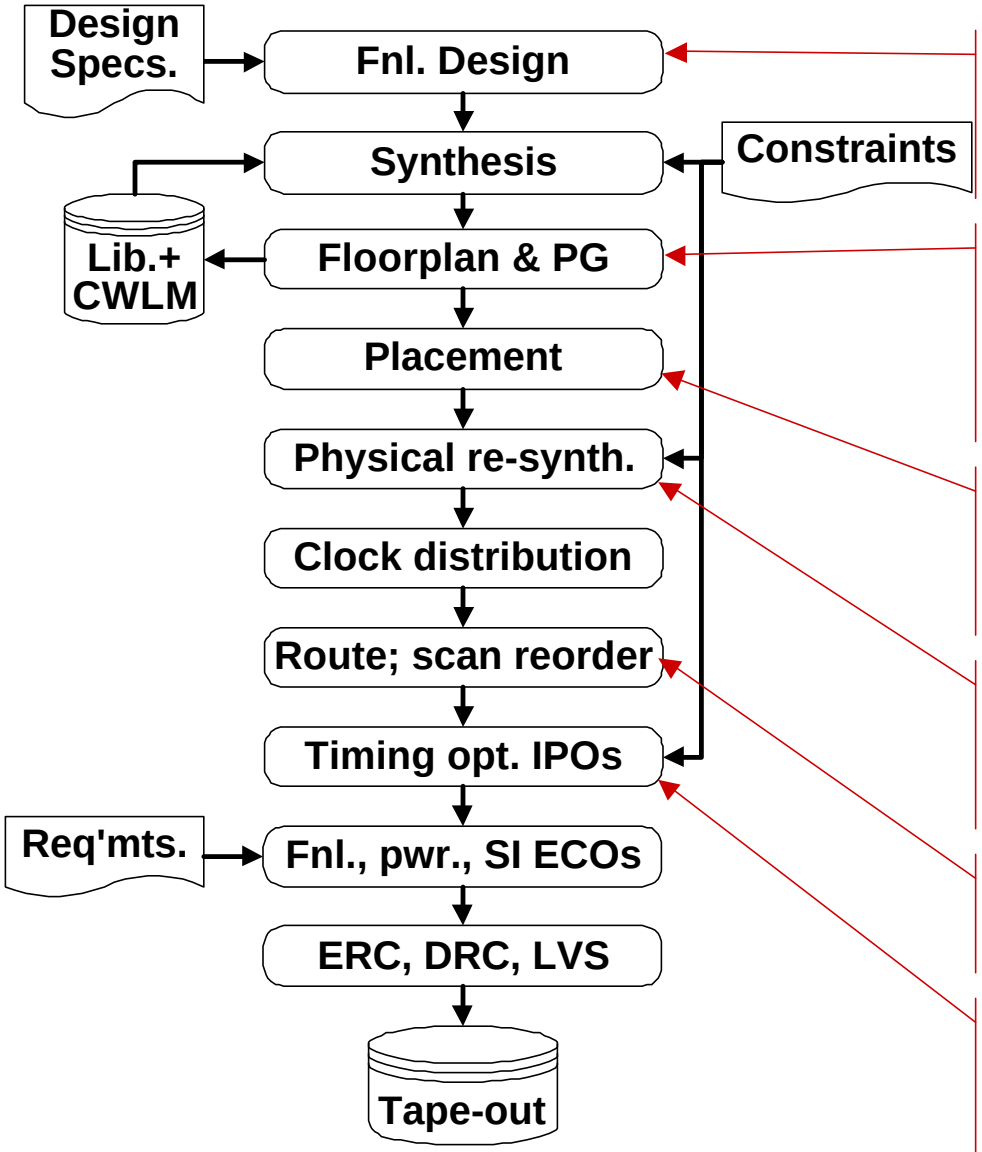




- 40% - 80% of core area memory-based
- Physical synthesis critical to timing closure

Material used with permission

Block-level design methodology (example)



- Architectural optimization (timing)
- Inter-group buses, bandwidth
- Clock, SI, test; validation

- Floorplanning and custom WLM
- Power distribution (Internal, I/O)
- I/O driver, pad ring design
- Board-level timing, SI

- Row definitions
- Placement of cells
- Congestion analysis

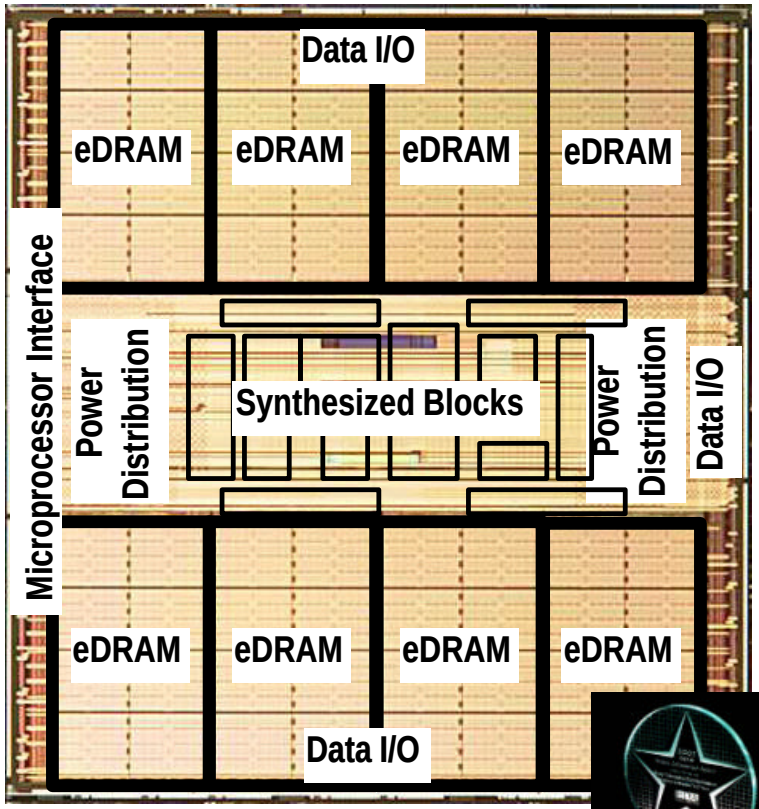
- Placement-based re-synthesis
- Noise management
- Clock distribution

- Full routing
- Scan stitching, re-ordering

- Full RC back-annotation
- Hierarchical timing, electrical and SI analysis and IPO/ECO

Sony Computer Entertainment GS®I-32

- Architectural design enhancements
  - 8x higher eDRAM vs. PS2 Rendering Processor (256 Mb)
  - eDRAM bandwidth = 48 GB/s (Buses >2K bits wide)
  - Rendering speed = 75M polygons/s



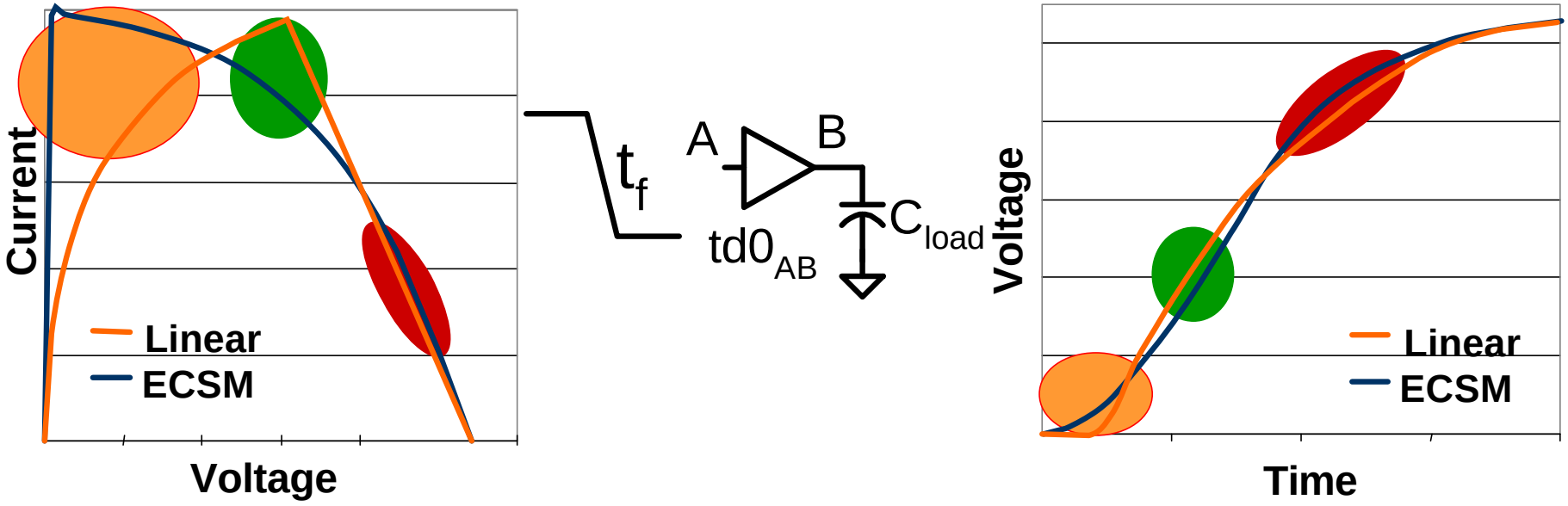
ISSCC2001 9.6

DAC2001 Gold Design Achievement

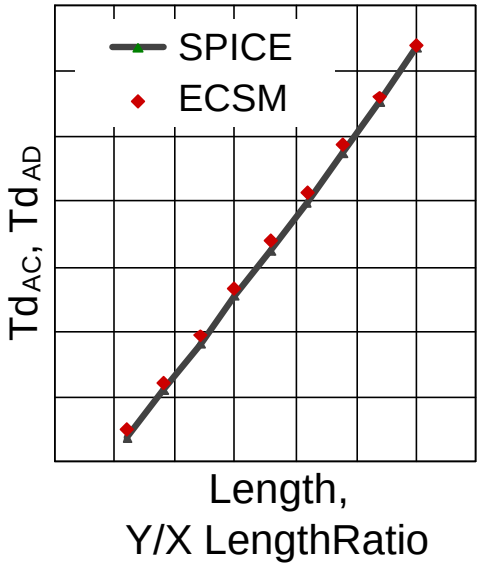
- "Gscube" renders 1.2G polygons/s
- Exceeds highest HDTV standard
  - 1920x1080, 60 fps progressive
- 280M + 7.5M transistors
- 21.7 x 21.3 mm^2
- >400K components
- >500K signal nets
  - >2K nets >10 mm. long
- 0.18 um, 6-metal eDRAM CMOS
- Netlist to tape-out = 10 weeks
- 1st Silicon Success®

Accurate numerical model for circuit behavior

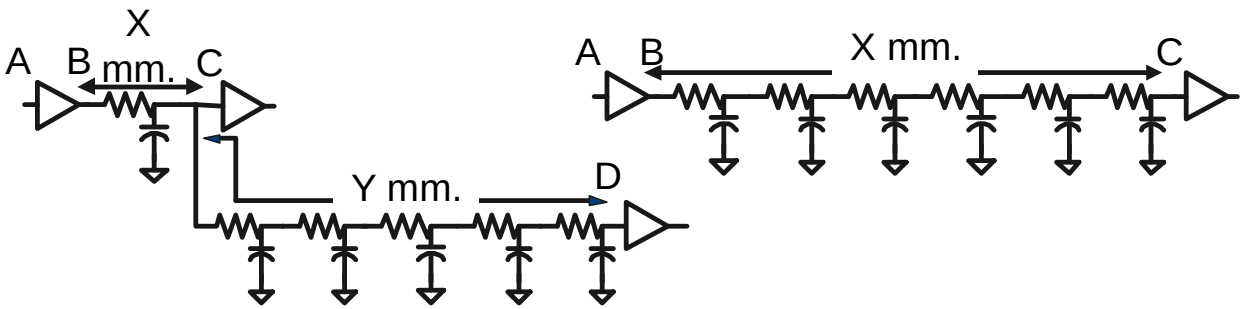
- Circuit behavior nonlinear
- Conventional linear model → >5% error in delay calculation
- Nonlinear model → accurate di/dt
- Instance-based, net-by-net delay calculation

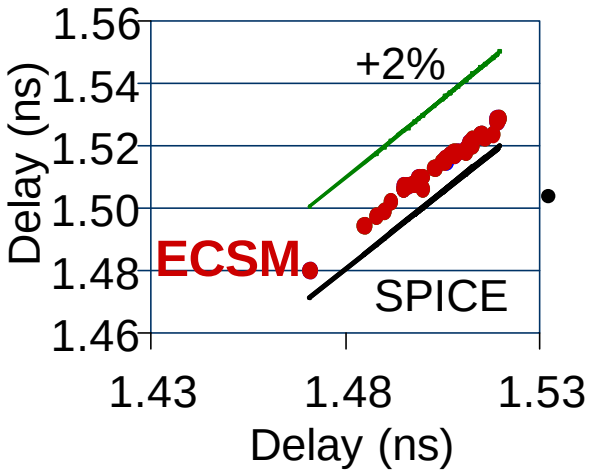


Accurate delay calculation



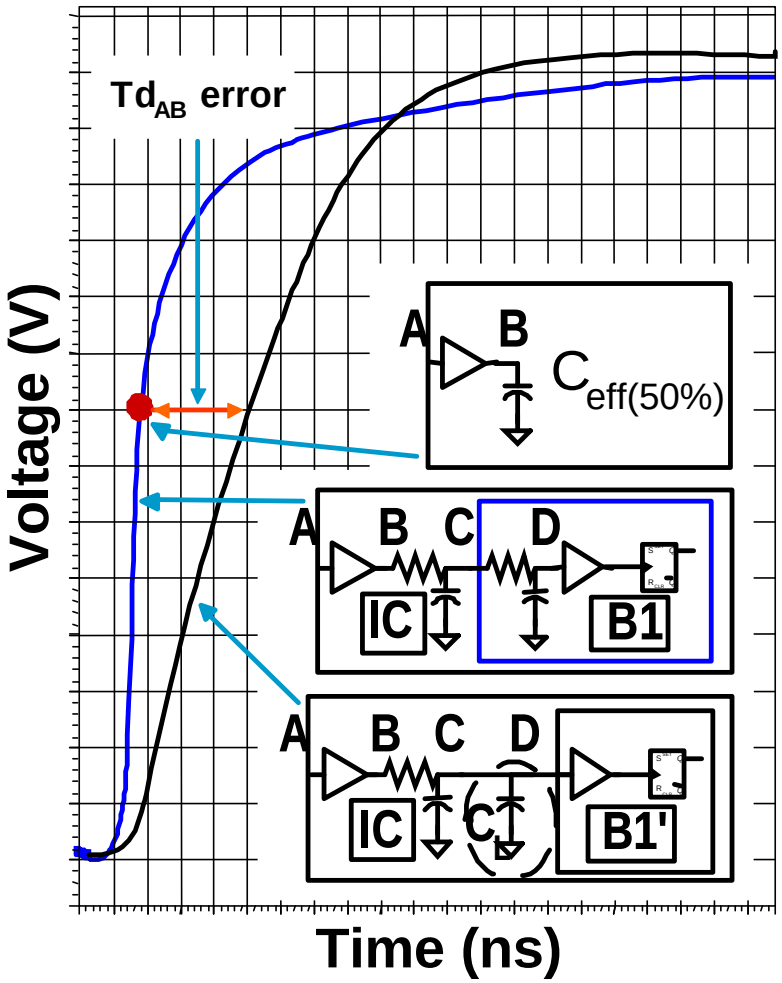
- Net lengths from ~100um to multiple mm.
  - Modeling RC effects critical
- Short / long net segments ratios varied
- Complex RC topologies
- ~2% correlation to SPICE





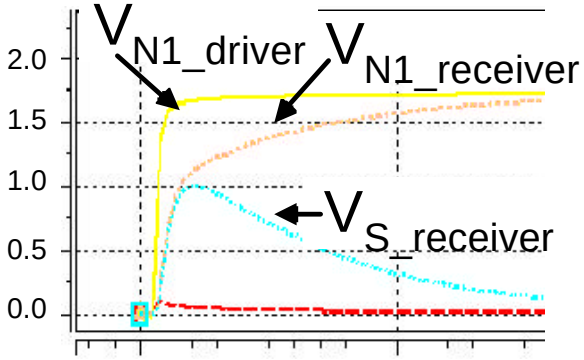
- Improved accuracy → Faster to market, volume
  - Design IP: 260K placeable objects; 187K nets
  - 10% → 5% accuracy: 1,512 of 2,807 STA paths OK

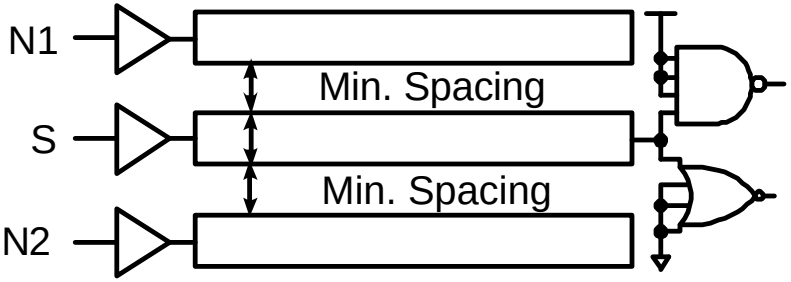
Accurate fully-hierarchical timing

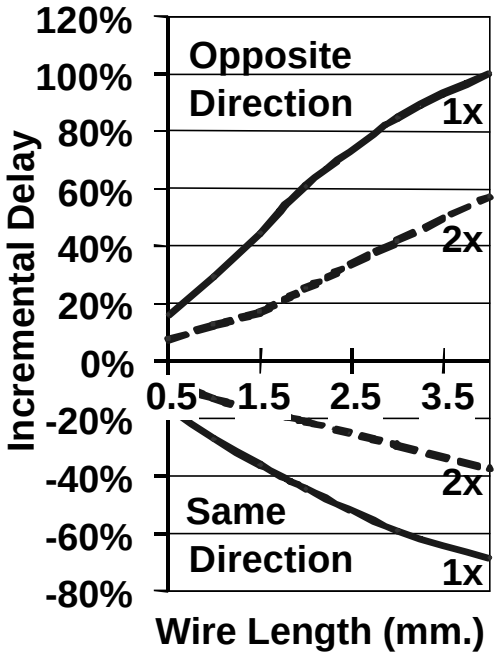


- Signal paths traverse hierarchy
  - Block inputs with ~0 – 2 mm. metal → RC delay
- Model block boundary pin input RC as C_L
- C_L over-estimates effective capacitance when RC significant
  - Driver delay over-estimated
- Design issues
  - Latent hold time defects
  - Signal nets overdriven for setup margin
- Delay calculation with $C_{eff(50\%)}$ fits RC waveform at threshold

Signal integrity

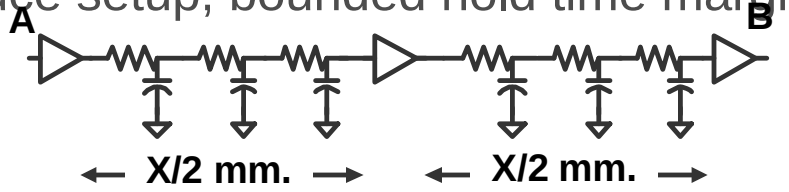






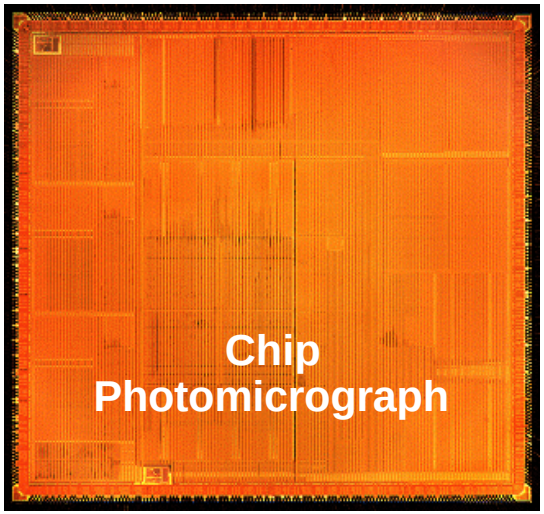
- All 3 signals switch concurrently
- 1x, 2x: 1-grid, 2-grid spacing

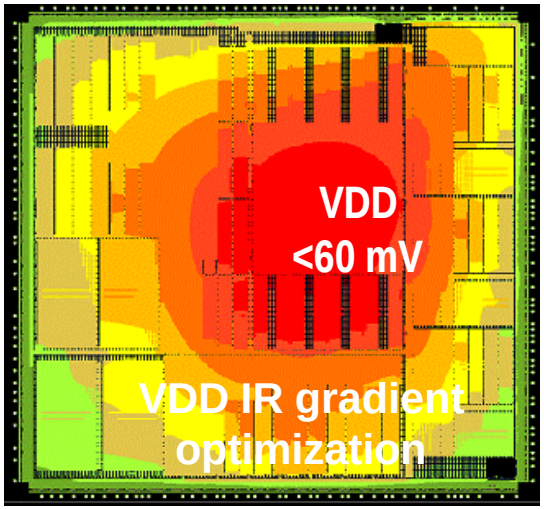
- Crosstalk-induced timing uncertainty
  - Effect proportional to victim & aggressor strengths, timing overlap, coupled length & spacing, voltage switching direction, current switching direction, etc.
- Insert buffers ~1.5 - 2.5 mm.
  - Bound timing uncertainty; reduce total delay
- Address impact in Static Timing Analysis
  - Reduce setup, bounded hold time margin

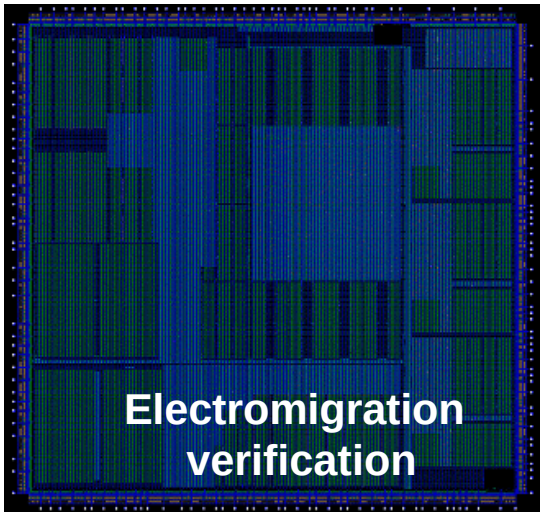


Power / current distribution

- IC power distribution ~1-2 full metal layers; >5-15+ A current





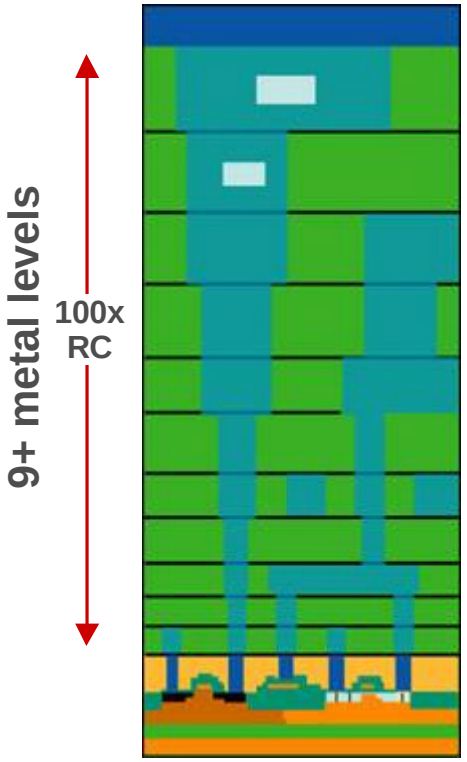


- Design needs
  - Manage static, dynamic draw
  - Ensure valid timing across design envelope
  - Ensure electromigration immunity
  - Manage noise immunity, simultaneously-switched outputs, inputs

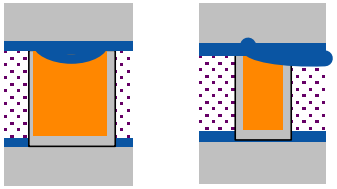
Material used with permission.

Wiring is central to nanometer SoC design

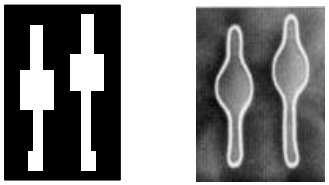
- Wiring dominates electrical closure
  - Differing properties across M1-8
- Wires dominate manufacturability
  - RLC variation; vias
- Wiring interacts
  - Timing, clocking, crosstalk, signal integrity, power inter-related

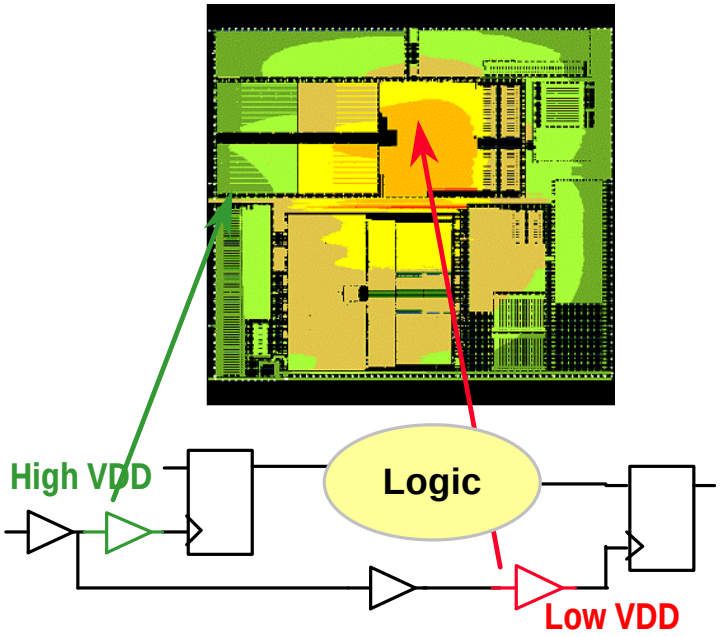


Copper distortions



Subwavelength distortions

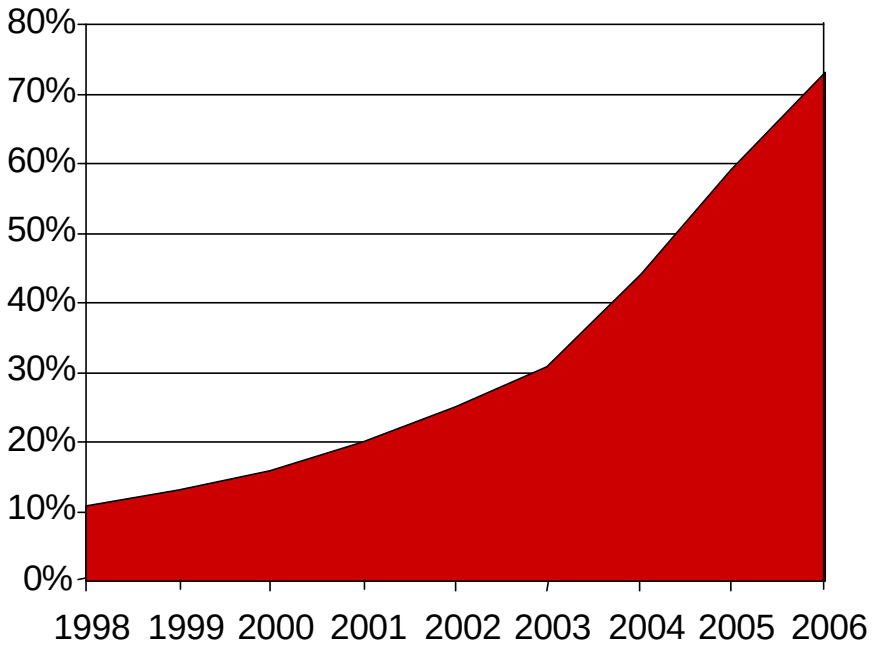




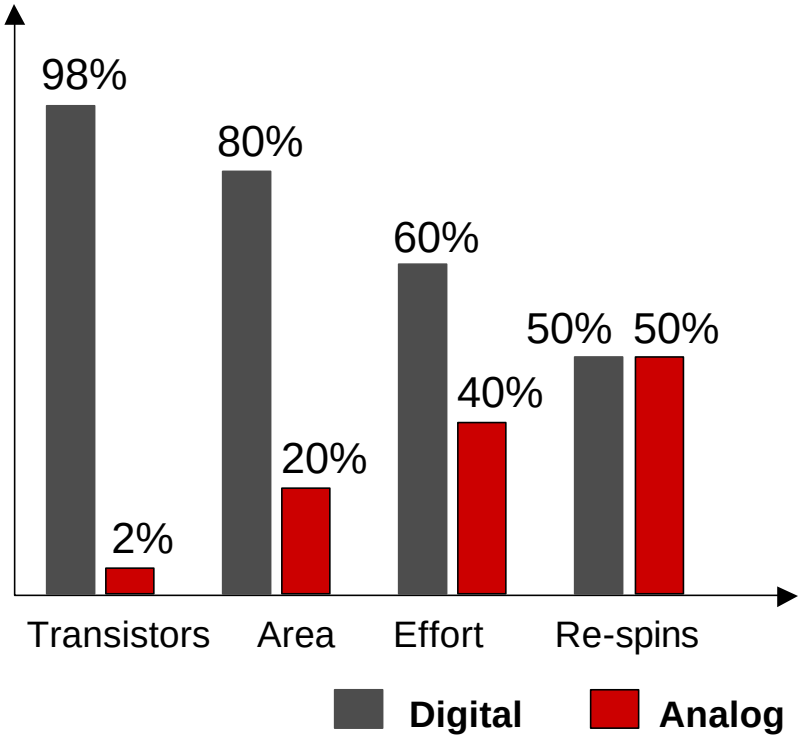
Delta VDD → Hold time failure

Most SoCs are mixed-signal

SoCs with Digital and Analog



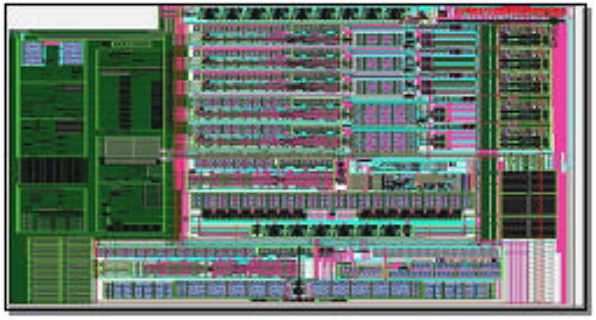
Analog's Impact on Overall Design



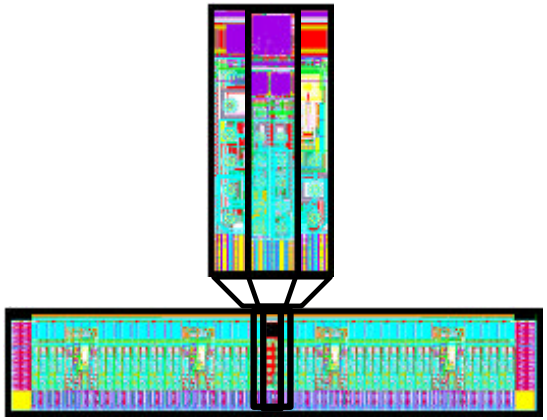
Successful analog integration critical to 1st Silicon Success®

Proven std. CMOS analog IP is essential

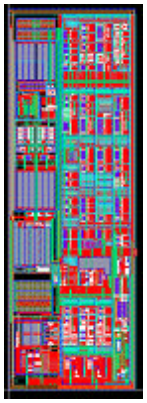
Critical building blocks for SoCs (datacom, RF, consumer)



8b,10b 10-100MHz ADCs
130nm

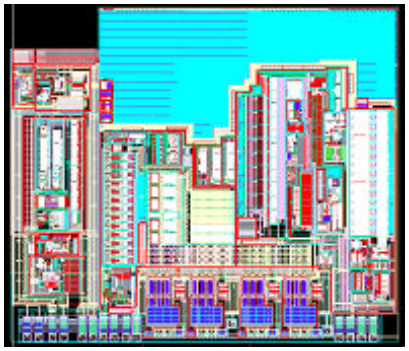


1.25, 2.5, 3.125G SerDes
130nm

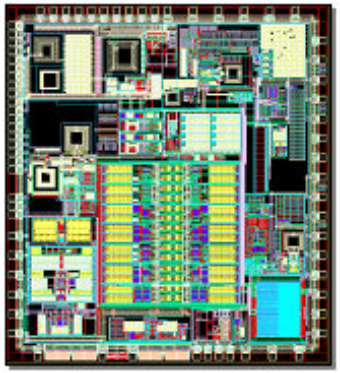


Low Jitter Ring/LC PLLs
130nm

USB 2.0
PHYs



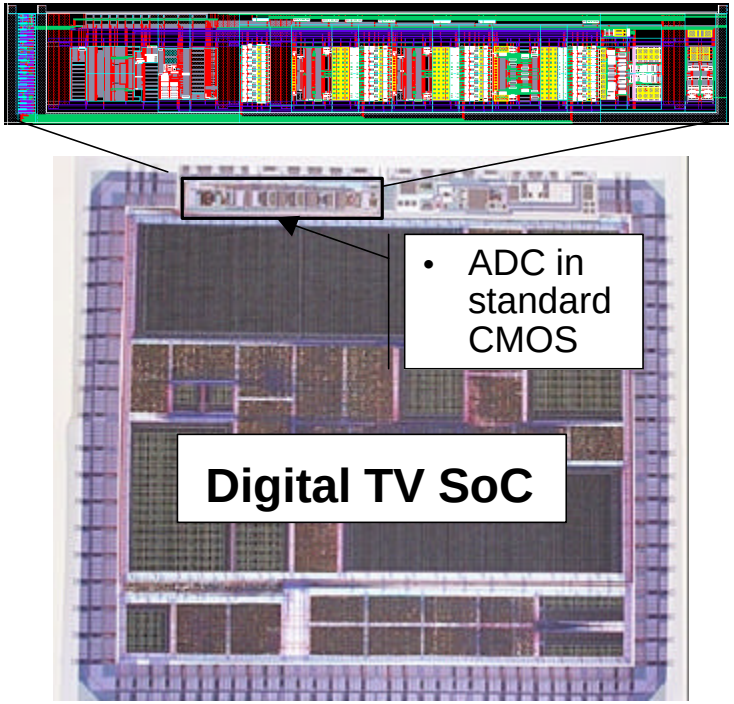
10/100BT Ethernet
PHYs

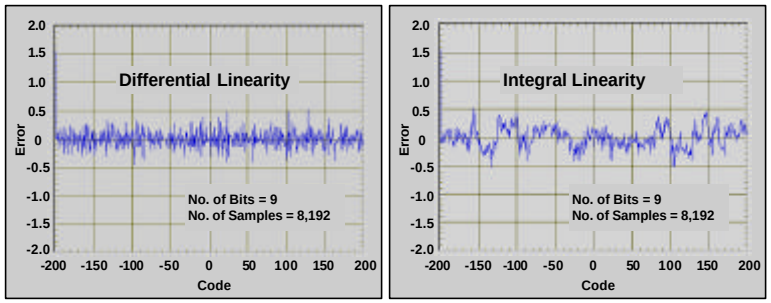


2.4GHz RF
XCVRs

Mixed-signal SoCs

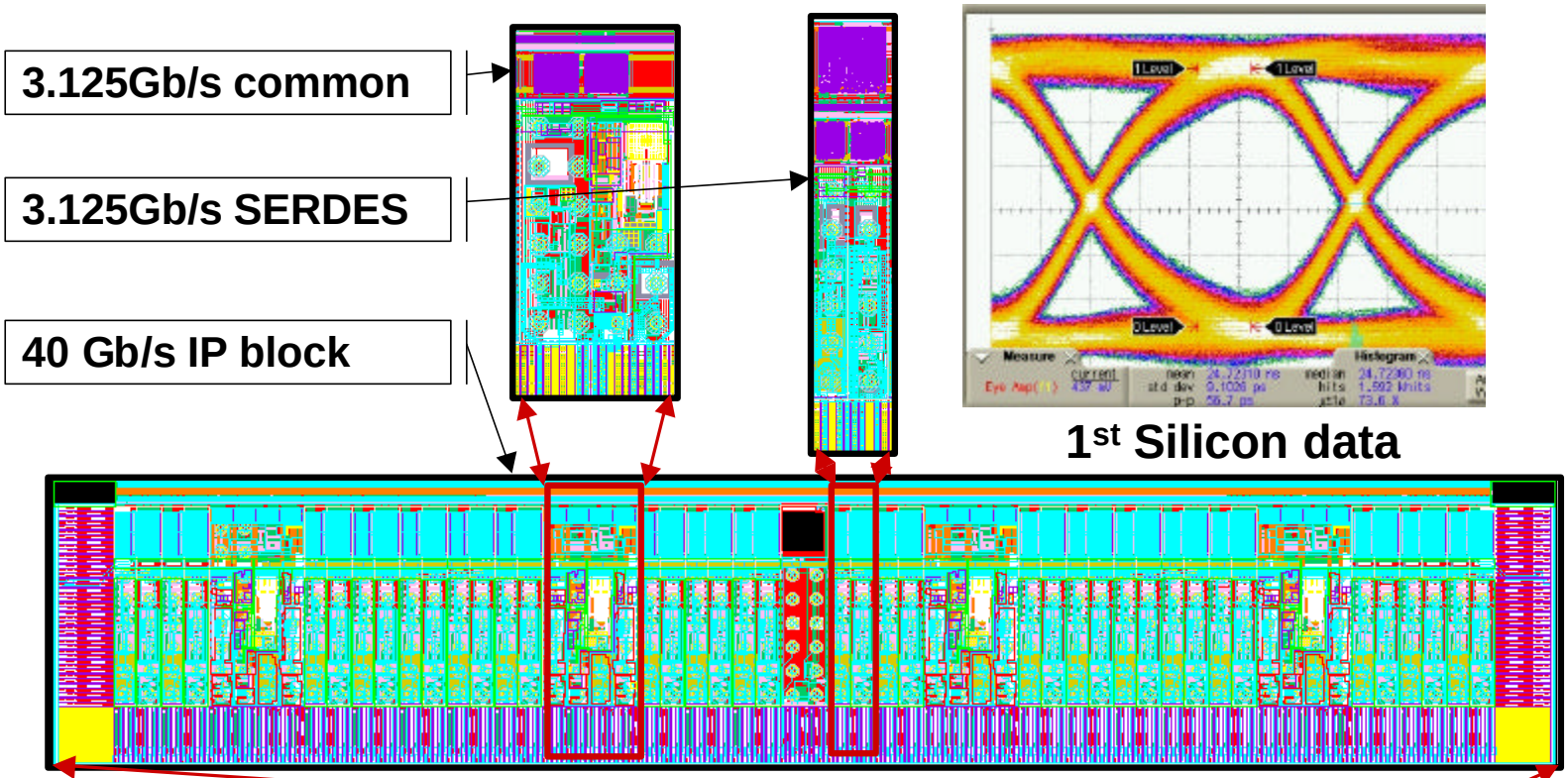
Analog IP + SoC design experience is critical





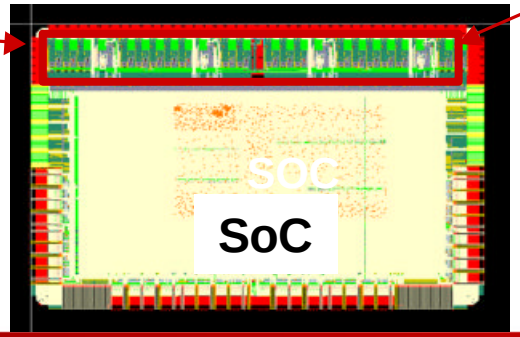
- Electrical / physical design
  - Analog / digital isolation
  - Quality of RLCs in std. CMOS
  - Metal fill effects on analog
  - Clk jitter impacts on SNR, BER
  - Analog spice/package models
- Board/package/chip co-design
  - Signal, power distri., pin locations
  - Lead inductance/mutual coupling
  - Low R and C I/O ESD
- Verification
  - Analog and digital compatibility
- Test requirements
  - Tester, measurements, test time

Industry-First 40Gb/s SoC uses versatile Cadence SerDes IP



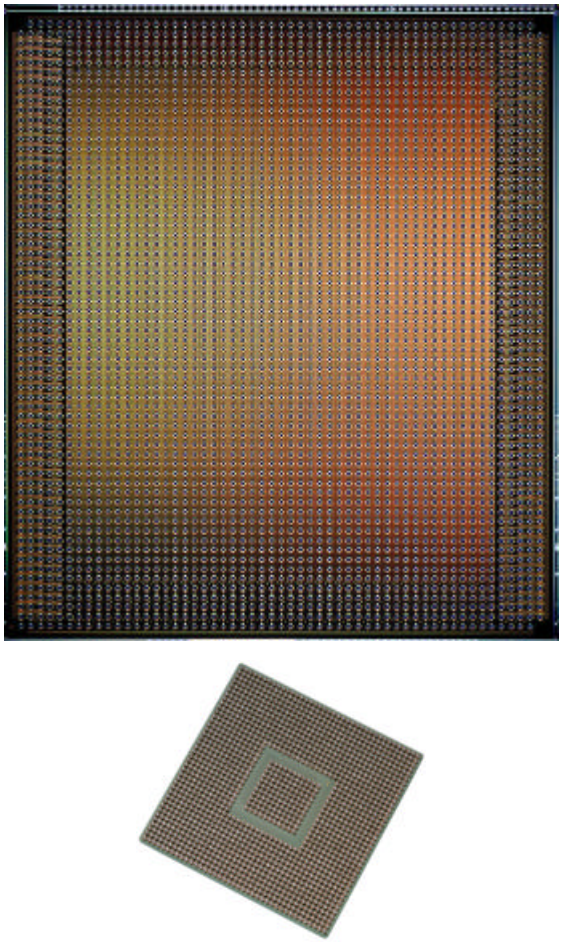
1st Silicon data

- **TSMC 0.13um standard CMOS logic hard IP core**
  - Compatible rates (GHz): .155, .622, 1.06, 1.244,.1.25, 1.56, 2.125, 2.488, 2.5, 2.75, 3.1, 3.25
  - Compatible standards: Infiniband, XAUI, Rapid IO, SXI5, Fiber Channel, Gigabit Ethernet, SONET VSR, OC3, OC12 ,OC48



Material used with permission

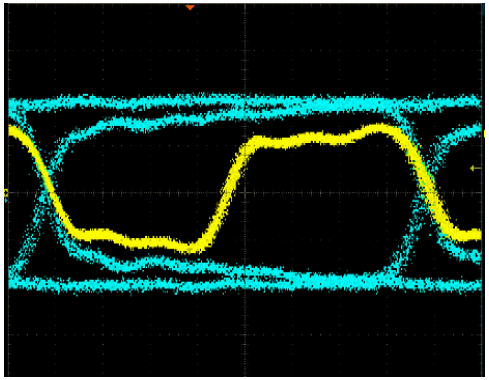
Industry-first OC768 framer-mapper processor electrical design



- 0.15-micron, 8 metal
- Over 50 clock domains
  - 100MHz → ~700MHz
- 1,413 bumps flip-chip BGA
- 560 signals @ 622 MHz LVDS
- Some design challenges
  - Clock distribution
  - Timing
  - RDL design
  - Power distribution
  - Signal integrity
  - Full signal transmission path

Infineon Technologies, Inc. material used with permission

Industry-first OC768 framer-mapper processor design results

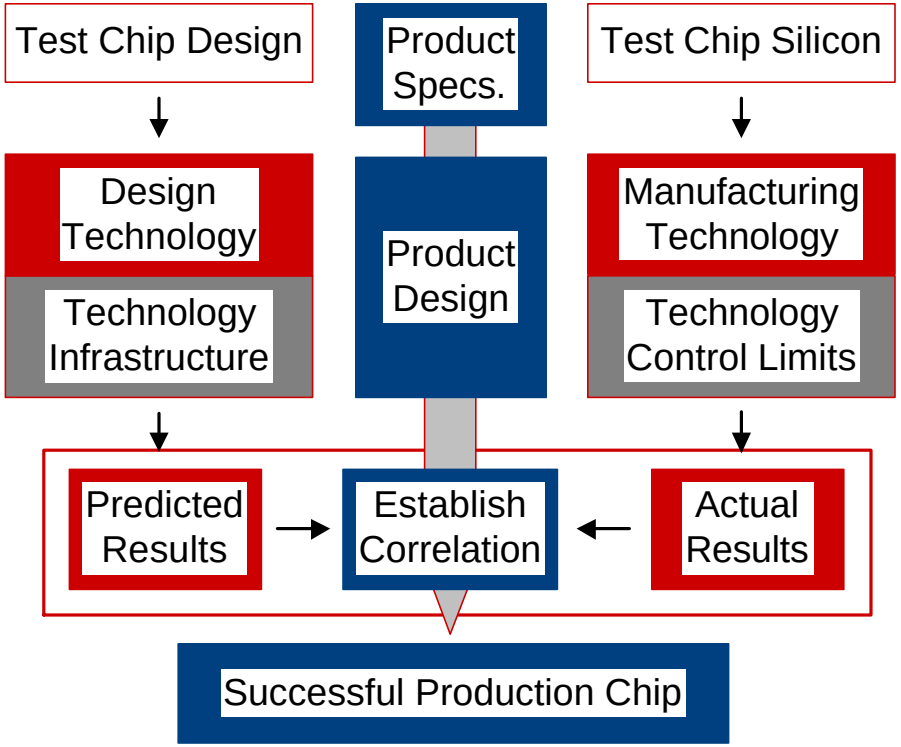


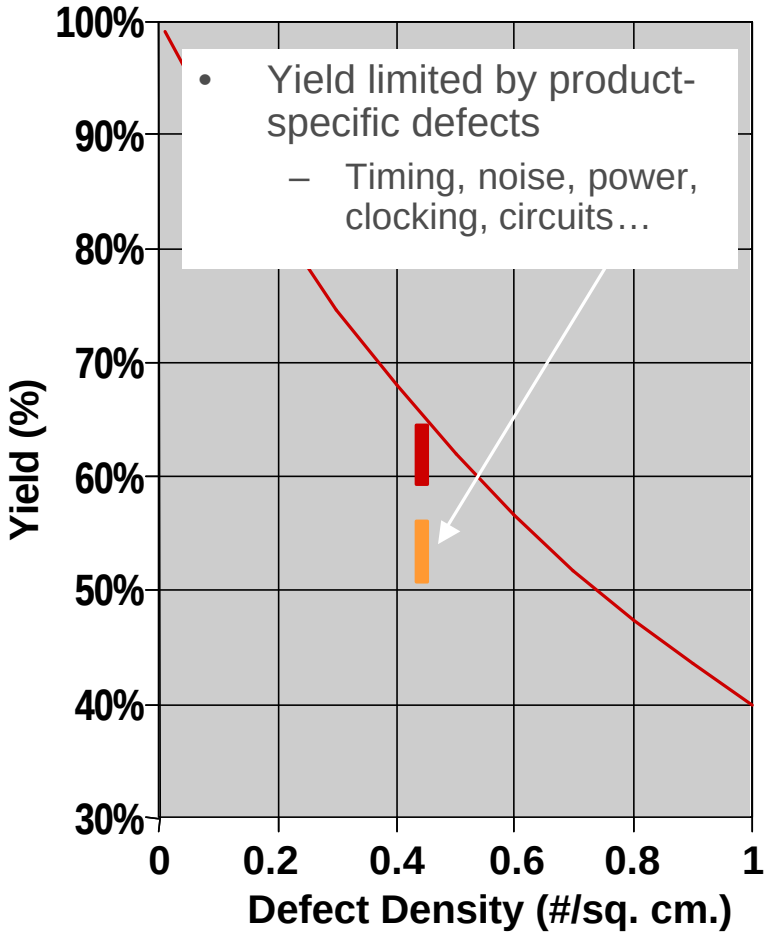
- First silicon success
- 160 Gb/s throughput

Infineon Technologies, Inc. material used with permission.

Technology Readiness

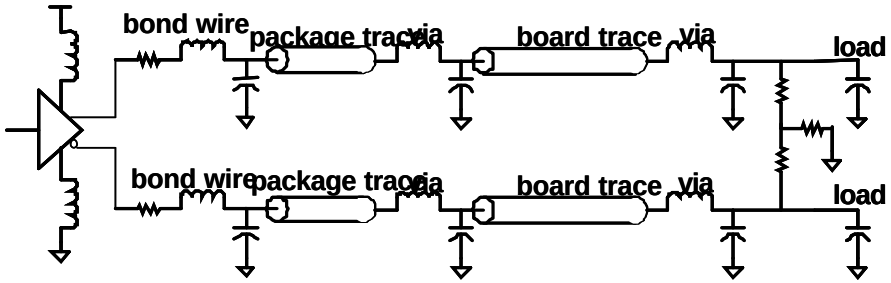
On-time delivery of new products with new technology



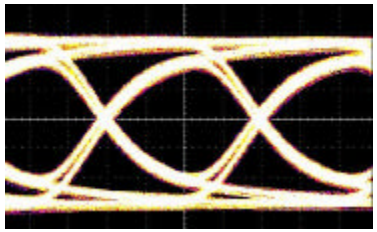


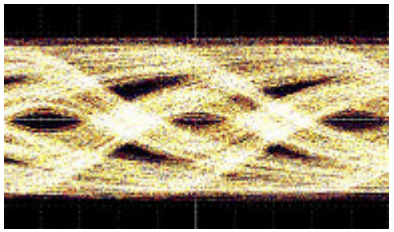
- Validated, robust design margins
  - Validate design space across manufacturing boundary limits

Analog, digital signal transport



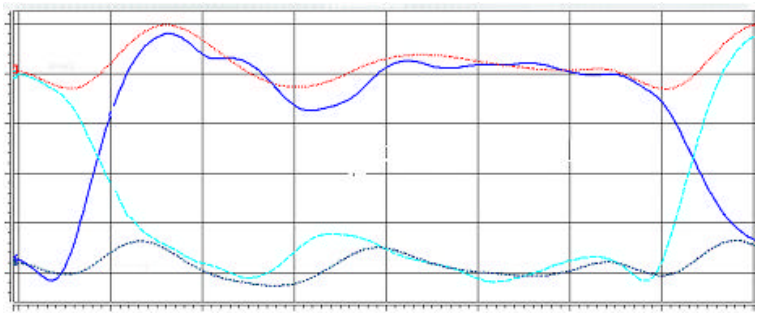
No Pre-emphasis



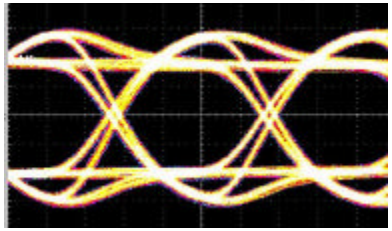


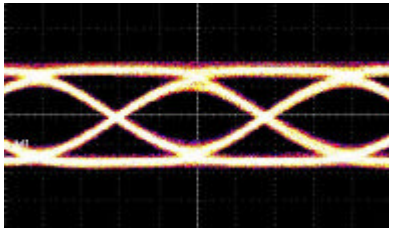
Near end

Far end- 34” Tyco Board



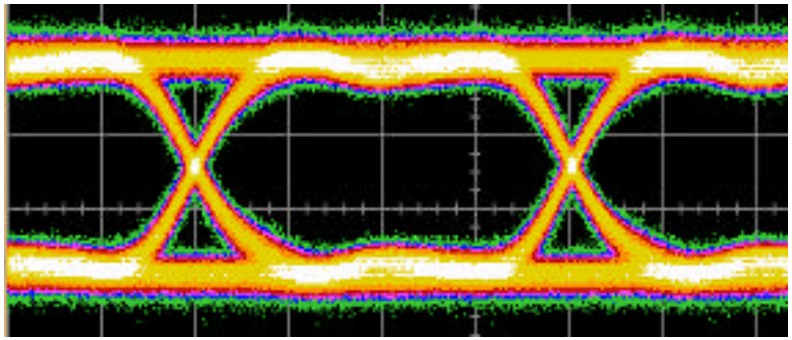
With Pre-emphasis

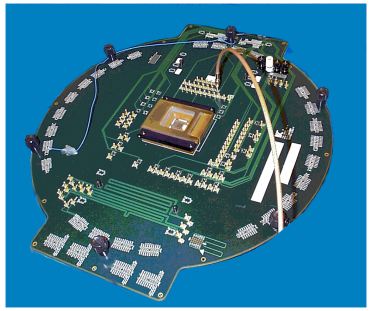


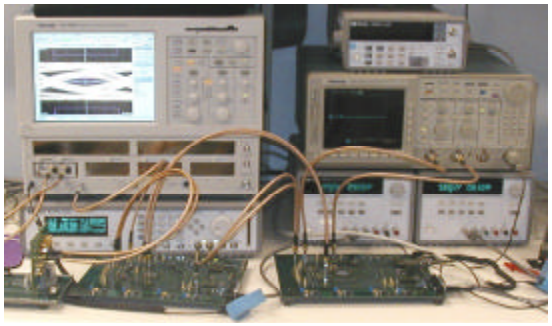


Near end

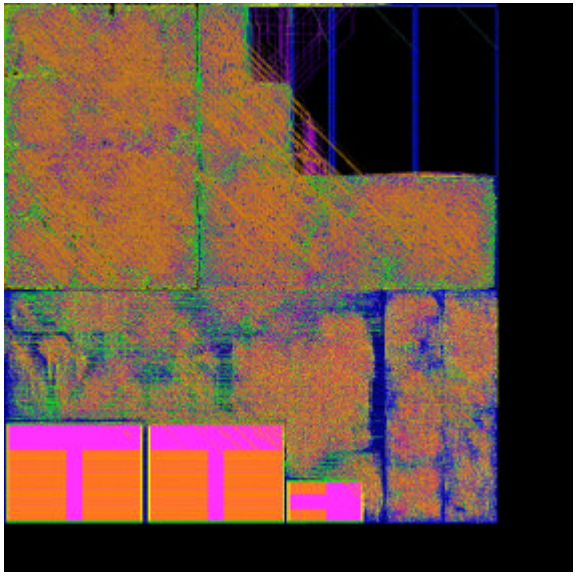
Far end- 34” Tyco Board

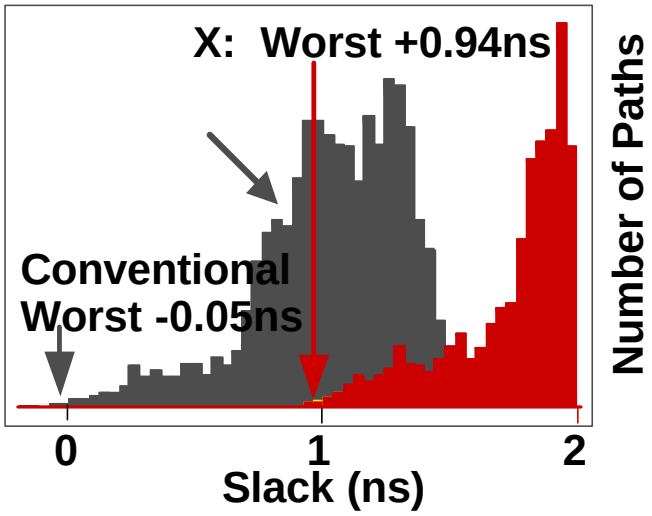






X-architecture based microprocessor design





- Concurrent improvements to all three metrics
  - 19.8% path delay reduction and 10% area reduction
  - Performance and power and cost (area, # vias)

Tile	Reduction	
	Wire	Via
A	25 %	37 %
B	13 %	28 %
C	21 %	35 %
D	22 %	32 %

Igarashi, et. al., "A Diagonal Interconnect Architecture and its Application to RISC Core Design," 2002 International Solid State Circuits Conference, Feb. 2002. Material used with permission.

Design partnerships critical to success

- Rapid growth in SoC market
  - $23B in 2002 to $53B in 2006; 59% → 80% SoCs
- Design complexity growing exponentially on many dimensions: Conventional methods do not scale
- Leading-by-Design accelerates / focuses SoC design
  - Mixed-signal design methodology, fully-hierarchical design, physical synthesis, nonlinear delay calculation, power distribution, signal integrity, transmission line effects, analog IP
- Design partnerships critical to success
  - Specialize, innovate and partner to build the product delivery value chain
- First-to-Market and First-to-Volume drives business success
  - First silicon success critical