Challenges in A/D Design and Practical Understanding of A/D Specifications

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Topics:

I. Examples of A/D systems and specifications

II. Quantization and SNR

III. THD and SFDR

IV. ENOB and power estimations

V. Practical limitations

VI. Systems and specifications revisited

VII. Summary

Basic Rule: “Ask questions and challenge opinions !”

I. Examples of A/D systems and specifications

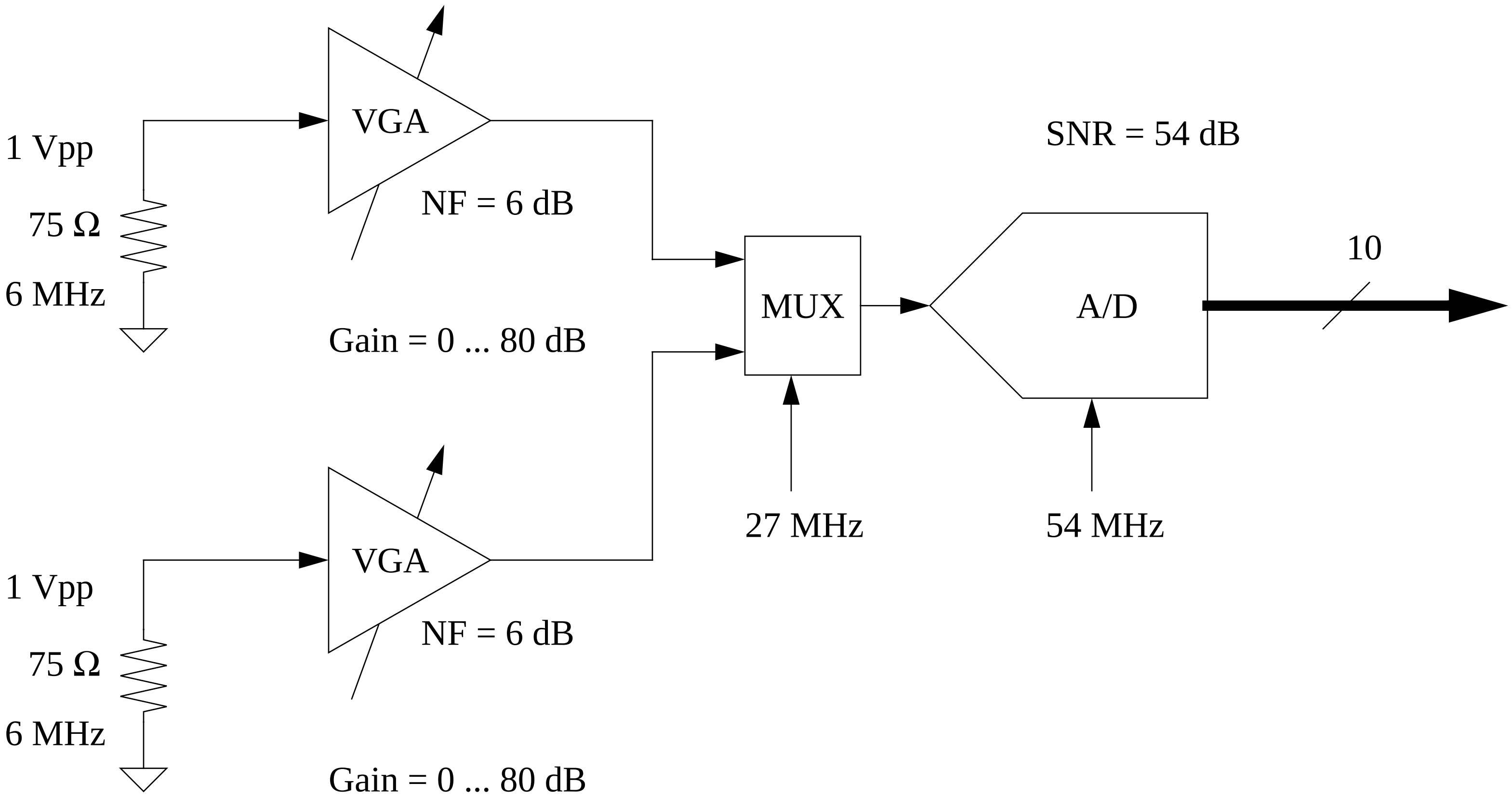
I.1 10-bit A/D specifications:

- Resolution N = 10 bit
- Signal-to-noise ratio SNR = 60 dB
- Total harmonic distortion THD = -62.5 dB
- Maximum differential non-linearity DNL = +/- 0.5 LSB
- Maximum integral non-linearity INL = +/- 1 LSB
- Input signal frequency Fin = 200 MHz
- Sampling rate Fs = 50 MS/s (undersampling)

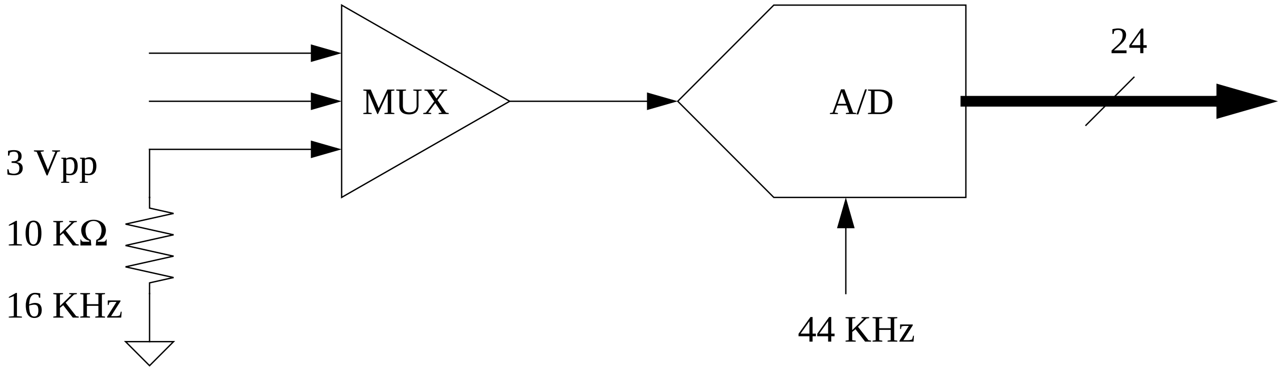
I.2 8-bit A/D specifications:

- Resolution N = 8 bit
- Signal-to-noise ratio SNR = 43 dB
- Spurious free dynamic range SFDR = 72 dB
- Maximum differential non-linearity DNL = +/- 0.5 LSB
- Maximum integral non-linearity INL = +/- 1 LSB
- Input signal frequency Fin = 5 MHz
- Sampling rate Fs = 50 MS/s

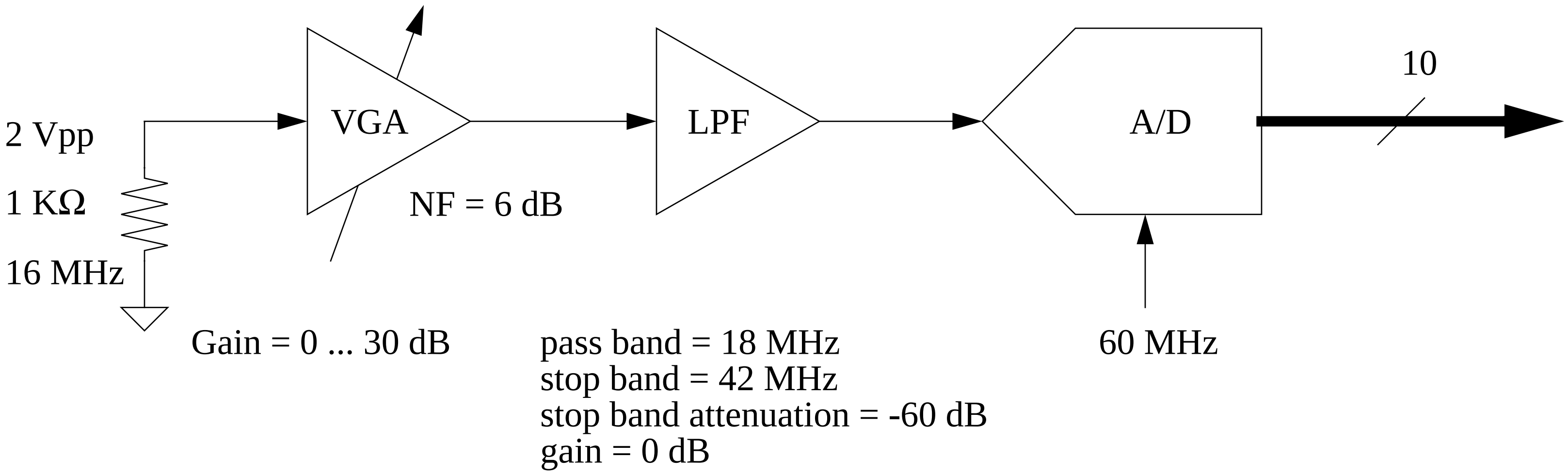
I.3 Video decoder system



I.4 Audio system



I.5 Receiver IF/baseband

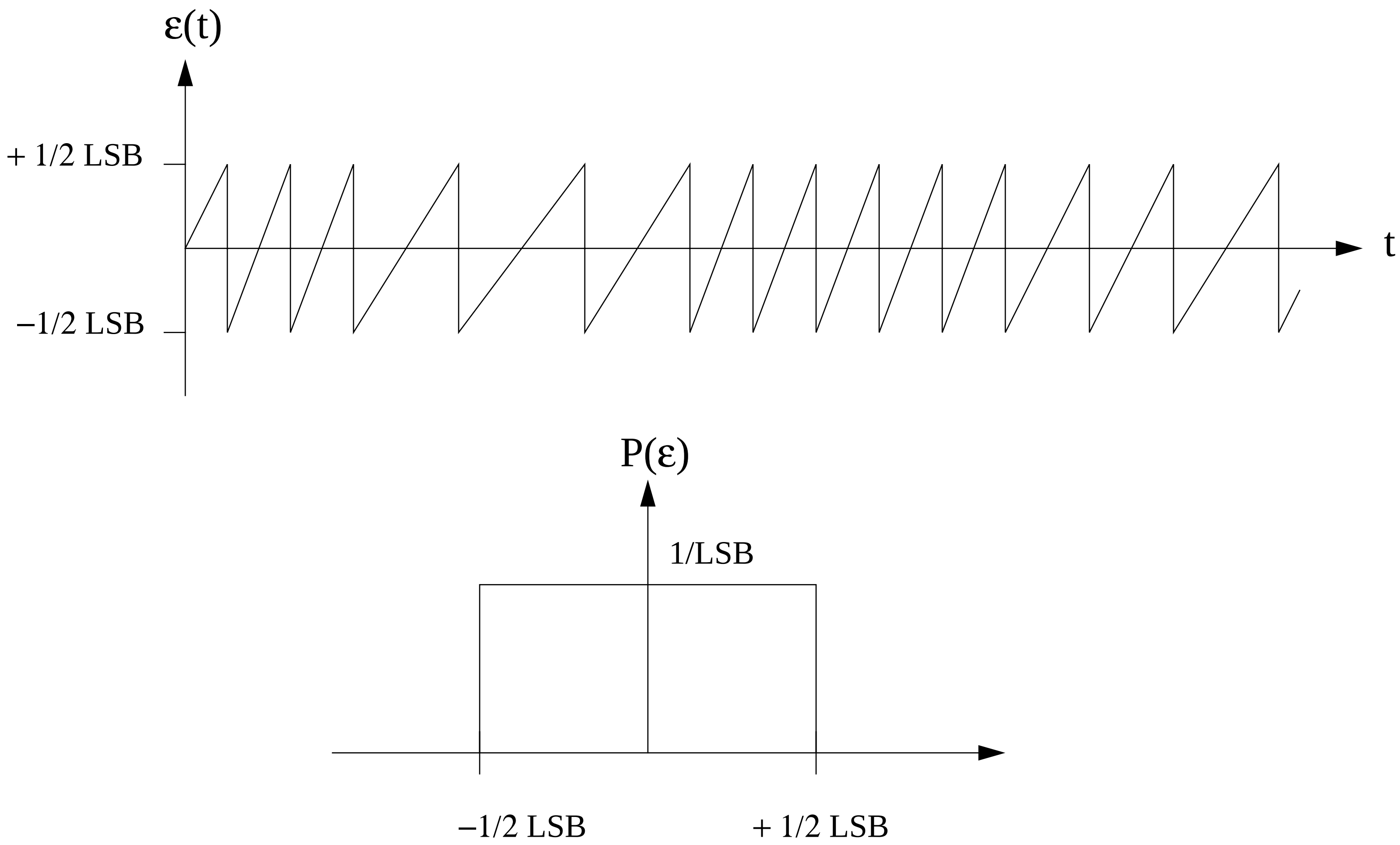


II. Quantization and SNR

Noise contributors:

- Quantization
- Circuit noise: - thermal
  - 1/f
  - pick-up noise (digital/substrate etc.)
- Clock jitter

II.1 Ideal quantization



Ideal Quantization (cont'd)

Quantization error power

$$Pq = \int_{-\frac{1}{2}LSB}^{\frac{1}{2}LSB} P(x) \cdot x^2 dx = \frac{LSB^2}{12} \qquad (1)$$

Signal power

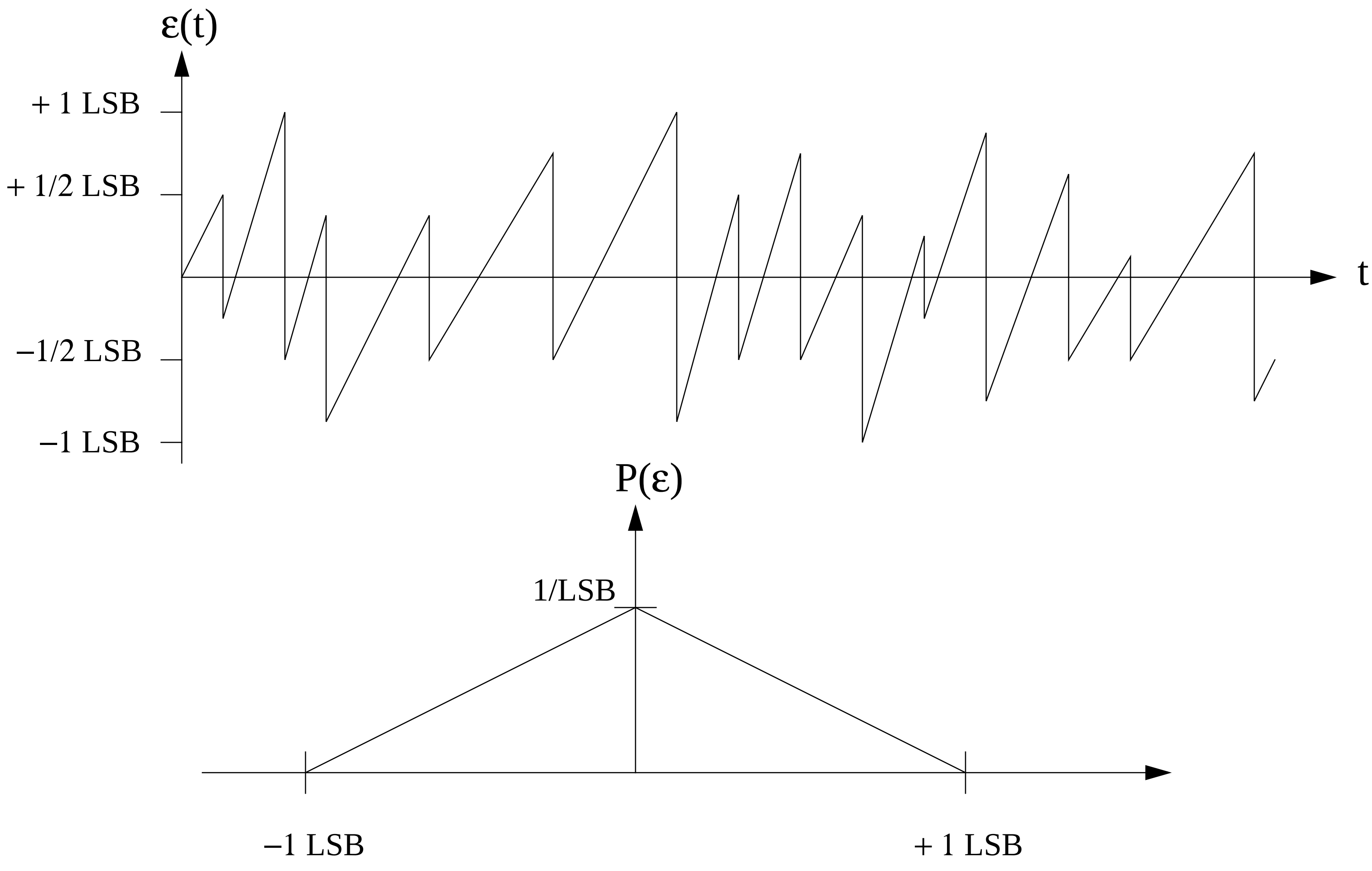
$$Ps = \frac{(2^{N-1})^2 \cdot LSB^2}{2} \qquad (2)$$

Signal-to-noise ratio

$$SNR = \frac{Ps}{Pq} = 10 \cdot \log 10\left(\frac{3}{2} \cdot 2^{2N}\right) = 6.02 \cdot N + 1.76 \;\; dB \qquad (3)$$

II.2 Quantization with DNL

- assume DNL max = +/- 1/2 LSB



Quantization with DNL (cont'd)

Quantization error power

$$Pq = \int_{-1LSB}^{1LSB} P(x) \cdot x^2 dx = \frac{LSB^2}{6} \tag{4}$$

Signal-to-noise ratio

$$SNR = \frac{Ps}{Pq} = 10 \cdot \log 10\left(\frac{3}{4} \cdot 2^{2N}\right) = 6.02 \cdot N - 1.25 \quad dB \tag{5}$$

SNR with thermal noise

$$SNR = \frac{Ps}{Pq + Pn} \tag{6}$$

if

$$Pn \approx Pq \tag{7}$$

$$SNR = \frac{Ps}{Pq} = 10 \cdot \log 10\left(\frac{3}{8} \cdot 2^{2N}\right) = 6.02 \cdot N - 4.27 \quad dB \tag{8}$$

III. THD and SFDR

Ideal quantization power

$$Pq = \frac{LSB^2}{12} \qquad (9)$$

- energy distributed at signal harmonics (aliased back in 0 to Fs/2 interval)
- maximum number of harmonics ~ $\pi * 2^N$
  (derived from max. amplitude and max. slew rate)

Min. power per harmonic

$$Ph = \frac{Pq}{\pi \cdot 2^N} = \frac{LSB^2}{12 \cdot \pi \cdot 2^N} \qquad (10)$$

Ideal SFDR

$$SFDR = \frac{Ps}{Ph} = 10 \cdot \log 10\left(\frac{12 \cdot \pi}{8} \cdot 2^{3N}\right) = 9.03 \cdot N + 6 \ \ dB \qquad (11)$$

Realistic SFDR from ideal quantization only

$$SFDR = 9.03 \cdot N \ \ dB \qquad (12)$$

IV. ENOB and power estimation

- signal to noise plus distortion ratio

$$SNDR = \frac{Ps}{Pq + Pn + Pthd} \qquad (13)$$

where Pthd is the power in the first several harmonics

- the effective number of bits is based on ideal quantization SNR

$$ENOB = \frac{SNDR(dB) - 1.76}{6.02} \qquad (14)$$

- practical ENOB with $Pn \approx Pq$

$$ENOB = N - 1 \qquad (15)$$

- energy per effective conversion

$$E = \frac{Pd}{Fs \cdot 2^{ENOB}} \qquad (16)$$

where Pd - power dissipation (W)
Fs - sampling rate (Hz)

state of the art designs E = 1-1.5 pJ / effective conversion (scaled pipelines)

ENOB and power estimation (cont'd)

- power dissipation depends strongly on the thermal noise
- power dissipation depends weakly on the quantization noise
- power efficiency if $Pn \gg Pq$ (noise limited by thermal, rather than quantization) implies

$$ENOB < N - 1 \qquad (17)$$

V. Practical limitations

V.1 SNR limitations

- thermal noise (limited by power dissipation and silicon area)

- clock jitter determines an equivalent signal noise

$$Pj = (2^{N-1} \cdot 2 \cdot \pi \cdot f_{in})^2 \cdot \overline{\Delta t_{jitter}{}^2} \tag{18}$$

  that limits the achievable SNR to

$$SNR = \frac{1}{\pi \cdot fin \cdot \Delta t_{jitter}} \tag{19}$$

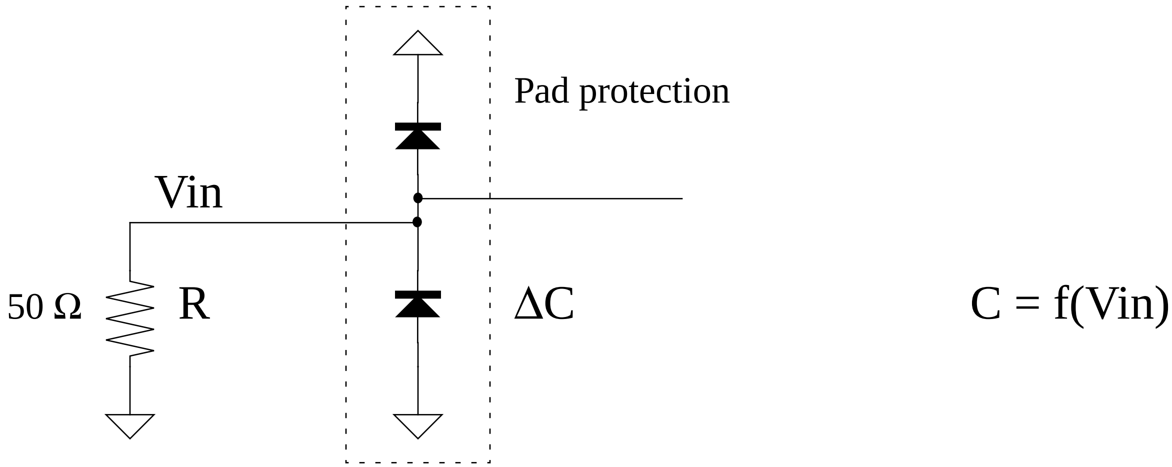
  example: 1 ps rms jitter limits a 50 MHz input signal to 76 dB or 12.3 ENOB

- quantization noise
- calibration quantization and calibration noise
- pick-up/substrate noise

V.2 THD limitations

- input pad non-linear capacitance

$$THD \approx fin \cdot R \cdot \Delta C \qquad (20)$$

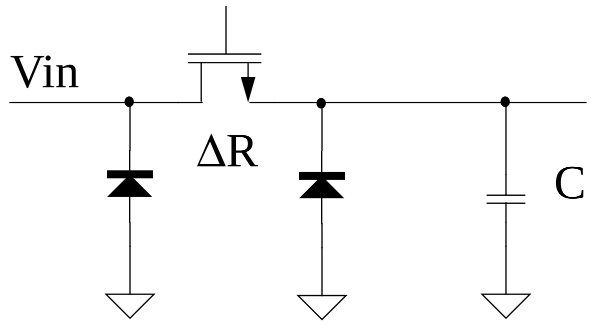


- example: R=50 Ω, ΔC = 1 pF, fin = 20 MHz, THD = 0.1 % or -60 dB (single ended)
- solutions:
  - fully differential implementations (even order harmonic cancellation);
  - bootstrapping of input node (reduce ΔC);
  - reduce signal source impedance (R);
  - use a transimpedance amplifier (the input pad is a virtual ground node);
  - calibration and correction of non-linearity;

THD limitations (cont’d)

- sample and hold switch non-linearity

$$THD \approx fin \cdot \Delta R \cdot C \qquad (21)$$

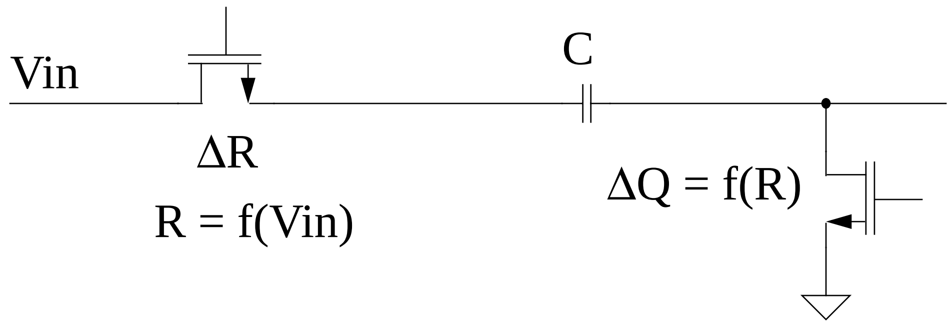


R = f(Vin)

- solutions:
  - fully differential implementations (even order harmonic cancellation);
  - bootstrapping of sampling switch (reduce ΔR - limited by size and back bias);
  - reduce loading (C - limited by thermal noise);
  - use a closed loop S/H implementations (slow and high power dissipation);
  - calibration and correction of non-linearity;

THD limitations (cont’d)

- signal dependent residual charge injection



- opamp finite loop gain and non-linear transfer function
- stage finite settling
- calibration noise and calibration quantization

VI. Systems and specifications revisited

VI.1 10-bit A/D specifications:

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issues:

- SNR implies ENOB = 9.67
- no margin for thermal noise
- margin for jitter -74.6 dB
- clock jitter < 0.3 ps rms

I.2 8-bit A/D specifications:

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issues:

- SFDR ~ 9*N dB is limited by ideal quantization

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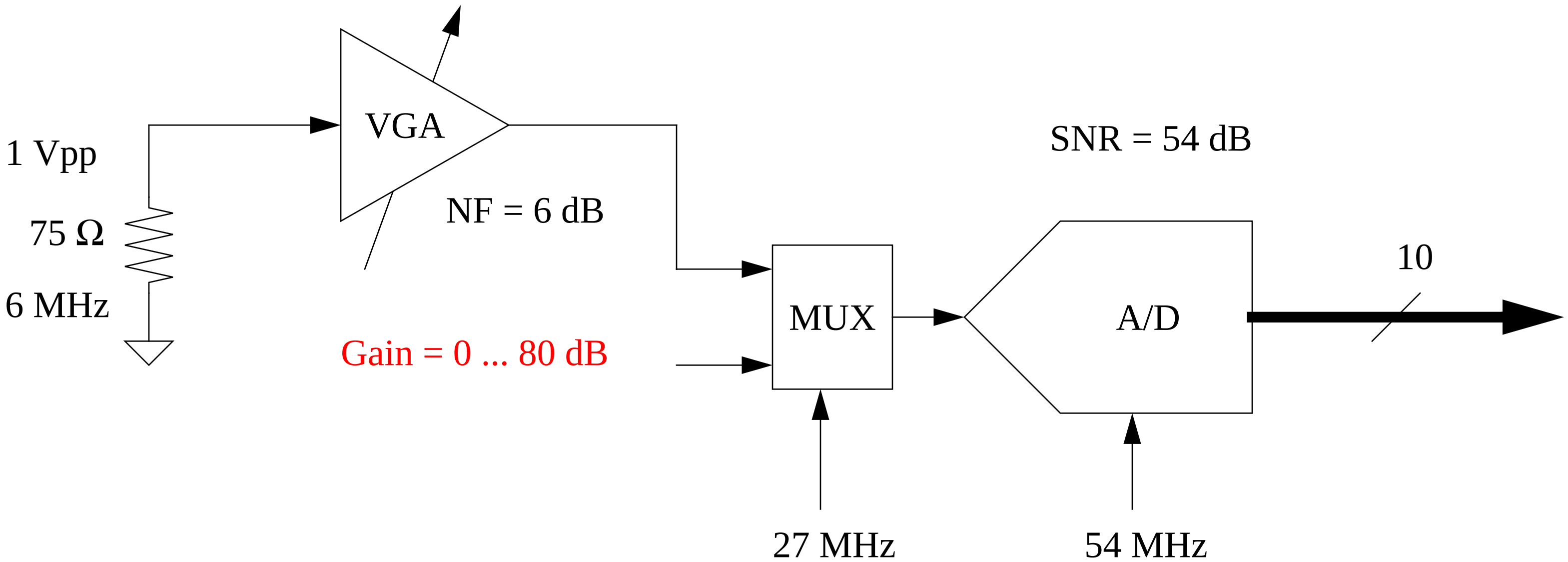


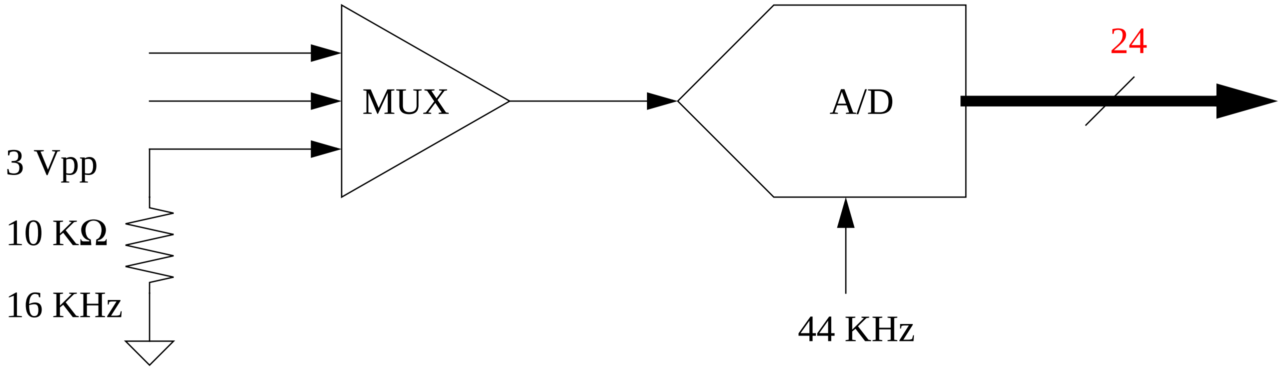
input noise:

$$Vn = \sqrt{4 \cdot k \cdot T \cdot B \cdot R} = 2.7\ \mu Vrms \tag{22}$$

max. SNR

$$SNR = \frac{Vin_{rms}}{Vn} = 102.4\ dB \tag{23}$$

I.4 Audio system



input noise:

$$Vn = \sqrt{4 \cdot k \cdot T \cdot B \cdot R} = 1.6\ \mu Vrms \tag{24}$$

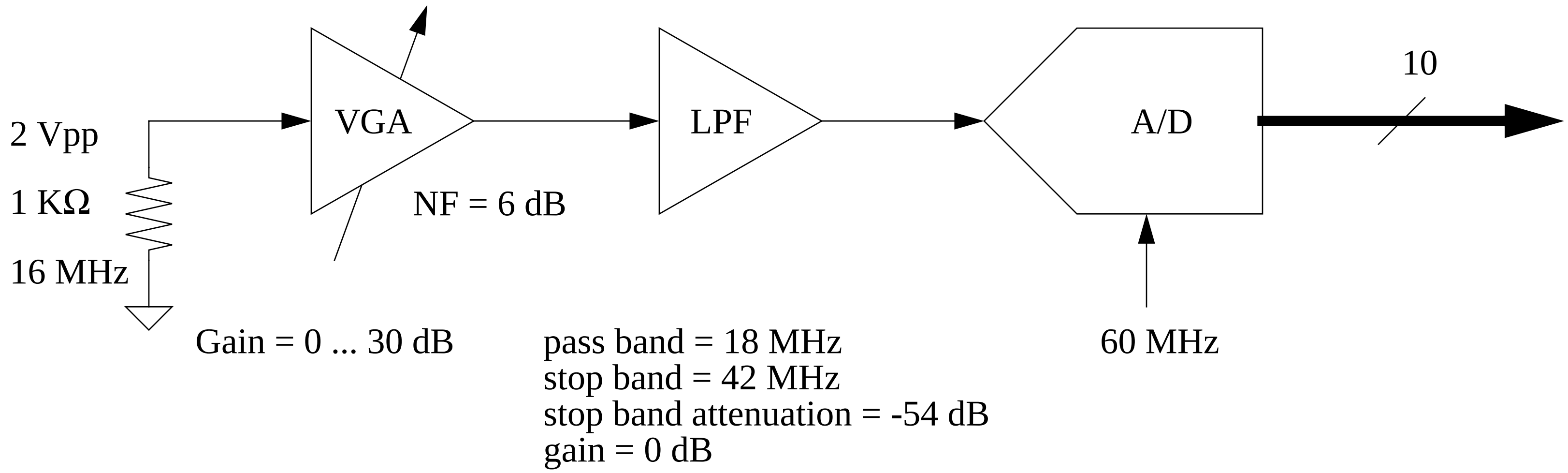
max. SNR

$$SNR = \frac{Vin_{rms}}{Vn} = 116.4\ dB \tag{25}$$

max. ENOB

$$ENOB = \frac{SNR - 1.76}{6.02} = 19\ bit \tag{26}$$

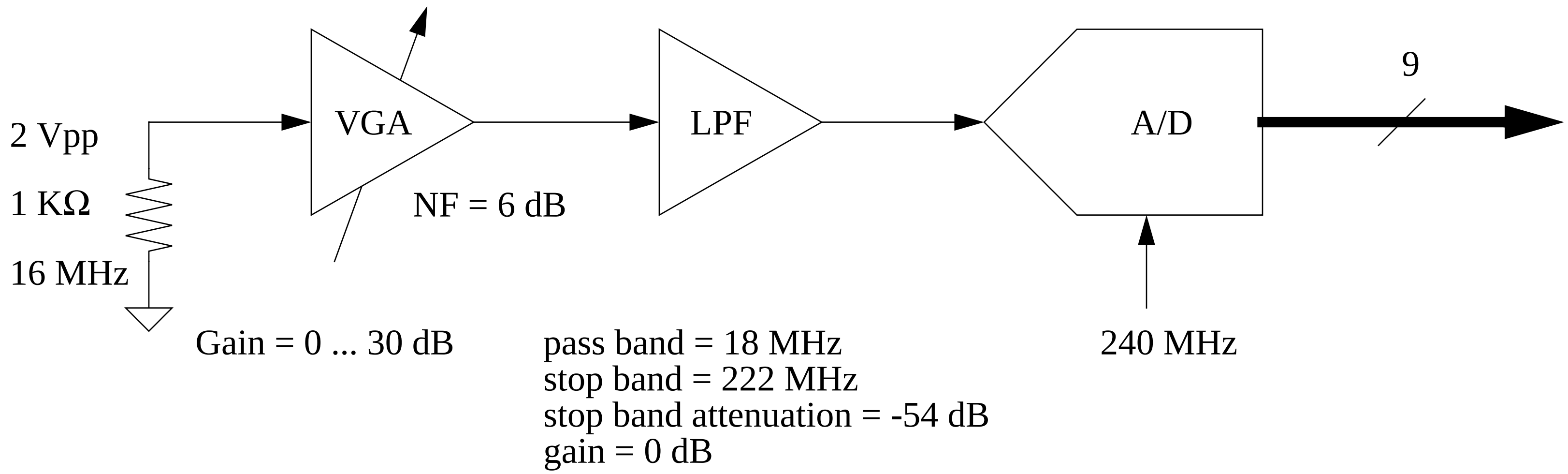
I.5 Receiver IF/baseband



- issues:
  - LPF needs a 7th order Chebyshev or 5th order elliptic;
  - LPF needs tuning within +/- 2%;

Receiver IF/baseband (cont'd)

alternative implementation



LPF: - untuned 3-pole;

VII. Summary

- Fundamental limitations based on ideal quantization can not be violated
- Real limitations are seriously degrading the A/D performance
- There are many limitations outside the A/D design (clock jitter, pad protection non-linearity)
- Best power efficiency is for ENOB < N-1
- Reduce quantization noise (It’s always easier to implement a N+1 bit converter rather than an N-bit converter for same performance)
- Use a system approach and challenge system assumptions for best use of the ADC